NAT-MCH-SCIx52

The **NAT-MCH-SCIx52** is a pre-configured package aiming for the special demands of the science community, featuring high-speed Ethernet connections as well as broad FatPipe bandwidth.

It comprises of the **NAT-MCH-S4** Carrier Hub (the double-width variant of the **NAT-MCH-G4**), a **NAT-MCH-G4-CLKP** clock mezzanine, and a **NAT-MCH-G4-HUB-Px52** Hub module.

With reagards to the base fabric (FabricA), the combination features 1G / 2.5G / 10G FabricA connections to each AMC, as well as a two 1GbE available at two RJ45 interfaces at the front panel. As an assembly option the RJ45 interfaces could be replaced by SFP fibre uplinks.

CLK1 and CLK2 (MLVDS signalling standard) can be routed by two low-jitter clock multiplexers, while CLK3 is carried out as a PCIe Reference Clock (100MHz Spread Spectrum Clock, HCSL). A precision timing option consisting of a GPS input and an onboard OCXO is available as seperately orderable assembly option.

By the 52 lanes of its PCIe switch, the **NAT-MCH-SCIx52** offers PCIe Gen4 x4 to all 12 AMCs (or x8 for up to six AMCs if supported by the backplane) as well as a PCIe Gen4 x4 uplink via QSFP at the front.

NAT-MCH-S4 Base Board Features

- Double-width, full-size MCH
- IPMI
- Console via USB and web interface
- 16 LEDs reflecting AMC / CU / PM status
- Firmware update via HPM
- Graphical system and FRU status
- Front Uplink (assembly options):
  - 1-10G Base Ethernet via RJ45 or
  - 1-25G optical Base Ethernet via SFP-28-DD
- Backplane:
  - Up to 12x 1GbE / 2.5GbE / 10GbE

NAT-MCH-G4-CLKP Features

- CLK1 / CLK2 (MLVDS): 2x low-jitter cross-point mux
- CLK3: PCIe Ref CLK (HCSL)
- PLL synthesizer
- CLK IN / OUT via SMA
- Optional precision timing support

NAT-MCH-G4-HUB-Px52 Features

- Microchip PFX PCIe x52 Gen4 Switch
- Front panel uplink via QSFP (PCIe Gen4 x4)
- Backplane PCIe Gen4:
- 12x PCIe Gen4 x4 / 6x PCIe Gen4 x8 (depending on backplane)

Refer to the **product website** or the **Technical Reference Manual** for more information.

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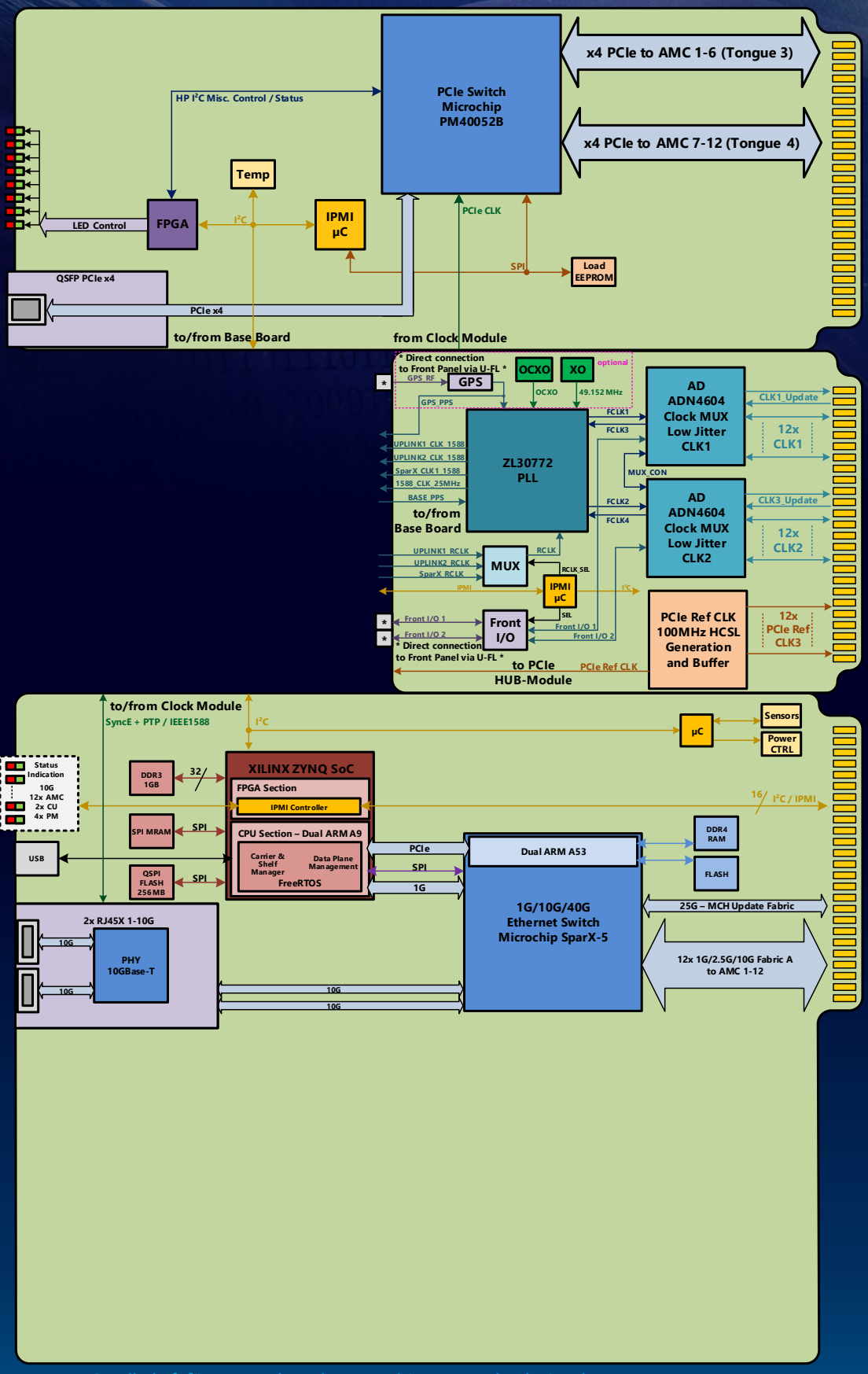

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