NAT-MCH-Gen4
Clock-Module
User Manual V1.3

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Note:

The release of the User Manual is related to a certain HW board revision.
For HW revisions earlier than the one given chapter “Supported HW Revisions“ please contact N.A.T. for the corresponding older Manual release.

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Conventions

If not specified otherwise, addresses and memory maps are provided in hexadecimal notation, identified by *0x*. Table 1 lists the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
CRC	Cyclic Redundancy Check
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MUX	Multiplexer
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
Rx	Receiver
RAM	Random Access Memory
(P)ROM	(Programmable) Read Only Memory
PLL	Phase Locked Loop
SFP	Small Form-Factor Pluggable
TCKL	Telecom Clock

1 INTRODUCTION

1.1 FUNCTIONAL OVERVIEW

The **NAT-MCH-G4-CLK** is a mezzanine module for the NAT-MCH-G4 MCH supporting telecom clocks TCLKA and TCLKB as well as a 100Mhz FCLKA for PCIe modules. The module provides support for manipulating the various input clocks and routing of the clocks to the desired outputs. To allow a flexible interconnect, the module is equipped with two crosspoint switches and a local PLL. The output of either a local oscillator or an oven controlled oscillator can be used as a reference input to the PLL.

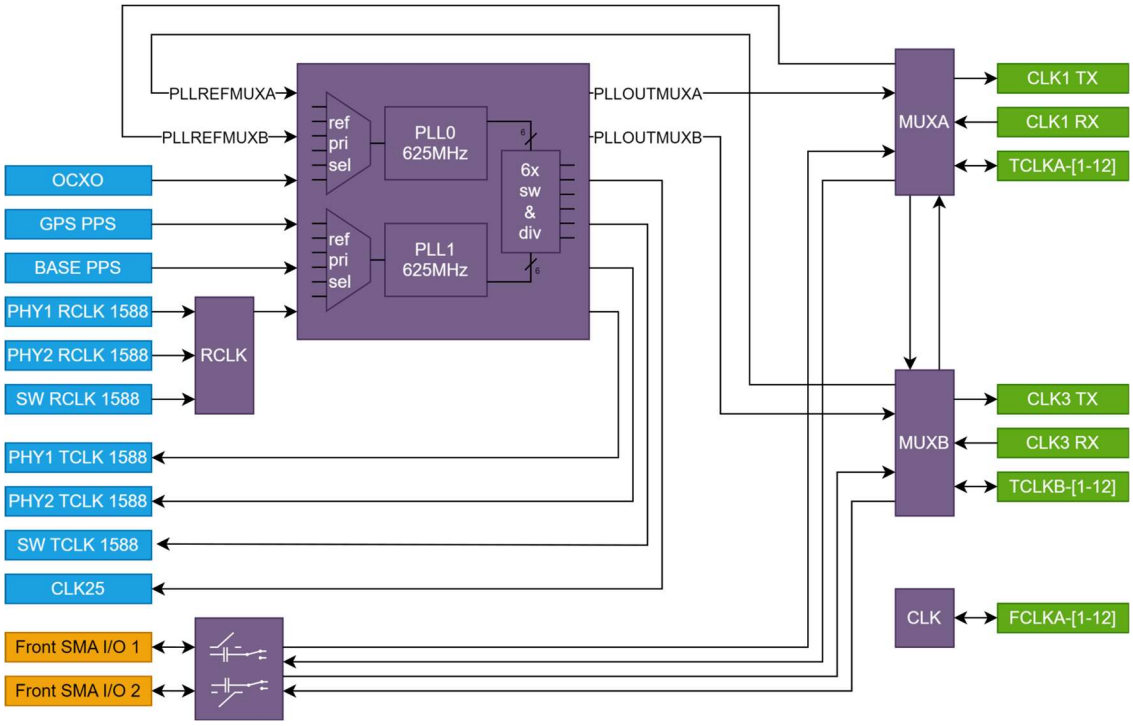


Figure 1: MCH-G4 Clock Module Blockdiagram

Figure 1 shows an overview of the clock module and possible interconnects. The inputs and outputs of the clock module shown in blue are located on the connector to the MCH base module. The front panel SMA connections are shown in orange. The backplane connections are shown in green. Everything that illustrates the internal functionality is coloured in purple.

The PLL system consists of PLL0 and PLL1 and has 6 reference inputs and 6 outputs. For each PLL (0 and 1) a reference priority list is configurable. A source PLL can be selected for each of the 6 outputs. Furthermore, the fixed PLL frequency of 500 MHz can be changed for each output via an adjustable frequency divider.

Front I/O signals can be switched between input and output and AC or DC coupling.

1.2 INPUT CLOCK SIGNALS

The clock module receives its input from the following clock sources:

- Front I/O coax connector at the front panel of the MCH (*)
- IEEE1588 reference clock input which is recovered from either the Ethernet PHYs or the Ethernet switch located on the base board
- TCLKB as coming from the backplane (**)
- CLK1_RX, CLK3_RX as coming from the backplane
- GPS 1pps signal

Both front I/O signal can be switched between Input/Output and AC/DC coupling.

1.3 OUTPUT CLOCK SIGNALS

Depending on the type of clock signal, the input clock signal can either be connected directly to one of the output signals or being routed through the onboard PLL and then connected to one of the output signals. Possible connections will be detailed in chapter 2.1. The module can provide the following output signals:

- Front I/O to coax connector located at the front panel (*)
- IEEE1588 synchronized output clocks
- TCLKA – Backplane Telecom Clock A (***)
- FCLKA – Backplane Fabric Clock A – a 100Mhz reference clock for PCIe applications. This clock is always on and can't be configured
- CLK1_TX, CLK3_TX backplane clocks

* Both front I/O signal can be switched between Input/Output and AC or DC coupling.

** TCLKB usually is the backplane clock input to the MCH. On the MCH Gen4 this clock can be configured as output to the AMCs as well. Users who want to make usage of this option should take care of possible termination issues.

*** TCLKA usually is the backplane clock output from the MCH. On the MCH Gen4 this clock can be configured as clock input to the MCH as well. Users who want to make usage of this option should take care of possible termination issues.

2 CONFIGURATION - OVERVIEW

In its basic operation the clock module builds a connection between an input clock and one or multiple output clocks. The input signal can either be directly connected to one of the outputs or being routed through the onboard PLL. The purpose of the onboard PPL is to stabilize and convert the input clock signal into an output clock signal. I.e. convert a 1pps input clock signal to a 10MHz output clock signal.

All type of clock signals can be configured individually.

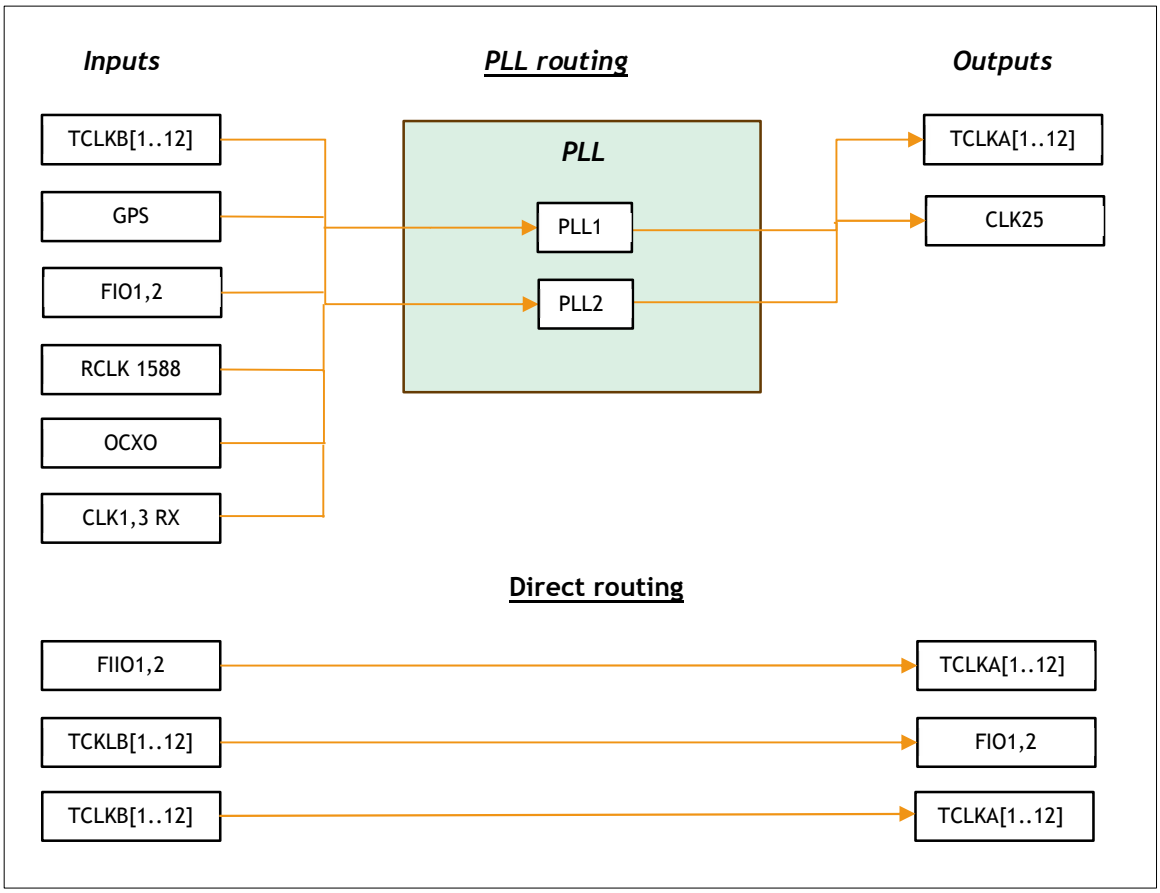
The table in Appendix A gives an overview about the various input and output signals as well as internally generated signals by the onboard devices. For the ease of addressing or configuration of these signals they are named “nodes” in the following chapters.

Each node has been assigned a symbolic name and an ID for addressing these nodes by the MCH CLI or by IPMI commands.

2.1 CLOCK ROUTING

The connection diagram below shows all possible clock interconnects:

Please note that multiple connections are possible, for example a TCLKB input can be routed to the PLL and in parallel to the front I/O connector FIO2. But the connection matrix is not completely orthogonal, limitations arise from internal resources. Table 2 gives an overview about the limitations.



2.1.1 Exclusive Connections

The following table shows the internal routing limitations. The routing between certain inputs nodes and certain output nodes is limited to one exclusive connection:

Table 2: Routing Limitations

Input Nodes	Constraint	Output Nodes
PHY1_1588 PHY2_1588 SW_1588	One of	PLL0, PLL1
FIO1 CK1_RX	One of	PLL0, PLL1
FIO2 CLK2_RX TCKLB[1..12]	One of	PLL0, PLL1, TCKLA[1..12]

An attempt to route multiple connections between those nodes leads to an error code being returned.

2.2 PLL Configuration

The PLL block of the MCH clock module has two independent PLLs (PLL0, PLL1). Each of the PLLs can be configured individually. The recommended PLL configuration sequence is outlined below:

1. Apply a routing between input clocks and one of the PLLs
2. Apply a routing between a PLL and one of the output clocks
3. Set the reference input frequency (optional, depending on input)
4. Set the reference priority
5. Set the output frequency
6. Enable the PLL

The configuration nodes within the can be found in Appendix A.

2.2.1.1 Setting the PLL Reference Input

The reference inputs are common for both PLLs. Each PLL can be assigned one or multiple reference inputs. The following table lists the input signals that can be used as refence inputs to the PLLs. can be set. Furthermore, it is not necessary to set the frequency for inputs with a fixed function, as the correct frequency is already set automatically at system startup (marked with *).

To set a reference input use a routing command to route the desired input to one of the PLLs.

Table 3: Possible PLL Reference Inputs

Input	Description
FIO1	Front Coax Connector Input/Output 1
FIO2	Front Coax Connector Input/Output 2
PHY1_1588*	IEEE1588 reference input from Phy1
PHY2_1588*	IEEE1588 reference input from Phy2

SW_1588*	IEEE1588 reference input from ethernet switch
GPS_PPS*	1 pps signal from GPS receiver
OCXO*	Reference frequency from Oven Controlled Oscillator
BP_CLK1	Reference clock from backplane signal RX_CLK1 (*)
BP_CLK3	Reference clock from backplane signal RX_CLK3 (*)

(*) requires setting of reference frequency – see below

2.2.1.2 Set the Reference Input Frequency

The expected input frequency must be set for the references used.

The following table shows the predefined frequencies

Valid Frequencies in Hz to be set are 1, 10, 25, 100, 250, 500, 1k, 10k, 25k, 50k, 100k, 250k, 500k 1M, 10M, 25M, 50M and 100M.

PLLs are getting disabled when the reference frequency input settings is changed.

2.2.1.3 Set the reference input priority

If multiple input signals are routed to the PLL, the PLL can automatically switch between the input signals according to the priority assigned to the input signals. I.e. if the signal with highest priority becomes instable or disappears, the PLL automatically switches to the signal with the second highest priority and so on.
Priority 0 is the highest and the default. A value of 15 disables the reference input. If a reference input frequency fails, which can be detected as the expected frequency was previously configured, the system automatically switches to the input with the next highest priority.

2.2.1.4 Configure a PLL output

The configuration of the PLL outputs includes the setting of a desired output frequency and the selection of which PLL (0/1) of the PLL system serves as the source for the respective output. Table 4 lists all signals that are PLL outputs and can therefore be configured as described.

Table 4: PLL Outputs

Signal	Description
PHY1_TCLK_1588	1588 Clock to Uplink 1 PHY
PHY2_TCLK_1588	1588 Clock to Uplink 2 PHY
SW_TCLK_1588	1588 Clock to Base Switch
CLK25	1588 synchronous 25MHz Clock
FIO1	Output to Coax Front I/O 1
FIO2	Output to Coax Front I/O 2
TCLKA1-12	Telecom Clock A to AMCs
TCLKB1-12	TCLKB Inputs from AMCs

The valid Frequencies are listed in Appendix A.

2.2.1.5 Enable the PLL

When the PLL system is fully configured for the desired use, the individual PLLs (1/2) can be activated.

2.2.2 Setting the Front I/O AC/DC Coupling

The Front I/O interface can be configured for AC or DC coupling. Possible configuration items are:

Table 5: AC/DC Coupling

Conf. Item	Coupling	Applicable Nodes
FIO_AC	AC	FIO1, FIO2
FIO_DC	DC	FIO1, FIO2

The default mode after power up is DC coupling !

2.2.3 Resetting the Clock Configuration

The complete clock configuration can be set into the initial state after power up with the RESET command.

Table 6: Configuration reset

Conf. Item	Applicable Nodes
RESET	GEN

3 CLI / SCRIPT BASED CLOCK CONFIGURATION

The configuration of the clock module is supported through the command line interface (CLI) of the MCH. To configure the clock module either individual commands can be entered at the MCH's console or a complete set of configuration commands can be provided to the clock module by the MCH's script functionality.

The basic syntax of the CLI commands for clock routing and configuration are:

Set clock route [site] [src_node] [dst_node]

Set clock route [site] [src_node] [fst_node] [lst_node]

Set clock config [site] [node] [config_item] [value]

[site] = 1 or 2 for MCH1 or MCH2

[node] = clock signal symbols according to Appendix A.

[config_item] = clock configuration items according to Appendix A.

[value] = to configure the Priority this are values in the range 0-15
a frequency is configured by using the frequency IDs according to Appendix A

3.1 EXAMPLES:

3.1.1 Basic Routing Example

Establish a clock routing on the clock module of MCH1 and route the input clock (TCLKB3) from AMC3 to the TCLKA5 output for AMC5:

Set clock route 1 TCLKB3 TCLKA5

3.1.2 Multi-Endpoint Example

Route the Front I/O signal 1 (FIO1) to all TCLKA outputs:

Set clock route 1 FIO1 TCLKA1 TCLKA12

3.1.3 Complex Routing Example with PLL

- *Route the Front I/O signal 1 (FIO1) to PLL0 and PLL2.*
- *Verify that the input frequency is 25MHz (ID=17).*
- *Connect the PLL0 output to the TCLKA signals and the PLL1 output to the TCLKB signals.*
- *Set the output frequency for TCLKA to 50MHz(ID=18) and TCLKB frequency to 1Hz(ID=1).*
- *Enable both PLLs*

```
set clock route 1 FIO1 PLL0_REF
set clock route 1 FIO1 PLL1_REF
set clock route 1 PLL0_OUT TCLKA1 TCLKA12
set clock route 1 PLL1_OUT TCLKB1 TCLKB12

set clock config 1 FIO1 PLL_REF_FREQ 17
set clock config 1 FIO1 PLL0_REF_PRIO 0
set clock config 1 FIO1 PLL1_REF_PRIO 0

set clock config 1 TCLKA1 PLL_OUT_FREQ 18
set clock config 1 TCLKB1 PLL_OUT_FREQ 1

set clock config 1 PLL0_OUT PLL_EN
set clock config 1 PLL1_OUT PLL_EN
```

3.1.4 Configuration Reset Example

```
set clock config 1 GEN RESET
```

4 IPMI BASED CONTROL CONFIGURATION:

All IPMI configuration commands send to the clock module are using an extension of the IPMI_NETFN_CONTR0_REQ command. The IPMI interface uses the same commands, configuration items and values as the CLI. The following commands are supported:

Table 6: Clock IPMI Commands

#	Command Description	Identifier	Value
0x20	Set routing between a clock input and output	IPMI_CMD_CLK_ROUTE	0x1A
0x21	Set clock configuration	IPMI_CMD_CLK_CONF	0x1B

Table 7: Set Clock Route Command

	Byte	Field description
Request	1	PICMG®-defined group extension command - 0x00
	2	Control information [7..1] – unused 0 : on / off control 1b = switch route on 0b = switch route off
	3	Clock Input ID: Rever to Appendix A for valid Clock Node IDs
	4	Clock output ID ID of a single output clock or the first clock of a clock range Rever to Appendix A for valid Clock Node IDs
	(5)	Clock output ID – optional - used for clock range definition only Last Clock ID to be configured
Response	1	Completion Code

Table 8: Set Clock Configuration Command

	Byte	Field description
Request	1	PICMG®-defined group extension command - 0x00
	2	Clock ID
	3	Node ID – refer to Appendix A
	4	Config_item – refer to Appendix A
	5	Value – a configuration value - optional
Response	1	Completion Code

Appendix A: Configuration Nodes and Items

Table 9: Configuration Nodes

Symbol	Description	NodeID
Output Nodes		
TCLKA[1..12]	Telecom Clock A to AMCs (*)	[0x01..0x0c]
TCLKC[1..12]	Telecom Clock C to AMCs (*) (**)	[0x21..0x2c]
FCLKA[1..12	Fabric Clock A to AMCs	[0x31..0x3c]
SW_TCLK1588	1588 Clock to Base Switch	0x40
PHY1_TCLK1588	1588 Clock to Uplink 1 PHY	0x41
PHY2_TCLK1588	1588 Clock to Uplink 2 PHY	0x42
CLK25_1588	1588 synchronous 25MHz Clock	0x43
CLK1_TX	Backplane clock TX1	0x46
CLK3_TX	Backplane clock TX3	0x47
Input Nodes		
TCLKB[1..12]	TCLKB Inputs from AMCs (***)	[0x11..0x1c]
MCLK	Local 49.152 MHz Oscillator	0x50
GPS	PPS Signal generated by onboard GPS module	0x51
OCXO	Oven controlled oscillator located on the base MCH	0x52
SW_PPS	1 pps clock generated by the Base Switch	0x53
SW_RX1588	Recovered IEEE1588 clock from base switch	0x54
PHY1_RX1588	Recovered IEEE1588 Clock from Uplink 1 PHY	0x55
PHY2_RX1588	Recovered IEEE1588 Clock from Uplink 2 PHY	0x56
CLK1_RX	Backplane clock RX1	0x57
CLK3_RX	Backplane clock RX3	0x58
Bi-Directional Nodes		
FIO1	Clock Input/Output at Front Coax I/O 1	0x44
FIO2	Clock Input/Output at Front Coax I/O 2	0x45
Internal Nodes		
PLL0_REF	PLL0 input node	0x60
PLL0_OUT	PLL0 output node	0x61
PLL1_REF	PLL1 input node	0x70
PLL1_OUT	PLL1 output node	0x71
Generic		
GEN	Node for generic clock module functions	0xf0

(*) Can optionally be configured as input

(**) Not available on NAT-MCH-G4-CLK

(***) can optionally be configured as output

Table 10: Configuration Items

Symbol	Description	ItemID
Configuration Items		
PLL_REF_FREQ	PLL Reference Frequency configuration	0x01
PLL0_REF_PRIO	PLL0 Input Priority setting	0x02
PLL1_REF_PRIO	PLL1 Input Priority setting	0x03
PLL_OUT_FRE	PLL output Frequency setting	0x04
PLL_EN	PLL output enable	0x05
PLL_DIS	PLL disable	0x06
FIO_AC	Set front I/O interface to AC coupling	0x07
FIO_DC	Set front I/O interface to DC coupling	0x08
RESET	Generic configuration reset	0x09

Table 11: Input / Output Frequency Assignments

Frequency	Input	Output	ID
1 Hz	□	□	1
10 Hz	□	□	2
25 Hz	□	□	3
50 Hz	□	□	4
100 Hz	□	□	5
250Hz	□	□	6
500Hz	□	□	7
1 KHz	□	□	8
10 KHz	□	□	9
25 KHz	□	□	10
50 KHz	□	□	11
100 KHz	□	□	12
250KHz	□	□	13
500KHz	□	□	14
1MHz	□	□	15
10 MHz	□	□	16
25 MHz	□	□	17
50 MHz	□	□	18
100 MHz	□	□	19
250 MHz		□	20
500 MHz		□	21

Appendix B: Reference Documentation

[1] Zarlink, ZL30772 PLL Data Sheet

[2] Analog Devices, AD4604 digital Crosspoint Switch

Appendix C: Document's History

Revision	Date	Description	Author
1.0	18.9.24	initial release	hl
1.1	3.12.24	Added field for PICMG identifier to ipmi messages	hl
	5.2.24	Reworked nodes and configuration table	hl
1.2	13.2.25	Added Frequency table	hl
1.3	16.4.25	Added Configuration items for AC/DC coupling and generic configuration RESET command	hl