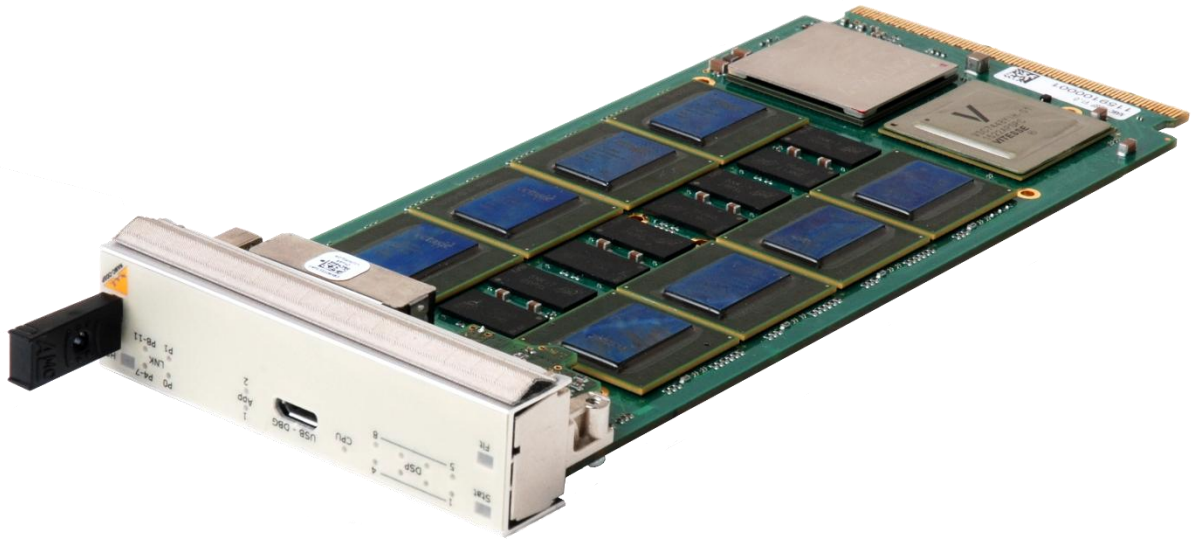
NAMC-ODSP-M

DSP BASED MEDIA PROCESSING/GATEWAY AMC MODULE

DESIGNED BY N.A.T. GMBH



PROGRAMMING MANUAL V1.0

HW REVISION 1.X

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1. PREFACE

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Note:

The release of the Programming Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAMC-ODSP-M's** programming capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAMC-ODSP-M's** main functionality and application field

Programming Notes

Detailed information on the programming options of the **NAMC-ODSP-M**

FPGA Register Description

Schedule of the most important FPGA registers

Document's History

Revision record

Note:

It is assumed, that the **NAMC-ODSP-M** is handled by qualified personnel only!

2. INTRODUCTION

The **NAMC-ODSP-M** is a DSP based media processing/gateway AMC which offers the opportunity to add video and audio acceleration to an ATCA or MTCA systems. This covers many advanced audio / video applications, conferencing systems, audio / video transcoding, video surveillance and T.38 fax relay applications.

The software provides an Ethernet packet-based configuration API so no DSP programming is required. It offers a very flexible architecture so that it can be easily prototyped, developed and deployed.

3. PROGRAMMING NOTES

3.1. Console Interfaces

3.1.1. Serial Interface

The **NAMC-ODSP-M** provides a serial command line interface (115200 bps, 8 data bits, no flow control) through the MicroUSB connector on the front plate. This provides an administrative interface and the ability to view the system logs.

3.1.2. Telnet Interface

A telnet console is also available on the board, but is disabled by default. This must be manually enabled through the board's web interface.

The telnet interface functions as a mirror of the serial interface; all data and commands that appears in the serial interface will be shown in the telnet interface, and vice versa.

3.1.3. Console Commands

The following commands are available on the command line:

- `format_flash`: Completely erase and format the flash filesystem
- `erase_eeprom`: Completely erase the EEPROM (the board configuration, including password)
- `show_eeprom`: Show the contents of the EEPROM
- `ip`: Show and/or edit the networking configuration
- `free`: Show available kernel memory
- `conf`: Print configuration
- `itdm_diag`: Enter itdm diagnostics
- `ps`: Show running processes
- `version`: Show version information
- `show_log`: Show recent log entries
- `mm`: Memory modify, modifies the byte at the given hex address. Usage: `mm <addr> <value>`
- `md`: Memory display, displays the value of the byte at the given hex address. `Usage: `md <addr>`

- `md16`: Memory display (16 bit), displays the value of 2 bytes at the given hex address. Usage: `md16 <addr>`
- `reset_dsp`: Reset a DSP (requires a reboot to bring it back online). Usage: `reset_dsp <dsp number>`
- `itdm`: Show the ITDM clock status

3.2. Web Interface

The web interface provides for basic configuration of the board, and provides a series of JSON REST API endpoints. The web interface is protected with HTTP Basic authentication. The username is `nat`, and the default password is `nat123`; this should be changed using the web interface or REST API in production.

3.2.1. REST API

All REST API endpoints require HTTP Basic authentication.

3.2.1.1. API Version 1

- `/api/v1/info`: board information (GET only)
- `/api/v1/config`: board configuration (GET or POST)
- `/api/v1/eth`: ethernet statistics (GET only)
- `/api/v1/dsp`: DSP information (GET only)
- `/api/v1/itdm`: ITDM statistics (GET only)
- `/api/v1/update`: firmware update (POST only)
- `/api/v1/password`: password update (POST only)
- `/api/v1/updateDSP`: DSP firmware update (POST only)
- `/api/v1/erase`: erase the flash filesystem (POST only)
- `/api/v1/log`: returns the console log buffer (GET only)

3.3. Board Control Interface

The **NAMC-ODSP-M** can be controlled from a host system via **M**essage **I**nterface (MIF).

For detailed information, please refer to chapter 5 Reference Documentation.

3.4. Networking

The **NAMC-ODSP-M** connects to the AMC backplane with a 1000Base-X Ethernet interface. This port is deactivated during the boot process, in order to isolate the DSPs and application so that the DHCP requests and replies are handled properly.

The application is configured by default with the following network settings:

Table 1 – Network Configuration

Parameter	Value
IP Address	192.168.1.240
Subnet Mask	255.255.255.0
Gateway	192.168.1.1

The network configuration can be modified using the `ip` console command, or by using the web interface.

3.5. Software Updates

The application and DSP firmwares can be updated either using the web interface, or the appropriate REST API endpoint.

To use the web interface, navigate to the application website, and open the Maintenance page. From there, use either the "Firmware upgrade" controls, or the "DSP boot image" controls, depending on what needs to be updated.

To use the REST API endpoints, post the raw binary contents of the firmware file to either `/api/v1/update` or `/api/v1/updateDSP` (including the appropriate authentication header), whichever is appropriate.

3.6. Upgrading from Linux

Starting from version 2.0 of the NAMC-ODSP-M software, the system is based on FreeRTOS. Due to the massive overhaul of the entire software stack and the new upgrade processes, a special process is required to upgrade from 1.x versions of the software (which are based on Linux) to the new version 2.x series. This process is described in the following sections.

3.6.1. Requirements

- `NAMC-ODSP-M_update.bin`: combined update package (containing the FPGA bitstream and application binary - different to the FreeRTOS firmware upgrade packages)
- FTP client
- MicroUSB cable

- Serial console software

3.6.2. Method

Note: This will erase the entire contents of both flash storages!

1. Transfer the `NAMC-ODSP-M_update.bin` file to the board using an FTP client.

2. Erase the flash on the board with the following command: \

```
`flash_erase /dev/mtd4 0 0`
```

3. Program the new firmware image to the flash with the following command: \

```
`update_firmware /var/ftp/NAMC-ODSP-M_update.bin`
```

4. Wait for the script to finish writing and verifying the new image.

5. Power cycle the board to boot into the new FreeRTOS-based system.

3.6.3. Setup

On the first boot, the **NAMC-ODSP-M** will not have any image with which to program the DSPs. In order to flash an image, you need to connect to the board with a MicroUSB cable and open a serial console (115200 Baud, flow control off).

Use the `ip` command to modify the network configuration as necessary (the board will have the default IP address of `192.168.1.240/24`), and then power cycle the board to apply the changes.

When it has finished booting, open a web browser and navigate to the web interface of the board with the IP address you have just set. The username for the web interface is "nat", and the default password is "nat123"; the password can be changed in the web interface.

Go to the Maintenance page and use the interface to upload a DSP image of your choosing. When it has finished uploading and saving the image, power cycle the board again.

The DSP LEDs on the front panel should light up as the boot process for each DSP completes. If any of the DSPs fail to boot due to a bad firmware image, its respective LED will blink.

3.7. TDM/ITDM Connectivity

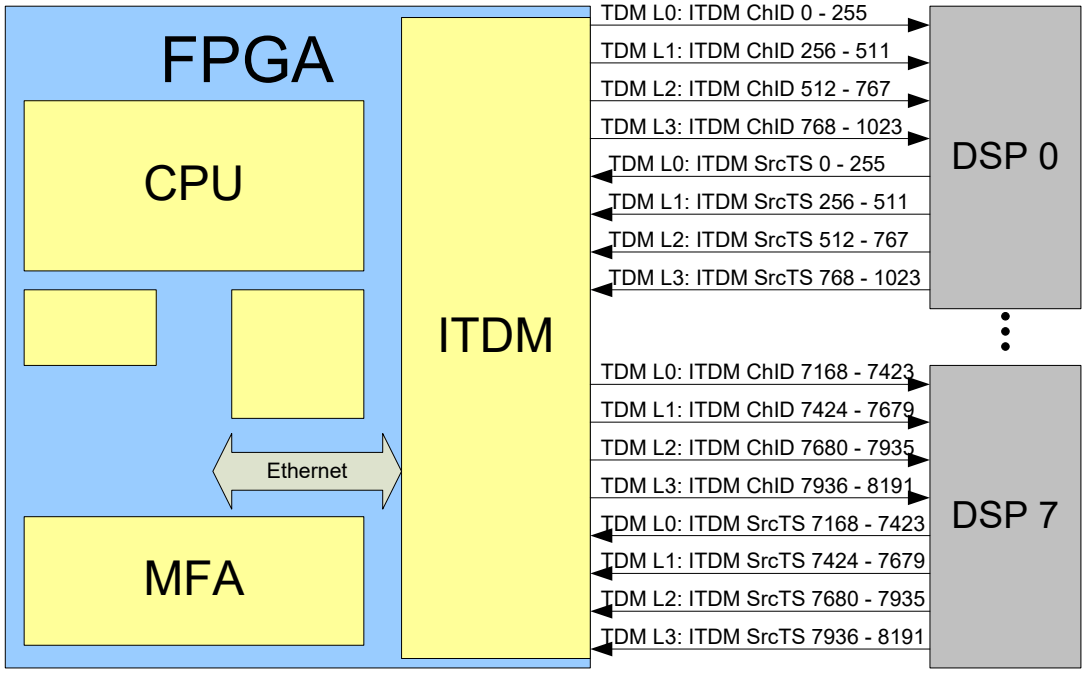
The block diagram below shows which ITDM channel-id is connected to which DSP TDM line and time-slot. There is a one-by-one relationship between the number of the ITDM channel-id in incoming direction and the ITDM engine local time-slot number in outgoing direction. The displayed connectivity can also be expressed in the following formula:

```
Ch-ID/Local-TS# = (DSP# * 1024) + (DSP-TDM-Line# * 256) + TS#
```

Table 2 – ITDM Ch-ID / Time-Slot Calculation

Parameter	Function
Ch-ID	ITDM Channel-ID: Data coming into the **NAMC-ODSP-M** on a certain Ch-ID will be connected to a specific DSP time-slot as documented here.
Local-TS#	Number of the local time-slot that can be connected to any outgoing ITDM connection towards another ITDM endpoint.
DSP#	Number of the DSP one the **NAMC-ODSP-M** ranging from 0 to 7.
DSP-TDM-Line#	Number of the physical TDM line of a DSP. Each DSP has four TDM lines towards the FPGA ranging from 0 to 3 (in the Vocallo API referred to as stream-id).
TS#	Number of the time-slot on a specific TDM line (stream-id) between FPGA and a DSP.

Figure 1 - NAMC-ODSP-M – TDM/ITDM Connectivity



4. FPGA REGISTER DESCRIPTION

The FPGA on the **NAMC-ODSP-M** implements various logical blocks. The following tables show the Misc_HDL_Block register definition. All registers are 32 bit wide, base address is 0x2004000.

Table 3 – 0x0000000 – BOARD_ID_REG

Bit	Name	Description	Default	Access
24..31		Reserved	na	Read Only
8..23	Board ID	Holds Board-ID	0x0B3B	Read Only
0..7	PCB Version	Holds PCB-Version	0x10	Read Only

Table 4 – 0x0000004 – FPGA_VERS_REG

Bit	Name	Description	Default	Access
16..31		Reserved	na	Read Only
8..15		FPGA_BLOCK_DESIGN_DEV_VERS	na	Read Only
0..7		FPGA_BLOCK_DESIGN_MAIN_VERS	na	Read Only

Table 5 – 0x0000008 – MISC_HDL_VERS_REG

Bit	Name	Description	Default	Access
16..31		Reserved	na	Read Only
8..15		MISC_HDL_BLOCK_DEV_VERS	na	Read Only
0..7		MISC_HDL_BLOCK_MAIN_VERS	na	Read Only

Table 6 – 0x000000C – GLOBAL_CONFIG_REG

Bit	Name	Description	Default	Access
0..31		TBD	na	R/W

Table 7 – 0x0000010 – GLOBAL_STAT_REG

Bit	Name	Description	Default	Access
6..31		TBD	na	Read Only
0..5		DIP_SW[6..1]	na	Read Only

Table 8 – 0x0000014 – LED_CTRL1_REG

Bit	Name	Description	Default	Access
28..31		PORT8-11_LINK_LED_CTRL	na	R/W
24..27		PORT4-7_LINK_LED_CTRL	na	R/W
20..23		PORT1_LINK_LED_CTRL	na	R/W
16..19		PORT0_LINK_LED_CTRL	na	R/W
12..15		APP2_LED_CTRL	na	R/W
8..11		APP1_LED_CTRL	na	R/W
4..7		CPU_LED_CTRL	na	R/W
0..3		AMC_STAT_LED_CTL	na	R/W

Table 9 – 0x0000018 – LED_CTRL2_REG

Bit	Name	Description	Default	Access
28..31		DSP8_LED_CTRL	na	R/W
24..27		DSP7_LED_CTRL	na	R/W
20..23		DSP6_LED_CTRL	na	R/W
16..19		DSP5_LED_CTRL	na	R/W
12..15		DSP4_LED_CTRL	na	R/W
8..11		DSP3_LED_CTRL	na	R/W
4..7		DSP2_LED_CTRL	na	R/W
0..3		DSP1_LED_CTRL	na	R/W

Table 10 – 0x0000018 – LED_CTRL2_REG

Bit	Name	Description	Default	Access
28..31		DSP8_LED_CTRL	na	R/W
24..27		DSP7_LED_CTRL	na	R/W
20..23		DSP6_LED_CTRL	na	R/W
16..19		DSP5_LED_CTRL	na	R/W
12..15		DSP4_LED_CTRL	na	R/W
8..11		DSP3_LED_CTRL	na	R/W
4..7		DSP2_LED_CTRL	na	R/W
0..3		DSP1_LED_CTRL	na	R/W

Table 11 – 0x000001C – PLL_CFG_REG

Bit	Name	Description	Default	Access
11..31		Reserved	na	R/W
8..10		PLL_IN2_SEL	na	R/W
7		Reserved	na	R/W
4..6		PLL_IN1_SEL	na	R/W
3		Reserved	na	R/W
2		PLL_CS_CA	na	R/W
1		PLL_AUTOSELECT	na	R/W
0		PLL_RST	na	R/W

Table 12 – 0x0000020 – PLL_STAT_REG

Bit	Name	Description	Default	Access
4..31		Reserved	na	Read Only
3		PLL_CS_CA	na	Read Only
2		PLL_LOS2	na	Read Only
1		PLL_LOS1	na	Read Only
0		PLL_LOL	na	Read Only

Table 13 – 0x0000024 – DSP_RST_REG

Bit	Name	Description	Default	Access
8..31		Reserved	0xAFFE00	R/W
7		DSP8_RST	na	R/W
6		DSP7_RST	na	R/W
5		DSP6_RST	na	R/W
4		DSP5_RST	na	R/W
3		DSP4_RST	na	R/W
2		DSP3_RST	na	R/W
1		DSP2_RST	na	R/W
0		DSP1_RST	na	R/W

Table 14 – 0x0000028 – DSP_INT_REG

Bit	Name	Description	Default	Access
8..31		Reserved	0x220000	Read Only
7		DSP8_INT	na	Read Only
6		DSP7_INT	na	Read Only
5		DSP6_INT	na	Read Only
4		DSP5_INT	na	Read Only
3		DSP4_INT	na	Read Only
2		DSP3_INT	na	Read Only
1		DSP2_INT	na	Read Only
0		DSP1_INT	na	Read Only

Table 15 – 0x000002C – ETH_STAT_VECT_REG

Bit	Name	Description	Default	Access
16..31		ETH2_STATUS_VECTOR	na	Read Only
0..15		ETH1_STATUS_VECTOR	na	Read Only

Table 16 – 0x0000030 – SWITCH_CFG_REG

Bit	Name	Description	Default	Access
16..31		TBD	na	R/W
4..7		SW_VCORE_CFG[3..0]	Na	R/W
1..3		Rerserved	na	R/W
0		SW_RST	na	R/W

Table 17 – 0x000004C – ADC_STATUS

Bit	Name	Description	Default	Access
24..31		FPGA_DIE_TEMP[7..0] (in °C)	na	Read Only
12..23		Rerserved	na	Read Only
0..11		ADC_TEMP_VAL_RAW[11..0]	na	Read Only

5. REFERENCE DOCUMENTATION

- **NAMC-ODSP-M** Technical Reference Manual:
  https://www.nateurope.com/manuals/namc_odsp_m_man_hw.pdf
- **ODSP-M MIF API** Specification:
  Please contact N.A.T.

6. DOCUMENT'S HISTORY

Table 18 – Document's History

Rev	Date	Description	Author
1.0	30.01.2019	initial release	se
	14.03.2019	minor changes	se
	30.06.2021	updated reference documentation	se