NPCIE-UPLINK-O

PCIE UPLINK MODULE

DESIGNED BY N.A.T. GMBH

TECHNICAL REFERENCE MANUAL V1.5

HW REVISION 1.3

N.A.T. Gesellschaft für Netzwerk- und Automatisierungs-Technologie mbH
Konrad-Zuse-Platz 9 | 53227 Bonn, Germany | Phone: +49 228 965 864 - 0
sales@nateurope.com | www.nateurope.com

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. PREFACE

1.1. Disclaimer

The following documentation, compiled by N.A.T. GmbH (henceforth called N.A.T.), represents the current status of the product´s development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. N.A.T. is under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

We must caution you, that this publication could include technical inaccuracies or typographical errors.

N.A.T. offers no warranty, either expressed or implied, for the contents of this documentation or for the product described therein, including but not limited to the warranties of merchantability or the fitness of the product for any specific purpose.

In no event will N.A.T. be liable for any loss of data or for errors in data utilization or processing resulting from the use of this product or the documentation. In particular, N.A.T. will not be responsible for any direct or indirect damages (including lost profits, lost savings, delays or interruptions in the flow of business activities, including but not limited to, special, incidental, consequential, or other similar damages) arising out of the use of or inability to use this product or the associated documentation, even if N.A.T. or any authorized N.A.T. representative has been advised of the possibility of such damages.

The use of registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations (patent laws, trade mark laws, etc.) and therefore free for general use. In no case does N.A.T. guarantee that the information given in this documentation is free of such third-party rights.

Neither this documentation nor any part thereof may be copied, translated, or reduced to any electronic medium or machine form without the prior written consent from N.A.T. GmbH.

This product (and the associated documentation) is governed by the N.A.T. General Conditions and Terms of Delivery and Payment.

Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NPCIe-Uplink-O's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NPCIe-Uplink-O's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NPCIe-Uplink-O** for the first time

Functional Description

Detailed information on the individual devices and the **NPCIe-Uplink-O's** main features

Interfaces

Connector-, switch-, and LED description

Setup Options

Most common setup configurations

Configuration

Options to adapt the **NPCIe-Uplink-O** to personal needs

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NPCIe-Uplink-O** complies to

Document's History

Revision record

Note:

It is assumed, that the **NPCIe-Uplink-O** is handled by qualified personnel only!

2. INTRODUCTION

The **NPCIe-Uplink-O** is a PCIe interface card, which allows establishing two PCIe x8 or one PCIe x16 link between the optical uplink of the **NAT-MCH-PHYS80** and a PCIe-host.

For more information on the **NAT-MCH-PHYS80**, please refer to chapter 7.1 Internal Reference Documentation.

2.1. Basic Functionality

The **NPCIe-Uplink-O** is transparent to the PCIe-host, which means that no special driver is required. It supports SSC isolation and PCIe hot-plug functionality.

2.2. Main Features

Table 1 – Technical Data

Form Factor		
	• PCIe Interface Card • H: 111.15mm • L: 176.6mm	
Processing Resources		
FPGA	• Lattice MachXO2	
Memory	• SPI EEPROM	
Microcontroller	• Atmel ATXmega128	
PCIe-Switch		
	• Broadcom PEX8733	
Front Panel		
	• 2x QSFP-DD interfaces for single x16 or dual x8 uplinks • 4 bicolor LED (Green and Red)	
Compliance		
	• PCI Express Base Specification Rev. 3.0 • PCI Express CEM Specification Rev. 3.0	
Order Codes: NPCIe-Uplink-O – [TRX] – [Cable]		
TRX	- 0	without transceivers
	- 1	1x optical transceiver
	- 2	2x optical transceivers
Cable	- 0	without optical cable
	- 1	with optical cable
Environmental		
Operating Environment	• Default: 0°C to +50 °C (with forced cooling) • Humidity: 10% to 90% at +55°C (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 2g from 36Hz to 2KHz vibration compensation – especially hold-over stability – feasible via customer software) • Shocks: 20g, 11ms, 1⁄2 sine • Altitude: 0 to 5000m • Vibration compensation (especially hold-over stability) via custom software	
Storage Environment	• Default: -40°C to +85°C • Humidity: 5% to 95% (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 3g from 36Hz to 2KHz • Shocks: 30g, 11ms, 1⁄2 sine • Altitude: 0 to 15000m	

3. QUICK START

To ensure proper functioning of the **NPCIe-Uplink-O** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the PCIe edge connector to ensure proper contact when inserting the **NPCIe-Uplink-O** onto the mainboard.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NPCIe-Uplink-O** can be plugged onto any PC mainboard supporting PCIe standards.

Before installing or uninstalling the **NPCIe-Uplink-O**, read the Installation Guide and the User's Manual of the mainboard used.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-plug-capable, if you don't switch off the power.

Ensure that the **NPCIe-Uplink-O** is connected to the mainboard with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-PCIe-Uplink-O** must meet the following specifications:

+12V / 2.0A max.

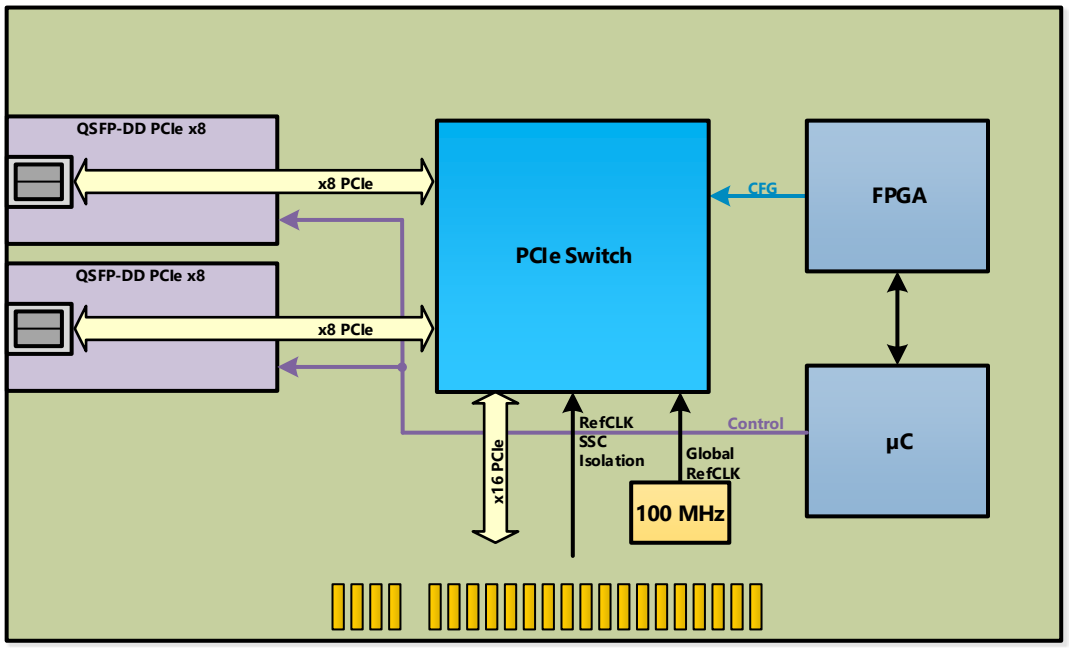
+ 3,3V / 0.5A max.

4. FUNCTIONAL DESCRIPTION

The **NPCIe-Uplink-O** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 1 – Block Diagram



4.1. PCIe Switch

The heart of the **NPCIe-Uplink-O** is a Broadcom PEX8733 PCIe switch. With station 0 ports, it connects to the PCIe host via the edge card connector; station 1 ports are linked to the optical transceivers. It can be configured to use one x16 or two x8 optical uplink(s).

The switch owns a SSC isolation clock input, so it is not mandatory to use a common clock in the whole PCIe hierarchy, even if the host is using a SSC reference clock.

Moreover, the PEX8733 makes a dedicated driver on host side needless, as the required settings can be made via the configuration EEPROM of the switch.

4.2. QSFP-DD Interface

The **NPCIe-Uplink-O** owns two QSFP-DD interfaces. They are connected to the FPGA and controlled by the µC via I^2C.

In combination with suitable transceivers (please refer to the section "Order Codes" in Table 1 – Technical Data), these interfaces provide either two PCIe x8 connections or one PCIe x16 connection.

4.3. Microcontroller

An Atmel ATxmega128 Microcontroller is located on the **NPCIe-Uplink-O** for I^2C communication. Basic function of this device is to configure and reset the PCIe switch and the BOA transceivers. It contains high-level functionality needed for board management, control-uplink to the MTCA system, and usage of PCIe hot-plug mechanism.

4.4. FPGA

The **NPCIe-Uplink-O** features a Lattice MachX02 FPGA as hardware extension of the on-board microcontroller.

Moreover, it handles PCIe side band signals coming from the edge connector and hot-plugging functionality for the attached MTCA system.

4.5. Advanced Functionality

Compared to "less-intelligent" PCIe uplink cards, this new design offers the following advantages:

- PCIe Gen3 x16 support
- SSC Isolation (host machine could run SSC, MTCA system not)
- PCIe Hot-Plug support (MTCA system can be started after host machine)
- Dual x8 operation towards two MTCA systems

5. INTERFACES

5.1. Front Panel and LEDs

The **NPCIe-Uplink-O** module is equipped with 4 bi-coloured LEDs. The function is described in the table below.

Note: the labelling is just for clarification, the board itself will not be labelled.

Figure 2 – Front Panel

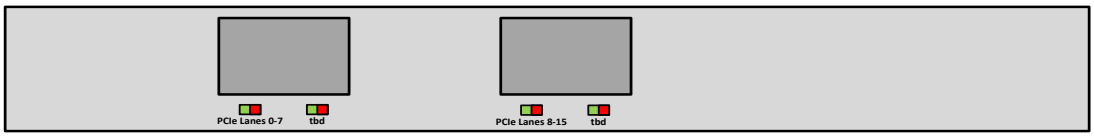
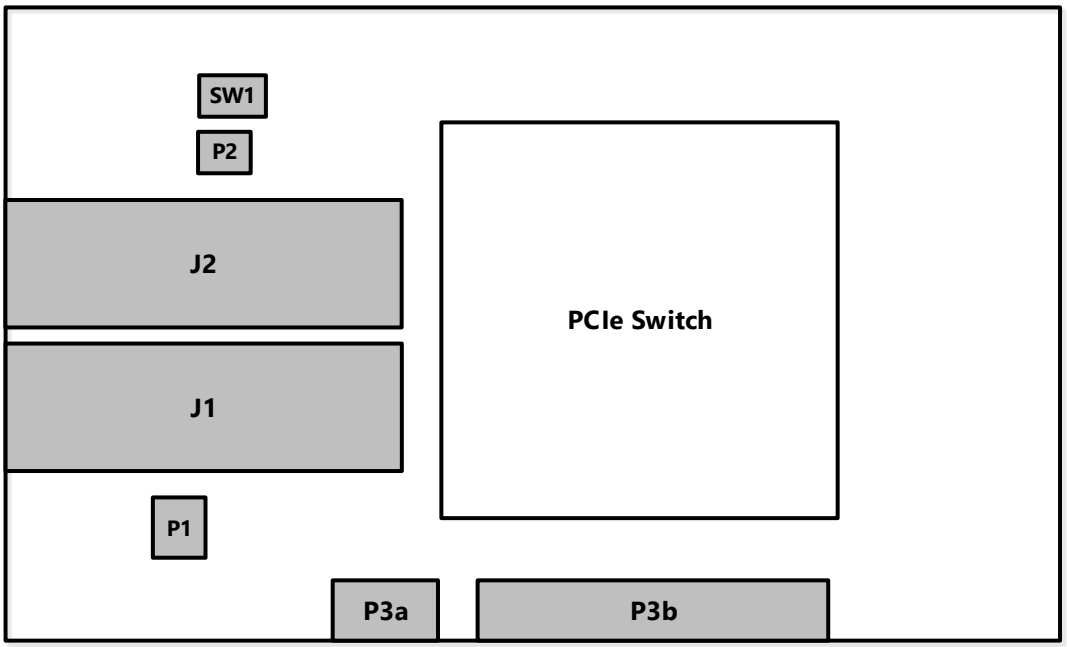


Table 2 – LED Functionality

LED	Colour	Function
PCIe Lanes 0-7	green slow blink	PCIe-GEN1-Link established
	green fast flash	PCIe-GEN2-Link established
	green solid ON	PCIe-GEN3-Link established
	red solid ON	no link
	OFF	no physical connection, or port not assembled
tbd	green / red	tbd
PCIe Lanes 8-15	green slow blink	PCIe-GEN1-Link established
	green fast flash	PCIe-GEN2-Link established
	green solid ON	PCIe-GEN3-Link established
	red solid ON	no link
	OFF	no physical connection, or port not assembled
tbd	green / red	tbd

5.2. Component-, Connector-, and Switch-Location

Figure 3 – Location Diagram



Please refer to the following tables to look up the connector pin assignment of the **NPCIe-Uplink-O**.

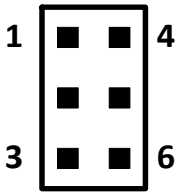
5.2.1. J5/6: QSFP-DD Interfaces

J5 and J6 are QSFP-DD cages, which can be populated with a suitable transceiver (separate order item).

5.2.2. P1: Microcontroller Programming Header

Connector P1 connects to the programming port of the Atmel ATxMega128 microcontroller.

Figure 4 – J1: Microcontroller Programming Header



Pin #	Signal	Signal	Pin #
1	PDI_DATA	3V3	2
3	DEBUG_RXD	DEBUG_TXD	4
5	PDI_CLK	GND	6

5.2.3. P2: FPGA Programming Header

Connector P2 offers a JTAG connection to the programming-port of the Lattice MachX02 FPGA.

Figure 5 – J4: FPGA Programming Header

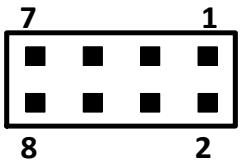


Table 3 – P2: FPGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	3V3	FPGA_TDO	2
3	FPGA_TDI	nc	4
5	FPGA_JTAGENB	FGPA_TMS	6
7	GND	FPGA_TCK	8

5.2.4. P3: PCIex16 Board Connector

Figure 6 – P3: PCIex16 Board Connector (top view)

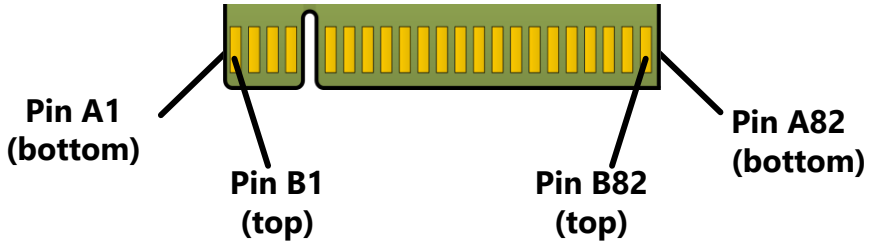


Table 4 – S1: AMC-Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
B1	12V	PCIE_PRSNT	A1
B2	12V	12V	A2
B3	12V	12V	A3
B4	GND	GND	A4
B5	PCIE_SMCLK	nc	A5
B6	PCIE_SMDAT	nc	A6
B7	GND	nc	A7
B8	nc	nc	A8
B9	FPGA_TRST#	nc	A9
B10	3V3AUX	nc	A10
B11	nc	PEX_PERST#	A11
B12	nc	GND	A12
B13	GND	PCIE_REFCLK_P	A13
B14	PCIe_TX_0_P	PCIE_REFCLK_N	A14
B15	PCIe_TX_0_N	GND	A15
B16	GND	PCIe_RX_0_P	A16
B17	PCIE_PRSNT	PCIe_RX_0_N	A17
B18	GND	GND	A18
B19	PCIe_TX_1_P	GND	A19
B20	PCIe_TX_1_N	GND	A20
B21	GND	PCIe_RX_1_P	A21
B22	GND	PCIe_RX_1_N	A22
B23	PCIe_TX_2_P	GND	A23
B24	PCIe_TX_2_N	GND	A24
B25	GND	PCIe_RX_2_P	A25
B26	GND	PCIe_RX_2_N	A26
B27	PCIe_TX_3_P	GND	A27
B28	PCIe_TX_3_N	GND	A28
B29	GND	PCIe_RX_3_P	A29
B30	nc	PCIe_RX_3_N	A30

Pin #	Signal	Signal	Pin #
B31	PCIE_PRSNT	GND	A31
B32	GND	nc	A32
B33	PCIe_TX_4_P	GND	A33
B34	PCIe_TX_4_N	GND	A34
B35	GND	PCIe_RX_4_P	A35
B36	GND	PCIe_RX_4_N	A36
B37	PCIe_TX_5_P	GND	A37
B38	PCIe_TX_5_N	GND	A38
B39	GND	PCIe_RX_5_P	A39
B40	GND	PCIe_RX_5_N	A40
B41	PCIe_TX_6_P	GND	A41
B42	PCIe_TX_6_N	GND	A42
B43	GND	PCIe_RX_6_P	A43
B44	GND	PCIe_RX_6_N	A44
B45	PCIe_TX_7_P	GND	A45
B46	PCIe_TX_7_N	GND	A46
B47	GND	PCIe_RX_7_P	A47
B48	PCIE_PRSNT	PCIe_RX_7_N	A48
B49	GND	GND	A49
B50	PCIe_TX_8_P	nc	A50
B51	PCIe_TX_8_N	GND	A51
B52	GND	PCIe_RX_8_P	A52
B53	GND	PCIe_RX_8_N	A53
B54	PCIe_TX_9_P	GND	A54
B55	PCIe_TX_9_N	GND	A55
B56	GND	PCIe_RX_9_P	A56
B57	GND	PCIe_RX_9_N	A57
B58	PCIe_TX_10_P	GND	A58
B59	PCIe_TX_10_N	GND	A59
B60	GND	PCIe_RX_10_P	A60
B61	GND	PCIe_RX_10_N	A61
B62	PCIe_TX_11_P	GND	A62
B63	PCIe_TX_11_N	GND	A63
B64	GND	PCIe_RX_11_P	A64
B65	GND	PCIe_RX_11_N	A65
B66	PCIe_TX_12_P	GND	A66
B67	PCIe_TX_12_N	GND	A67
B68	GND	PCIe_RX_12_P	A68
B69	GND	PCIe_RX_12_N	A69
B70	PCIe_TX_13_P	nc	A70
B71	PCIe_TX_13_N	nc	A71
B72	GND	PCIe_RX_13_P	A72
B73	GND	PCIe_RX_13_N	A73
B74	PCIe_TX_14_P	GND	A74
B75	PCIe_TX_14_N	GND	A75
B76	GND	PCIe_RX_14_P	A76
B77	GND	PCIe_RX_14_N	A77

Pin #	Signal	Signal	Pin #
B78	PCIe_TX_15_P	GND	A78
B79	PCIe_TX_15_N	GND	A79
B80	GND	PCIe_RX_15_P	A80
B81	PCIE_PRSNT	PCIe_RX_15_N	A81
B82	GND	GND	A82

Note: Naming of the signals differs from schematics' signal names. Signals with index *'TX'* refer to incoming signals from PCIe host (PC), signals associated with *'RX'* indicate outgoing signals from the **NPCIe-Uplink-O** to the PCIe host.

5.2.5. SW1: Multipurpose DIP-Switch

The tables below provide information on the operating parameters and configuration options of SW1.

Figure 7 – SW1: Multipurpose Dip-Switch

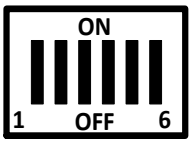


Table 5 – SW1 – Operating Parameters

Switch #	Function
SW1-1	Tbd
SW1-2	Tbd
SW1-3	Tbd
SW1-4	Tbd
SW1-5	Tbd
SW1-6	Tbd

Table 6 – DIP SW1 – Configuration

Switch #	ON	OFF
SW1-1	Tbd	***Tbd***
SW1-2	Tbd	***Tbd***
SW1-3	Tbd	***Tbd***
SW1-4	Tbd	***Tbd***
SW1-5	Tbd	***Tbd***
SW1-6	Tbd	***Tbd***

Note: Default configuration is labelled with ***bold, italic letters***.

6. CONFIGURATION

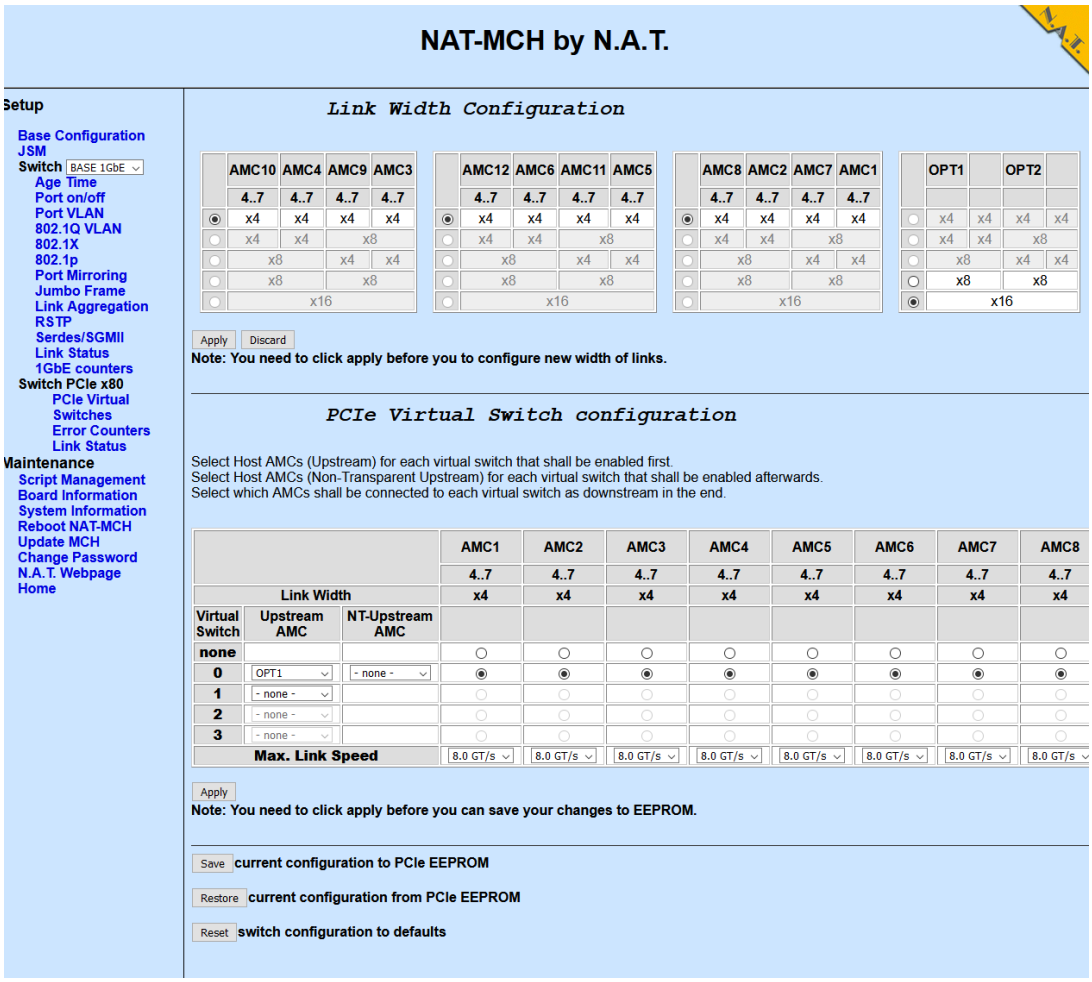
For basic configuration **NAT-MCH** firmware 2.21.9 or higher is required, as well as **NAT-MCH-HUB-PCIex80** AVR 1.10 or higher, and FPGA V1.3 or higher.

6.1. Basic Configuration

Once connected to the **NAT-MCH-PHYS80**, the **NPCIe-Uplink-O** can be configured by web interface.

- Choose '`Switch PCIe x80 → PCIe Virtual Switches`' to see the following matrix:

Figure 8 – Configuration via Web Interface



- Choose '`Width configuration (x16 or x8/x8)`' according to your Uplink board

- Click ‘Apply’
- Set ‘Opt1’ as your Upstream port in ‘Pcie Virtual Switch Configuration’ below
- Click ‘Apply’
- Click ‘Save’ to store current configuration in EEPROM

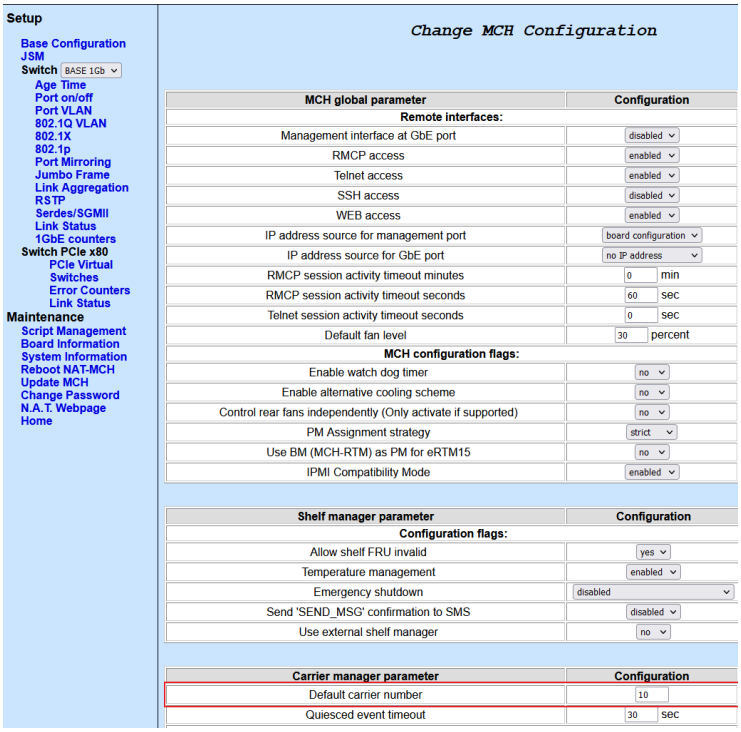
6.2. Mapping between PCIe-Devices and NAT-MCH-PHYS80

If a **NPCIe-UPLINK-O** is connected to two **NAT-MCH-PHYS80** modules, it is mandatory to identify, which PCIe device is mapped to which **NAT-MCH-PHYS80**.

Please note: the following configuration option is only available with **NAT-MCH-PHYS80** FW 2.22.5 and higher!

As shown in the figure below, a Default Carrier Number (>1 and <16) can be chosen. Save and reboot afterwards.

Figure 9 – Default Carrier Number Configuration



After reboot, enter the PCIe Virtual Switch Configuration via the web interface. By clicking the ‘Save’ button, the information is written into the EEPROM of the x80 PCIe switch on the **NAT-MCH-PHYS80**.

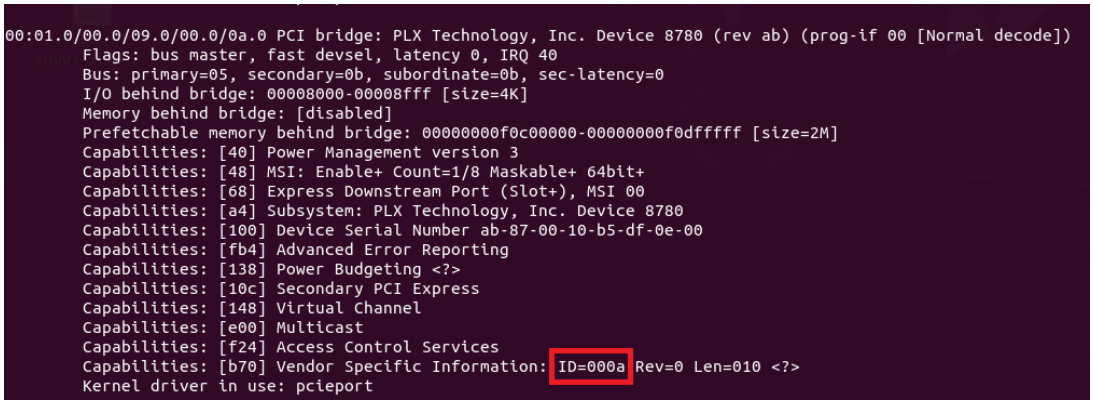
Now the Carrier Number can be found in the capabilities of the appropriate PCIe device on the **NPCIe-UPLINK-O**.

With Linux, all PCIe devices can be listed with the command:

`'sudo lspci -P -v'`

The entry `'Vendor Specific Information'` shows the Carrier Number ID as highlighted in the screenshot below.

Figure 10 – Carrier Number in PCIe Device Capabilities



7. SPECIFICATIONS AND COMPLIANCES

7.1. Internal Reference Documentation

- **NPCIe-Uplink-O**
  Please find the latest versions of all documents on our product website by clicking on the "Collaterals"-Button.

7.2. External Reference Documentation

- Atmel ATxmega128 Microcontroller Data Sheet, Rev.A, 08/2018
- Broadcom PEX8733 PCIe Switch Product Brief, V1.0, 08/2011
- Lattice MachX02 FPGA Data Sheet DS1035 3.3, 03/2017

7.3. Standards Compliance

- PCI Express Base Specification Rev. 3.0
- PCI Express CEM Specification Rev. 3.0

7.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.7. Product Safety

The board complies with EN60950 and UL1950.

7.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7.9. Abbreviation List

Table 7 – Abbreviation List

Abbreviation	Description
CFG	Configuration
EEPROM	Electrically Erasable PROM
FPGA	Field Programmable Gate Array
HP	Hot Plug
I^2C	Inter-Integrated Circuit
LVDS	Low Voltage Differential Signaling
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
MPO24	Multiple-Fiber Push-On/Pull-off - Optical Fiber Connector
PCI(e)	Peripheral Component Interconnect (Express)
SSC	Spread Spectrum Clock

8. DOCUMENT'S HISTORY

Table 8 – Document's History

Rev	Date	Description	Author
1.0	05.03.2019	• initial release	se
	26.03.2019	• Added cable recommendation information	se
1.1	02.06.2020	• Correction of Connector Assignment P3 • Typo correction / Minor changes • Added assembly option (1 or 2 BOAs) • Added chapter 6 – Setup Options	se
1.2	18.02.2021	• Updated Table 1 – Technical Data	se
	08.06.2021	• Updated Table 2 – LED Functionality • Added chapter 6 Configuration • Updated chapter 7.1 Internal Reference Documentation	se
1.3	18.11.2021	• Updated chapter Setup Options • Reorganized and updated chapter 6 Configuration and added information about PCIe Device Mapping	se
1.4	29.03.2022	• Updated chapter 1.2 About This Document • Renamed chapter 5 Interfaces • Updated chapter Setup Options	Se
1.5	28.04.2025	• Updated to latest HW-Version; change from BOA to QSFP-DD interface	se