NAT-MCH-PCIEX80

NAT-MCH-HUB-MODULE

DESIGNED BY N.A.T. GMBH

TECHNICAL REFERENCE MANUAL V1.1

HW REVISION 1.3

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1. PREFACE

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-MCH-PCIex80's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-MCH-PCIex80's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-MCH-PCIex80** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-MCH-PCIex80's** main features

Hardware

Information about LEDs, connectors, and port assignments

Setup Options

Most common setup configurations

Configuration

Options to adapt the **NAT-MCH-PCIex80** to personal needs

Firmware Update

Description of the firmware update procedure

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-MCH-PCIex80** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-MCH-PCIex80** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-MCH-PCIex80** is a double-width HUB-module applicable for the double-width **NAT-MCH-M4**. Together with the **NAT-MCH-CLK-PHYS**, these modules merge into the **NAT-MCH-PHYS80**.

2.1. Basic Functionality

The **NAT-MCH-PCIex80** provides an 80-port PCIe Gen3 switch that allows each of the 12 AMCs in a MTCA.4.x system to be connected by an x4 link. An optional **NAT-MCH-RTM** (via **NAT-MCH** base board) is connected by an x16 link.

The **NAT-MCH-PHYS80** offers two x8 optical uplinks via QSFP-DD, which can be combined to one x16 uplink. The **NPCIe-Uplink-O** as counterpart allows establishing links between the optical uplink of the **NAT-MCH-PHYS80** and a PCIe-host.

The PCIe switch also accommodates higher bandwidths, i.e. x8 or x16 to a reduced number of AMC slots if the backplane provides appropriate connectivity.

Finally, the PCIe switch provides the ability to establish up to four virtual PCIe clusters and assign the AMC slots to these. The up to four PCIe Root Complexes can be any of the AMC-CPUs, the **NAT-MCH-RTM** CPU or an external PC.

The **NAT-MCH-PCIex80** supports full non-transparent bridging functionality to allow implementation of multi-host systems, and intelligent I/O modules.

2.2. Applications

Any applications with demands on scalable high bandwidth and non-blocking interconnection, including servers, storage, video streaming, blade servers, and embedded control products.

Especially in combination with the **NAT-MCH-PHYS80**, the **NAT-MCH-PCIex80** is highly suitable for physics applications e.g., particle accelerators, synchrotron experiments, colliding beam accelerators, neutrino oscillation, plasma control, and fusion research.

2.3. Main Features

Table 1 – Technical Data

Form Factor		
	• Double-width, full-size HUB module • Width: 148 mm, Depth: <180.6 mm	
Compatible MCH		
	• **NAT-MCH-M4** (as base board for **NAT-MCH-PHYS80**)	
On-Board Resources		
FPGA	• Lattice MachXO2 FPGA	
Microcontroller	• Atmel ATmega1284P	
PCIe Switch	• PLX PEX8780	
Front Panel Uplink		
	• Two PCIe x8 / one PCIe x16 optical front uplinks	
LEDs		
Indicator LEDs	• 12 LEDs for Ethernet status and activity of 12 AMC slots • 3 bi-colored LEDs for Ethernet status and activity of 3 optical uplinks • 1 bi-colored LED for Ethernet status and activity of downlink to CPU on **NAT-MCH-BASE**	
Backplane Interconnect		
AMC-Interconnection	• Gen3 x1 and x4 to each AMC via Fabric D-G ***or*** • Gen3 x8 and x16 switching functionality to reduced number of AMCs (not supported by standard backplanes)	
RTM via NAT-MCH	• Gen3 x16 link	
Clock		
	• 100 MHz PCIe compliant clock signal from **NAT-MCH-CLK** / **-CLK-PHYS** • PCIe clock can be provided as FCLKA to AMCs	
Compliance		
	• PCI Express Base Specification Rev. 1.1 • PICMG µTCA.0 Rev. 1.0 • PICMG AMC.0 Rev. 2.0 • PICMG AMC.1 Rev. 1.0 • PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) • IPMI Specification v2.0 Rev. 1.0 • RoHS	
Order Codes NAT-MCH-PCIex80 – [TRX] – [Cable]		
TRX	- 0	without transceivers
	- 1	1x optical transceiver
	- 2	2x optical transceivers
Cable	- 0	without optical cable
	- 1	with optical cable
Environmental		
Operating Environment	• default: 0 to +50 degrees Celsius • Humidity: 10% to 90% (non-condensing)	
Storage Environment	• default: -40 to +85 degrees Celsius • Humidity: 10% to 90% (non-condensing)	

3. QUICK START

As the **NAT-MCH-PCIex80** is only available mounted on a **NAT-MCH-M4** baseboard, please refer to the according manual for information about quick start, unpacking, mechanical and electrical requirements.

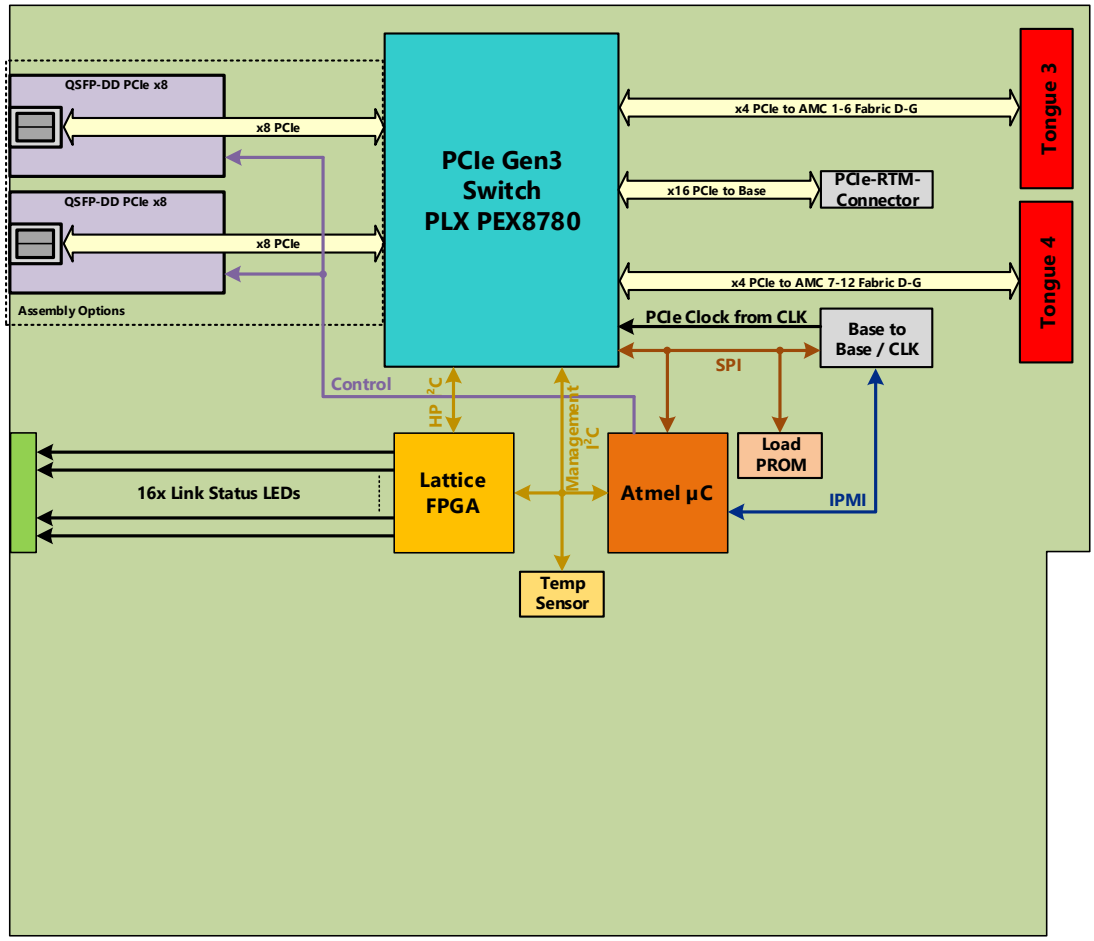
References are given in chapter 8.1 Internal Reference Documentation.

4. FUNCTIONAL DESCRIPTION

The **NAT-MCH-PCIex80** can be divided into a number of functional blocks, which are described in the following paragraphs.

The figure below gives an overview on the functional blocks.

Figure 1 – Block Diagram NAT-MCH-PCIex80



4.1. PCIe Switch PLX8780

The **NAT-MCH-PCIex80** is equipped with a PLX PEX8780 PCI Express switch, which supports up to 20 ports (depending on configuration), per default with 4 lanes (PCIe x4) towards the AMC slots, and 16 lanes (PCIe x16) towards the RTM and the Uplink port (assembly option).

If supported by the backplane, the **NAT-MCH-PCIex80** can offer even a higher bandwidth (x8 or x16) to a reduced number of AMCs. For the port assignment, please refer to chapter 5.3 Port Assignment.

The PLX PEX8780 supports non-blocking switching at full line rate. Quality of Service (QoS) is provided by the PEX8780, supporting 2 virtual cannels and 8 traffic classes per port. Every switch port can be configured as upstream port.

The PCIe Switch can be configured by strapping pins, by loading an EEPROM, or by PCIe messages from a host.

A standard configuration is done by the microprocessor and resistors by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.

These standard settings can be changed by reading the EEPROM after a reset or by receiving PCIe messages from a host.

The EEPROM contains basic configuration information for the PCIe switch as well as user settings e.g., upstream port settings. The user settings can be changed by the CPU on the **NAT-MCH BASE** module.

The /PERST pin is also connected to the microcontroller. The value of this pin can also be controlled by programming a register in the microcontroller.

4.2. QSFP-DD Interfaces

The **NPCIe-Uplink-O** owns two QSFP-DD interfaces. They are connected to the FPGA and controlled by the µC via I^2C.

In combination with suitable transceivers, these interfaces provide either two PCIe x8 connections or one PCIe x16 connection.

4.3. Microcontroller

For configuration of the PCIe switch and hot-swap functionality, an 8-bit Atmel ATmega1284P microcontroller resides on the **NAT-MCH-PCIex80**. The µC can be updated by the CPU on the **NAT-MCH BASE** module via SPI interface. Normal communication between the CPU and the µC is done by IPMI messages over the I^2C interface.

The strapping options and the reset signal of the switch can be controlled by programming registers in the microcontroller. Also, the PCIe Hot-Plug signals can be served by the µC.

Furthermore, three temperature sensors are connected to a second I^2C bus of the microcontroller, which makes these sensors accessible to the CPU on the **NAT-MCH BASE** module via IPMI.

4.4. FPGA

The Lattice MachXO2 FPGA is used to emulate a set of I^2C port expanders that the PLX switch normally uses to extend its pins for PCIe Hotplug support on all ports. The FPGA implements

an I^2C interface towards the PLX switch and behaves as if there were 12 I^2C port expenders connected.

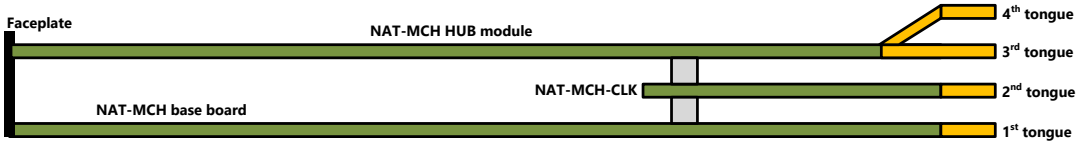
Moreover, it implements a second interface towards the Atmel µC, so that the Hotplug signals finally can be exchanged with the **NAT-MCH-M4** main firmware.

4.5. Interface to Mezzanines

The **NAT-MCH-PCIex80** interfaces with the **NAT-MCH-CLK** module, the **NAT-MCH-CLK-PHYS** module, or a **NAT-MCH-CLK** spacer, which on its part is connected to the **NAT-MCH-M4** baseboard.

The arrangement of the mezzanines is shown in the figure below.

Figure 2 – Arrangement of Mezzanine Modules



The Microcontroller on the **NAT-MCH-PCIex80** can be updated by the CPU on the **NAT-MCH-M4** module via SPI interface. Normal communication between Microprocessor and CPU is done by IPMI messages via I^2C interface.

A configuration EEPROM for the PCIe Switch resides on the **NAT-MCH-PCIex80**. This EEPROM can be programmed / updated by the CPU of the **NAT-MCH-M4** module via SPI interface.

A 100 MHz PCIe compliant clock signal from the **NAT-MCH CLK** module can be used by the **NAT-MCH-PCIex80**. The PCIe clock can be provided as Fabric Clock (FCLKA) to the AMC slots.

5. HARDWARE

5.1. Front Panel and LEDs

The **NAT-MCH-PCIex80** is equipped with various LEDs described in the following sections.

Figure 3 – NAT-MCH-PCIex80: Front Panel

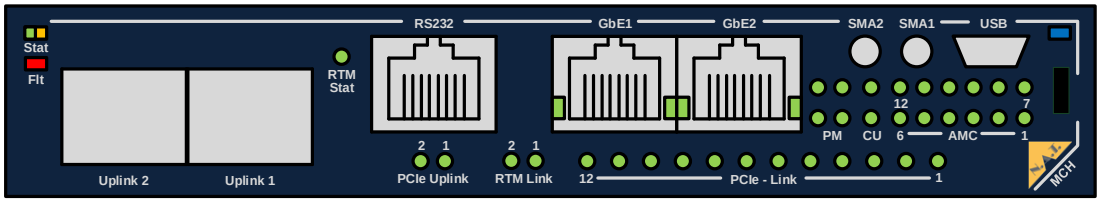


Table 2 – LED Functionality

LED	Color	Function
12x PCIe-Link-Status of AMC 1-12	OFF	no link established
	Green slow blink	PCIe Gen1 Link (2.5 GBaud)
	Green fast flash	PCIe Gen2 Link (5 GBaud)
	Green solid ON	PCIe Gen3 Link (8 GBaud)
RTM-Link 1	OFF	no link established
	Green slow blink	PCIe Gen1 Link (2.5 GBaud)
	Green fast flash	PCIe Gen2 Link (5 GBaud)
	Green solid ON	PCIe Gen3 Link (8 GBaud)
Optical Uplink 1/2	OFF	no link established
	Green slow blink	PCIe Gen1 Link (2.5 GBaud)
	Green fast flash	PCIe Gen2 Link (5 GBaud)
	Green solid ON	PCIe Gen3 Link (8 GBaud)

Note:

- LED for Optical Uplink 2 is used only in case the upstream port is set up as two x8 links
- LED for RTM Link 2 is tbd

5.2. Connector- and Switch-Location

Figure 4 – Location Diagram – Top

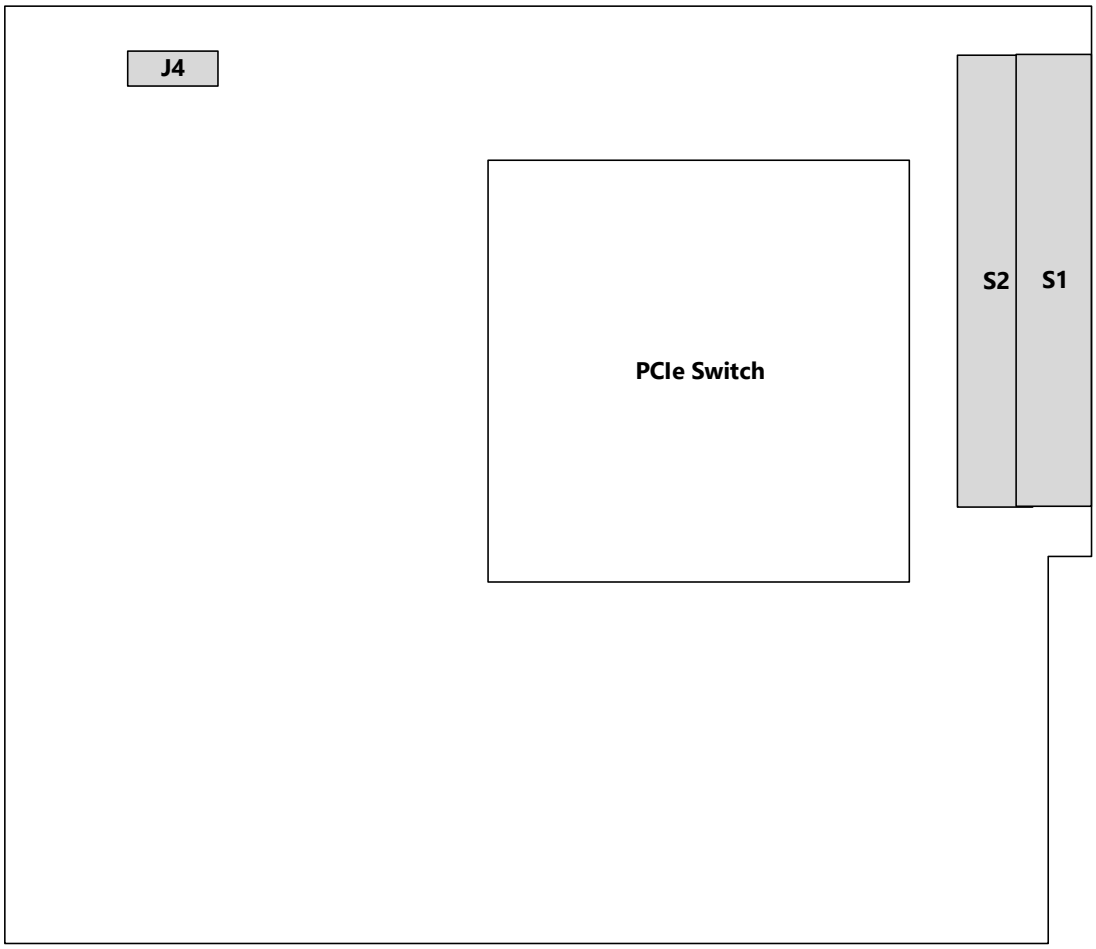
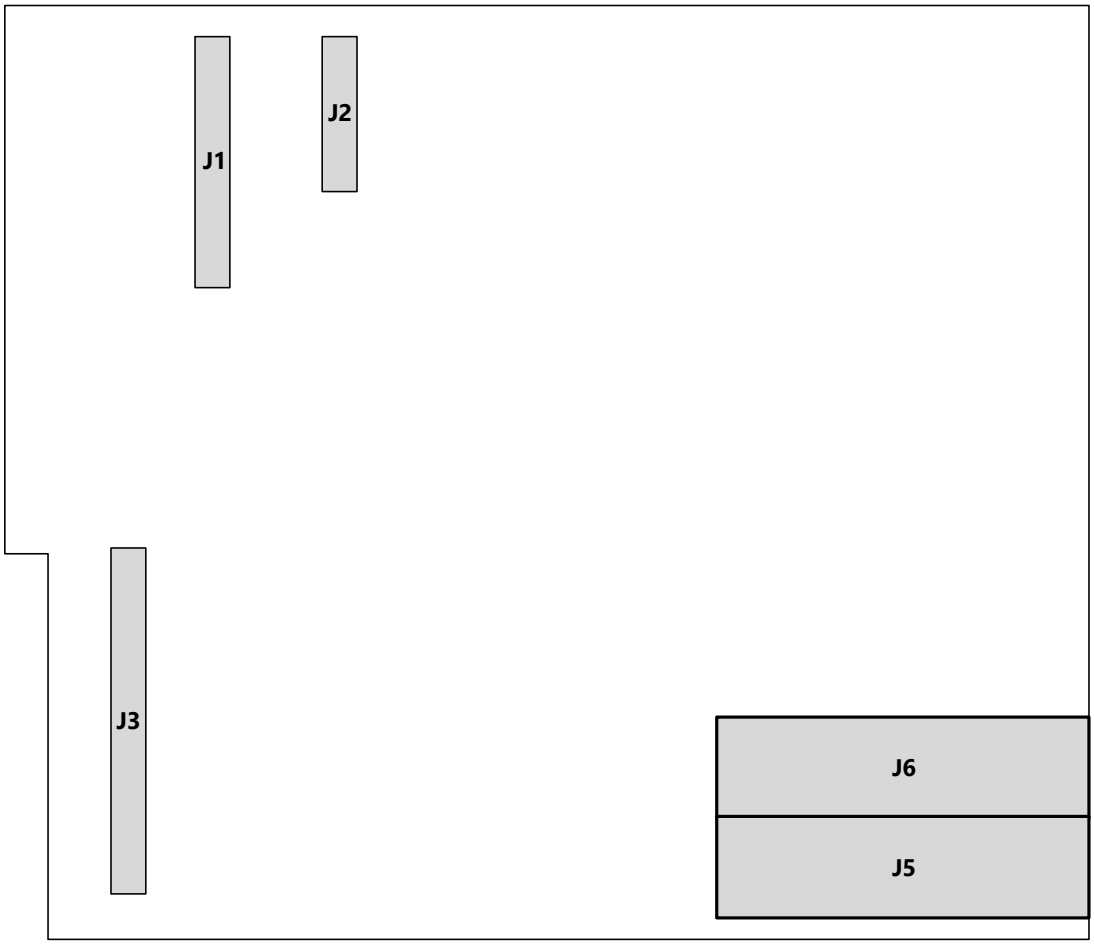


Figure 5 – Location Diagram – Bottom



Please refer to the following tables to look up the connector pin assignment of the **NAT-MCH-PCIex80**.

5.2.1. S1: MCH Edge Connector (3rd Tongue)

The **NAT-MCH-PCIex80** connects to the 3rd tongue of the backplane via S1.

Figure 6 – S1: MCH Edge Connector (3rd Tongue)

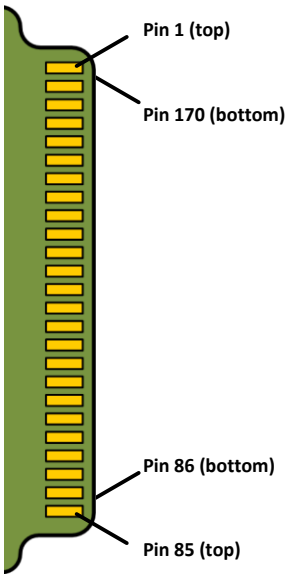


Table 3 – S1: MCH Edge Connector (3rd Tongue) – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149

Pin #	Signal	Signal	Pin #
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100

Pin #	Signal	Signal	Pin #
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

5.2.2. S2: MCH Edge Connector (4th Tongue)

The **NAT-MCH-PCIex80** connects to the 4th tongue of the backplane via S2.

Figure 7 – S2: MCH Edge Connector (4th Tongue)

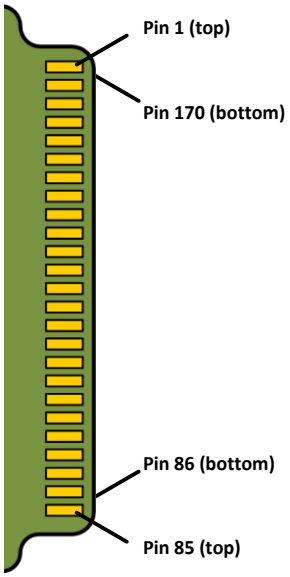


Table 4 – S2: MCH Edge Connector (4th Tongue)

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126
46	GND	GND	125
47	TxFG9+	RxFG9+	124

Pin #	Signal	Signal	Pin #
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

5.2.3. J1: Connector to 1st/2nd PCB

Via J1, the **NAT-MCH-PCIex80** connects to the **NAT-MCH-CLK** module, from where the signals are routed to the **NAT-MCH-M4**.

Figure 8 – J1: Connector to 1st/2nd PCB

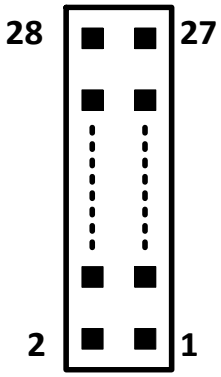


Table 5 – J1: Connector to 1st/2nd PCB – Pin Assignment

Pin #	Signal	Signal	Pin #
1	INT1	INT2	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_HUB_P	NC	14
15	PCIeCLK_HUB_N	SPICLK	16
17	GND	NC	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	NC	24
25	SDA	/RESET_HUBPCB	26
27	GND	GND	28

5.2.4. J2: PCIe Reference Clock Connector

The PCIe Reference Clock from the **NAT-MCH-CLK** / **-CLK-PHYS** module is routed via J2 to the **NAT-MCH-PCIex80** HUB module.

Figure 9 – J2: PCIe Reference Clock Connector

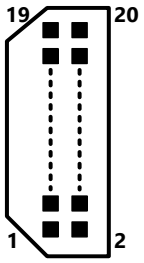


Table 6 – J2: PCIe Reference Clock Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	nc	nc	2
3	nc	RxCLK_N	4
5	nc	RxCLK_P	6
7	nc	nc	8
9	nc	nc	10
11	nc	nc	12
13	nc	TxCLK_N	14
15	nc	TxCLK_P	16
17	nc	nc	18
19	nc	nc	20

5.2.5. J3: RTM-PCIe Connector

Connector J3 connects to the **NAT-MCH-M4**, which routes the PCIe-Lanes towards an optional **NAT-MCH-RTM**.

Figure 10 – J3: RTM-PCIe Connector

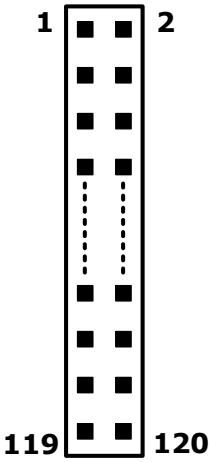


Table 7 – J3: RTM-PCIe Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	2
3	UpLNK_ETH0-Tx_P	UpLNK_ETH0-Rx_P	4
5	UpLNK_ETH0-Tx_N	UpLNK_ETH0-Rx_N	6
7	GND	GND	8
9	UpLNK_ETH1-Tx_P	UpLNK_ETH1-Rx_P	10
11	UpLNK_ETH1-Tx_N	UpLNK_ETH1-Rx_N	12
13	GND	GND	14
15	RTM_CONo	RTM_CON1	16
17	GND	GND	18
19	RTM_CLK1_P	RTM_CLK0_P	20
21	RTM_CLK1_N	RTM_CLK0_N	22
23	GND	GND	24
25	RTM_PCIe00-Tx_P	RTM_PCIe00-Rx_P	26
27	RTM_PCIe00-Tx_N	RTM_PCIe00-Rx_N	28
29	GND	GND	30
31	RTM_PCIe01-Tx_P	RTM_PCIe01-Rx_P	32
33	RTM_PCIe01-Tx_N	RTM_PCIe01-Rx_N	34
35	GND	GND	36
37	RTM_PCIe02-Tx_P	RTM_PCIe02-Rx_P	38
39	RTM_PCIe02-Tx_N	RTM_PCIe02-Rx_N	40
41	GND	GND	42
43	RTM_PCIe03-Tx_P	RTM_PCIe05-Rx_P	44
45	RTM_PCIe03-Tx_N	RTM_PCIe05-Rx_N	46
47	GND	GND	48

Pin #	Signal	Signal	Pin #
49	RTM_PCIe03-Rx_P	RTM_PCIe06-Rx_P	50
51	RTM_PCIe03-Rx_N	RTM_PCIe06-Rx_N	52
53	GND	GND	54
55	RTM_PCIe04-Rx_P	RTM_PCIe07-Rx_P	56
57	RTM_PCIe04-Rx_N	RTM_PCIe07-Rx_N	58
59	GND	GND	60
61	RTM_PCIe04-Tx_P	RTM_PCIe06-Tx_P	62
63	RTM_PCIe04-Tx_N	RTM_PCIe06-Tx_N	64
65	GND	GND	66
67	RTM_PCIe05-Tx_P	RTM_PCIe07-Tx_P	68
69	RTM_PCIe05-Tx_N	RTM_PCIe07-Tx_N	70
71	GND	GND	72
73	RTM_PCIe08-Rx_P	RTM_PCIe09-Rx_P	74
75	RTM_PCIe08-Rx_N	RTM_PCIe09-Rx_N	76
77	GND	GND	78
79	RTM_PCIe10-Rx_P	RTM_PCIe11-Rx_P	80
81	RTM_PCIe10-Rx_N	RTM_PCIe11-Rx_N	82
83	GND	GND	84
85	RTM_PCIe08-Tx_P	RTM_PCIe12-Rx_P	86
87	RTM_PCIe08-Tx_N	RTM_PCIe12-Rx_N	88
89	GND	GND	90
91	RTM_PCIe09-Tx_P	RTM_PCIe13-Rx_P	92
93	RTM_PCIe09-Tx_N	RTM_PCIe13-Rx_N	94
95	GND	GND	96
97	RTM_PCIe10-Tx_P	RTM_PCIe14-Rx_P	98
99	RTM_PCIe10-Tx_N	RTM_PCIe14-Rx_N	100
101	GND	GND	102
103	RTM_PCIe11-Tx_P	RTM_PCIe15-Rx_P	104
105	RTM_PCIe11-Tx_N	RTM_PCIe15-Rx_N	106
107	GND	GND	108
109	RTM_PCIe12-Tx_P	RTM_PCIe14-Tx_P	110
111	RTM_PCIe12-Tx_N	RTM_PCIe14-Tx_N	112
113	GND	GND	114
115	RTM_PCIe13-Tx_P	RTM_PCIe15-Tx_P	116
117	RTM_PCIe13-Tx_N	RTM_PCIe15-Tx_N	118
119	GND	GND	120

5.2.6. J4: FPGA Programming Header

J4 is a programming header for the Lattice MachXO2 FPGA

Figure 11 – J4: FPGA Programming Header

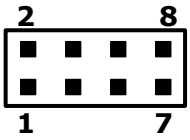


Table 8 – J4: FPGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	+3.3V	FPGA_TDO	2
3	FPGA_TDI	nc	4
5	FPGA_JTAGENB	FPGA_TMS	6
7	GND	FPGA_TCK	8

5.2.7. J5/6: QSFP-DD Interfaces

J5 and J6 are QSFP-DD cages, which can be populated with a suitable transceiver (separate order item).

5.3. Port Assignment

A certain switch port is not constrained to the according AMC port or MCH fabric. The following table shows the standard configuration:

Switch ports to AMC slots: PCIe x4-Link
Switch ports to Uplink ports: PCIe x16-Link

Table 9 – PCIe Switch Lane to MCH Fabric / AMC Port Mapping

Switch Lanes	Switch Port	MCH Fabric	AMC Slot # / Uplink
0	0	G-10	10
1		F-10	
2		E-10	
3		D-10	
4	1	G-4	4
5		F-4	
6		E-4	
7		D-4	
8	2	G-9	9
9		F-9	
10		E-9	
11		D-9	
12	3	G-3	3
13		F-3	
14		E-3	
15		D-3	
16	4	G-12	12
17		F-12	
18		E-12	
19		D-12	
20	5	G-6	6
21		F-6	
22		E-6	
23		D-6	
24	6	G-11	11
25		F-11	
26		E-11	
27		D-11	
28	7	G-5	5
29		F-5	
30		E-5	
31		D-5	
32	8	G-8	8
33		F-8	
34		E-8	
35		D-8	
36	9	G-2	2

Switch Lanes	Switch Port		MCH Fabric	AMC Slot # / Uplink	
37			F-2		
38			E-2		
39			D-2		
40	10		G-7	7	
41			F-7		
42			E-7		
43			D-7		
44	11		G-1	1	
45			F-1		
46			E-1		
47			D-1		
48	12		RTM-15	Uplink via RTM	
49			RTM-14		
50			RTM-13		
51			RTM-12		
52			RTM-11		
53			RTM-10		
54			RTM-9		
55			RTM-8		
56			RTM-7		
57			RTM-6		
58			RTM-5		
59			RTM-4		
60			RTM-3		
61			RTM-2		
62			RTM-1		
63			RTM-0		
64	16	16	UpLNK1-0	Front Uplink1	Front Uplink1
65			UpLNK1-1		
66			UpLNK1-2		
67			UpLNK1-3		
68			UpLNK1-4		
69			UpLNK1-5		
70			UpLNK1-6		
71			UpLNK1-7		
72		17	UpLNK1-8 / UpLNK2-0		Front Uplink2
73			UpLNK1-9 / UpLNK2-1		
74			UpLNK1-10 / UpLNK2-2		
75			UpLNK1-11 / UpLNK2-3		
76			UpLNK1-12 / UpLNK2-4		
77			UpLNK1-13 / UpLNK2-5		
78			UpLNK1-14 / UpLNK2-6		
79			UpLNK1-15 / UpLNK2-7		

6. CONFIGURATION

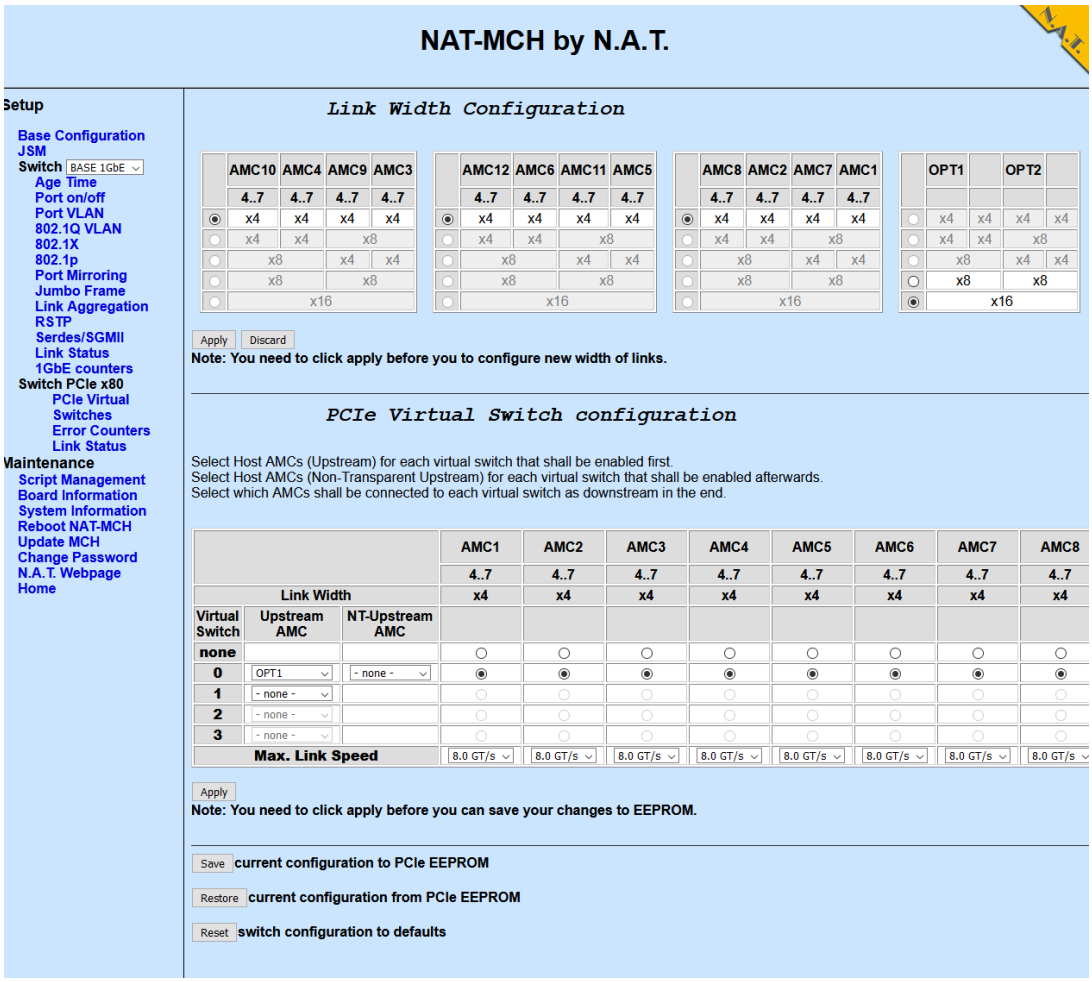
For basic configuration **NAT-MCH** firmware 2.21.9 or higher is required, as well as **NAT-MCH-HUB-PCIex80** AVR 1.10 or higher, and FPGA V1.3 or higher.

6.1. Basic Configuration

Once connected to the **NAT-MCH-PHYS80**, the **NPCIe-Uplink-O** can be configured by web interface.

- Choose '`Switch PCIe x80 → PCIe Virtual Switches`' to see the following matrix:

Figure 12 – Configuration via Web Interface



- Choose '`Width configuration (x16 or x8/x8)`' according to your Uplink board
- Click '`Apply`'

- Set ‘Opt1’ as your Upstream port in ‘Pcie Virtual Switch Configuration’ below
- Click ‘Apply’
- Click ‘Save’ to store current configuration in EEPROM

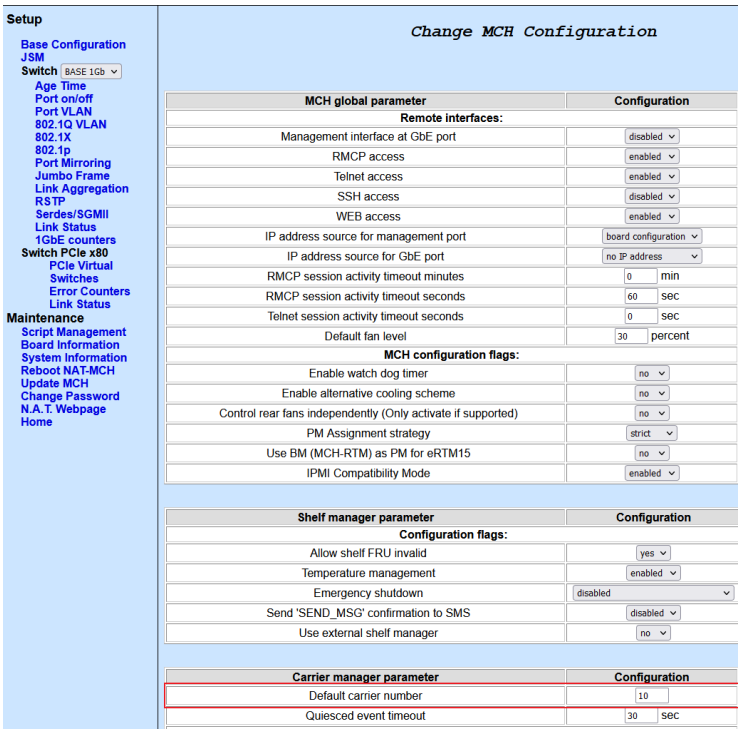
6.2. Mapping between PCIe-Devices and NAT-MCH-PHYS80

If a **NPCIe-UPLINK-O** is connected to two **NAT-MCH-PHYS80** modules, it is mandatory to identify, which PCIe device is mapped to which **NAT-MCH-PHYS80**.

Please note: the following configuration option is only available with **NAT-MCH-PHYS80** FW 2.22.5 and higher!

As shown in the figure below, a Default Carrier Number (>1 and <16) can be chosen. Save and reboot afterwards.

Figure 13 – Default Carrier Number Configuration



After reboot, enter the PCIe Virtual Switch Configuration via the web interface. By clicking the ‘Save’ button, the information is written into the EEPROM of the x80 PCIe switch on the **NAT-MCH-PHYS80**.

Now the Carrier Number can be found in the capabilities of the appropriate PCIe device on the **NPCIe-UPLINK-O**.

With Linux, all PCIe devices can be listed with the command:

`'sudo lspci -P -v'`

The entry `'Vendor Specific Information'` shows the Carrier Number ID as highlighted in the screenshot below.

Figure 14 – Carrier Number in PCIe Device Capabilities

```
00:01.0/00.0/09.0/00.0/0a.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab) (prog-if 00 [Normal decode])
        Flags: bus master, fast devsel, latency 0, IRQ 40
        Bus: primary=05, secondary=0b, subordinate=0b, sec-latency=0
        I/O behind bridge: 00008000-00008fff [size=4K]
        Memory behind bridge: [disabled]
        Prefetchable memory behind bridge: 00000000f0c00000-00000000f0dfffff [size=2M]
        Capabilities: [40] Power Management version 3
        Capabilities: [48] MSI: Enable+ Count=1/8 Maskable+ 64bit+
        Capabilities: [68] Express Downstream Port (Slot+), MSI 00
        Capabilities: [a4] Subsystem: PLX Technology, Inc. Device 8780
        Capabilities: [100] Device Serial Number ab-87-00-10-b5-df-0e-00
        Capabilities: [fb4] Advanced Error Reporting
        Capabilities: [138] Power Budgeting <?>
        Capabilities: [10c] Secondary PCI Express
        Capabilities: [148] Virtual Channel
        Capabilities: [e00] Multicast
        Capabilities: [f24] Access Control Services
        Capabilities: [b70] Vendor Specific Information: ID=000a Rev=0 Len=010 <?>
        Kernel driver in use: pcieport
```

7. FIRMWARE UPDATE

Usually only the **NAT-MCH-M4** base module firmware must be updated. But it is also possible that the **NAT-MCH-PCIex80** itself needs an update.

In both cases, the update procedure is executed via web interface or CLI. Please refer to the corresponding section of the **NAT-MCH** User's Manual (chapter 8.1 Internal Reference Documentation).

8. SPECIFICATIONS AND COMPLIANCES

8.1. Internal Reference Documentation

- **NAT-MCH**
  Please find the latest versions of all documents on our product website by clicking on the "Collaterals"-Button.

8.2. External Reference Documentation

- Atmel ATmega1284P Microcontroller Data Sheet, Rev. 8059D, 11/2009
- Lattice MACHXO2 FPGA Family Data Sheet, Rev 1.0, 11/2010
- PLX PEX8780 PCIe Switch Product Brief, V1.0, 10/2010

8.3. Standards Compliance

- PCI Express Base Specification Rev. 1.1
- PICMG µTCA.0 Rev. 1.0
- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)
- IPMI Specification v2.0 Rev. 1.0

8.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant

deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

8.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

8.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

8.7. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8.8. Abbreviation List

Table 10 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
FCLKA	Fabric Clock
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
I^2C	Inter-Integrated Circuit
IPMI	Intelligent Platform Management Interface
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
MPO	Multiple-Fiber Push-On/Pull-off - Optical Fiber Connector
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
QoS	Quality of Service
RTM	Rear Transition Module
SerDes	Serializer/Deserializer
SPI	Serial Peripheral Interface

9. DOCUMENT'S HISTORY

Table 11 – Document's History

Rev	Date	Description	Author
0.9	16.09.2014	• Initial release	SE
1.0	01.04.2016	• Minor corrections	KS
1.1	28.04.2025	• Migration to current document design • Reworked complete document • Adaption to latest HW-Version 1.3 (QSFP-DD instead of MPO)	Se