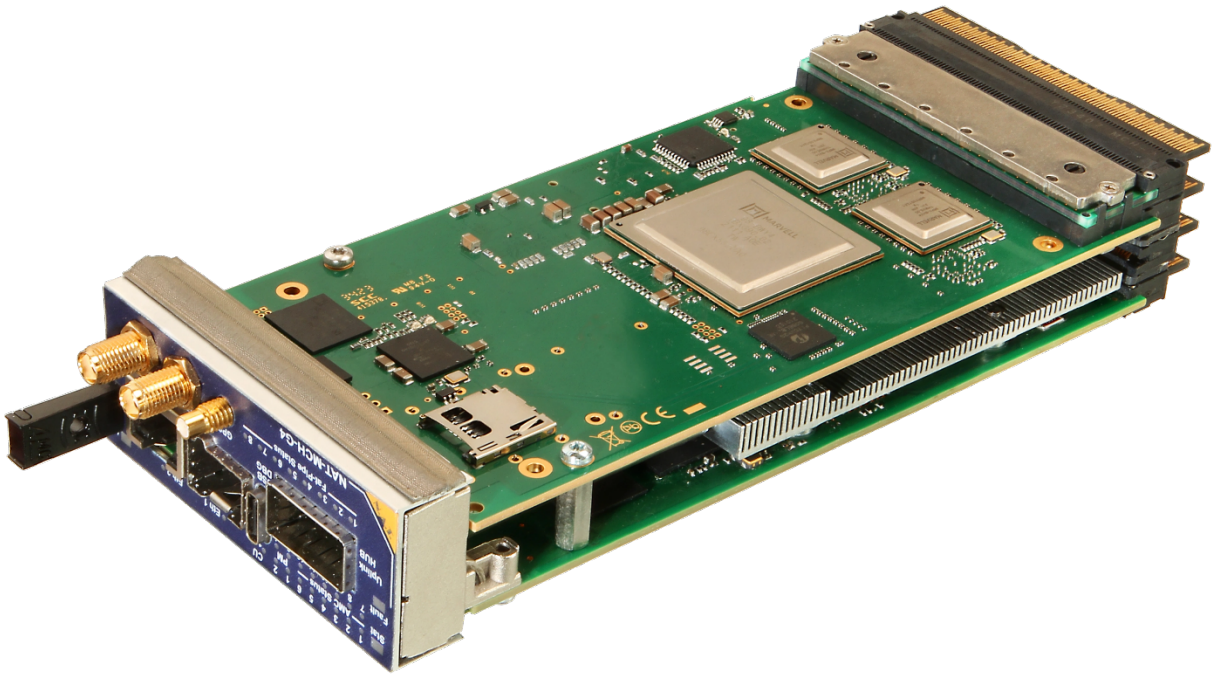
NAT-MCH-G4

4TH GENERATION MTCA CARRIER HUB

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.8

HW REVISION 1.X

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1. PREFACE

1.1. Disclaimer

The following documentation, compiled by N.A.T. GmbH (henceforth called N.A.T.), represents the current status of the product´s development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. N.A.T. is under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document gives an overview on the **NAT-MCH-G4's** functional capabilities. To cover all possible variants, it is divided into several sections:

Preface

General information about this document

Introduction

Abstract on the **NAT-MCH-G4's** main functionality and field of applications

Getting Started

Important information and mandatory requirements to be considered before operating the **NAT-MCH-G4** for the first time

NAT-MCH-G4 Base Board

Detailed information on main features, functional description, front panel, and LEDs for the base board

NAT-MCH-G4 Clock Mezzanine

Detailed information on main features, functional description, front panel, and LEDs for the clock mezzanine

NAT-MCH-G4 HUB Modules

Detailed information on main features, functional description, front panel, and LEDs for HUB modules

Specifications and Compliances

List of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-MCH-G4** complies to

Document's History

Revision record

Note:

It is assumed that the **NAT-MCH-G4** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-MCH-G4** MicroTCA Carrier Hub family comprises of a base module, a clock mezzanine, and various Hub modules for Fat Pipe connections. Depending on the variant, these daughter cards provide up to 40GbE or PCIe Gen5 x8 links to the backplane. Various uplink options (up to 100GbE or PCIe Gen4 x16) at the front panel offer a wide and flexible range of possible choices to connect the MCH to external networks.

Moreover, RTM support with a PCIe Gen5 x16 link is possible (depending on chosen variant).

2.1. Base Board Variants

Basically, the **NAT-MCH-G4** provides central management and data switching as well as power and system management for any MicroTCA system with up to 12 AMCs. Yet another AMC can be operated in the second MCH slot without Fat Pipe functionality. Beyond that, the **NAT-MCH-G4** supplies up to two front and two rear Cooling Units as well as up to four Power Modules.

The base Ethernet Switch features a 1G/2.5G/10G Fabric A connection to each AMC. Basically, the **NAT-MCH-G4** features two 1-10G Ethernet uplinks the front panel. Depending on the assembly option, the front uplink even provides up to 4x 25G. Please consider, that these four ports cannot be combined to one port.

Another 25G Update Fabric connects to an optional second MCH in the MTCA system.

The **NAT-MCH-G4** comes in the form factor of a single-width, full-size AMC, compliant with the latest revision 3 of the MTCA.0 specification. For MTCA.4 systems, NAT offers the **NAT-MCH-S4**, a double-width, full-size MicroTCA Carrier Hub. Technically, it provides the same functionality as the single-width board but comes with optional RTM support and mounting space for NVMe / SSD memory devices.

Most information in this document is valid for both variants, so – unless otherwise specified – for reasons of clarity it is referred to **NAT-MCH-G4** only.

2.2. Clocking

In combination with an optional clock module, the **NAT-MCH-G4** offers several options for switching and manipulating clock signals.

Basically, two clock module variants are available:

The **NAT-MCH-G4-CLKP** comes with two low jitter Clock multiplexers providing CLK1 and CLK2 (MLVDS) to each AMC, CLK3 is executed as PCIe Reference Clock .

On the **NAT-MCH-G4-CLKT**, CLK3 is executed as a regular telecom clock.

Both variants feature two SMA connectors at the front panel to feed an external CLK signal to the MCH or to extract a CLK generated in the system. The direction of each SMA connector is configurable, the maximum frequency limit (as per MTCA.0 spec) is 100MHz.

As an assembly option, a precision timing (IEEE1588) variant is available for both modules which includes an optional GPS receiver with a dedicated SMC connector at the front panel to attach a GPS antenna and an onboard OCXO.

2.3. Ethernet Switching

Beyond the base Ethernet, the **NAT-MCH-G4-HUB-EX** module offers Fat Pipe Ethernet connections. It provides 10GbE (12 x4 lanes @ 2.5GbE) or even 40GbE (12 x4 lanes @10GbE) per AMC. Alternatively, four x1 ports with 1-10G are available for each AMC. The protocol can be set for each AMC independently.

A QSFP-DD uplink with 8x 1-25G can be operated as e.g., 2 x4@100GbE or 8 x1@25GbE.

Moreover, the **NAT-MCH-G4-HUB-EX** owns a x4 MCH update channel @ 10G/40G to a second MCH in the MTCA system.

2.4. PCIe Functionality

The **NAT-MCH-G4** MicroTCA Carrier Hub family features two HUB modules for applications requiring Fat Pipe PCIe functionality:

The single-width **NAT-MCH-G4-HUB-Px52** can be operated on both base module variants. It provides a QSFP-based PCIe Gen4 x4 uplink at the front panel as well as PCIe Gen4 x4 switching to each AMC. If supported by the backplane, PCIe Gen4 x8 links are available for up to 6 AMCs.

The double-width **NAT-MCH-G4-HUB-Px84** module is designed to perform with the **NAT-MCH-S4**, including RTM support as assembly option. It offers PCIe Gen5 x4 to all 12 AMCs (or x8 for up to six AMCs if supported by the backplane) as well as a PCIe Gen5 x16 (or two x8) uplink(s) via two QSFP-DD interfaces (depending on transceiver type). Additionally, PCIe Gen5 x16 is provided to an optional RTM.

The PCIe switches support multiple independent clusters with one Root Complex each.

2.5. Front panel uplinks

Various uplink options at the front panel offer a wide and flexible range of possible choices to connect the **NAT-MCH-G4** to external networks:

The **NAT-MCH-G4** base board offers Ethernet connections via SFP(-DD), ix, or RJ45 with 1-25G depending on the assembly option.

The **NAT-MCH-G4-HUB-EX** Fat Pipe Ethernet module features a QSFP-DD front uplink with 8x 1-25G.

The **NAT-MCH-G4-HUB-Px52** Fat Pipe PCIe module owns a PCIe Gen4 x4 uplink via QSFP, whereas the double-width **NAT-MCH-G4-HUB-Px84** features a PCIe Gen5 x16 (or two x8) uplink(s) via two QSFP-DD interfaces. Please note that the uplink transmission standard depends on the transceiver type.

Both clock module variants provide two SMA connectors for input or output of an up to 100MHz clock. With the precision timing assembly option, the clock modules come with an additional SMC connector for input of a GPS signal.

2.6. NAT-MCH-SCI for Science

Especially for the science community, NAT provides three product packages optimized for the special needs of this target group:

NAT-MCH-SCIx52: combination of the **NAT-MCH-S4**, the **NAT-MCH-G4-CLKP**, and the **NAT-MCH-G4-HUB-Px52** with one PCIe Gen4 x4 front uplink and no RTM support.

NAT-MCH-SCIx84: combination of the **NAT-MCH-S4**, the **NAT-MCH-G4-CLKP**, and the **NAT-MCH-G4-HUB-Px84** with one PCIe Gen5 x16 (or two x8) front uplinks and RTM support.

NAT-MCH-SCIxE: combination of the **NAT-MCH-S4**, the **NAT-MCH-G4-CLKP**, and the **NAT-MCH-G4-HUB-EX** with a QSFP-DD front uplink with 8x 1-25G.

2.7. Main Features

Table 1 – Main Features

Form Factor		
	• Single- or double-width, full-size Form Factor	
Base Board – NAT-MCH-G4 / -S4		

Processing Resources	• Xilinx Zynq MPSoC
	  • FPGA
	  • 2x ARM A9
	• 1GB DDR3 RAM, 32 bit-wide
	• 256 MB QSPI FLASH
	• IPMI Functionality via FPGA Section
	• Software / Firmware: FreeRTOS	

Base Ethernet Switch	• Microchip SparX-5 Base Ethernet Switch
	  • DDR4 RAM
	  • FLASH	

Front Uplink (assembly option)	• 4x 1-25G optical Base Ethernet via SFP-28-DD (depending on plug-in module) • 2x 1-10G Base Ethernet via ix • 2x 1-10G Base Ethernet vis RJ45	
Backplane	• Up to 12x 1GbE / 2.5GbE / 10GbE towards AMCs (assembly option) • 10G uplink to Fat Pipe Ethernet switch on HUB module • 25G update fabric to 2nd **NAT-MCH-G4**	
RTM-Support	• **NAT-MCH-S4-R** only – via Zone3 connector	
LEDs	• Standard AMC LEDs (Status, Fault, Hot-Swap) • 16 LEDs reflecting AMC / CU / PM status • Console via USB	
Clock Mezzanine		
	NAT-MCH-G4-CLKP	**NAT-MCH-G4-CLKT**
Processing Resources	• CLK1 / CLK2: 2x AD ADN4605 Clock Cross-Point-Switch (M-LVDS) • CLK3: PCIe Ref CLK (HCSL) • PLL synthesizer for any frequency operation • IEEE1588 support, Synchronous Ethernet support, Local oscillator (OCXO), and GPS receiver as precision timing assembly option	• CLK1-3: 3x AD ADN4605 Clock Cross-Point-Switch (M-LVDS) • PLL synthesizer for any frequency operation • IEEE1588 support, Synchronous Ethernet support, Local oscillator (OCXO), and GPS receiver as precision timing assembly option
Front Panel Connectivity	• CLK IN / OUT via SMA • GPS IN via SMC (comes with precision timing assembly option)	

Ethernet HUB Module – NAT-MCH-G4-HUB-EX		

Processing Resources	• Dual A53 Marvell 88F3720 CPU
	  • 4 GB eMMC
	  • 2 GB DRAM DDR4-1600, 16 bit
	• Marvell 98EX5520 Ethernet Switch
	• 4x Marvell 98PX1012 Port Extenders	

Front Panel Connectivity	• 1x QSFP-DD front uplink with eight 1-25G:
	  • Optical Short Range (100-300m)
	  • Optical Long Range (2-40km)
	  • Copper
	• Can be operated as e.g.:
	  • 2 x4 ports with up to 100GbE
	  • 8 x1 ports with up to 25GbE
	• 8x Fat-Pipe Status LEDs	

Backplane Connectivity	• 40G Ethernet to backplane can be operated as e.g.,
	  • x4 ports with 40GbE to each AMC
	  • x4 ports with 10GbE (XAUI) to each AMC
	  • 4 x1 ports with 1-10G to each AMC
	  • Protocol can be set for each AMC independently
	• 10GbE / 40GbE update to 2nd **NAT-MCH-G4** (no XAUI)	

PCIe HUB Modules		
	NAT-MCH-G4-HUB-Px52	**NAT-MCH-G4-HUB-Px84**
Processing Resources	• PCIe Switch Gen4 Switch with 52 lanes • Parallel operation of multiple PCIe domains • Non-transparent bridges for multiple root-complex CPU AMCs	• PCIe Switch Gen5 Switch with 84 lanes • Parallel operation of multiple PCIe domains • Non-transparent bridges for multiple root-complex CPU AMCs

Front Panel Connectivity	• 1x PCIe Gen4 x Front Uplink via QSFP:
	  • Optical Short Range (100-300m
	  • Optical Long Range (2-40km)
	  • Copper
	• 8x Fat-Pipe Status LEDs
		• 2x PCIe Gen5* x8 via 2x QSFP-DD
		  • Optical Short Range (100-300m)
		  • Optical Long Range (2-40km)
		  • Copper
		• Can also be operated as
		  • 1x PCIe Gen5* x16 Front Uplink
		• 8x Fat-Pipe Status LEDs

Backplane Connectivity	• PCIe Gen4 x4 to 12 AMCs • PCIe Gen4 x8 for up to 6 AMCs (if supported by backplane)	• PCIe Gen5 x4 to 12 AMCs • PCIe Gen5 x8 for up to 6 AMCs (if supported by backplane)
RTM Connectivity	• n/a	• PCIe Gen5 x16 link via Zone3 connector on **NAT-MCH-S4-R** (optional)

Compliance		
	• MTCA.0 / MTCA.4 • AMC.0, AMC.1, AMC.2, AMC.3, AMC.4 • IMPI V1.5 • HPM.1 • RoHS, REACH, CE	
Order Codes NAT-MCH [Form Factor] – [Front Uplink] – [Clock] – [HUB]		
Form Factor	- G4	Single-width, full-sized Base Board
	- S4-0	Double-width, full-sized Base Board, no RTM support
	- S4-R	Double-width, full-sized Base Board, with RTM support
Front Uplink	- RJ45	2x RJ45 Interfaces
	- iX	2x iX Interfaces
	- SFP	2x SFP Interfaces
Clock Module	- CLKP	CLK1 + CLK2: M-LVDS CLK3: PCIe Ref Clock (HCSL)
	- CLKP-PT	CLK1 + CLK2: M-LVDS CLK3: PCIe Ref Clock (HCSL) GPS receiver OCXO
	- CLKT	CLK1-CLK3: M-LVDS
	- CLKT-PT	CLK1-CLK3: M-LVDS GPS receiver OCXO
HUB	- EX	Ethernet HUB Module
	- Px52	PCIe x52 Switch, 1x PCIe Gen4 x4 Front Uplink, single-width form-factor, no RTM support
	- Px84	PCIe x84 Switch, 2x PCIe Gen5* x8 Front Uplink, double-width form factor, with RTM support
Pre-Configured Combo #1	**NAT-MCH-SCIx52**	• **NAT-MCH-S4-0** Base Board • RJ45 Front Uplink • **NAT-MCH-G4-CKLP** • **NAT-MCH-G4-HUB-Px52** • no RTM-Support
Pre-Configured Combo #2	**NAT-MCH-SCIx84**	• **NAT-MCH-S4-R** Base Board • RJ45 Front Uplink • **NAT-MCH-G4-CKLP** • **NAT-MCH-G4-HUB-Px84** • with RTM-Support
Pre-Configured Combo #3	**NAT-MCH-SCIxE**	• **NAT-MCH-S4-0** Base Board • RJ45 Front Uplink • **NAT-MCH-G4-CKLP** • **NAT-MCH-G4-HUB-EX** • with RTM-Support
Environmental		
Operating Environment	• Default temperature range: 0° to +55° Celsius • Extended temperature range: -40° to +85° Celsius • Humidity: 10% to 90% (non-condensing)	
Storage Environment	• Default temperature range: -40° to +85° Celsius • Humidity: 10% to 90% (non-condensing)	

Please note: the front uplink transmission standard depends on transceiver type

3. GETTING STARTED

To ensure proper functioning of the **NAT-MCH-G4** during its lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching and contaminating the golden pins of the connectors to ensure proper contact when connecting the **NAT-MCH-G4** to the MTCA-System.

Make sure that the board and its accessories are undamaged. Please also check that you have the complete set of accessories as stated on the delivery note.

3.2. Inserting the NAT-MCH-G4

The installation requires a MicroTCA system with backplane and cooling units.

Before installing or uninstalling the **NAT-MCH-G4**, read the Installation Guide and the User's Manual of the **NAT-MCH-G4** and the one of the MicroTCA system the MCH will be plugged into.

Do not turn on or off power before checking all already installed boards and modules for any necessary steps to take before turning on or off power.

Now insert the **NAT-MCH-G4** into the MicroTCA system and ensure that it is properly seated into the backplane connector(s). When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the rear panel or rack, and shielded by closed housing.

The **NAT-MCH-G4** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to exactly follow the hot-swap procedure to prevent damaging any hardware:

Insertion of a hot-swap-capable module

- Ensure the module and the power module support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the module carefully into the dedicated slot until it is completely seated in the connector(s).
- Check if the blue HS-LED turns on solid
- Now push in the hot-swap-handle to its "lock"-position.

- Check if the blue HS-LED starts blinking. In this case the module is being detected by the system management, and once the e-keying process has successfully finished, the module is connected to payload power.
- Check if the blue HS-LED is turned off and the module is operational.

Extraction of a hot-swap-capable module

- Pull the hot-swap-handle in "unlock"-position.
- The blue HS-LED of the module starts blinking and the system management is starting to disable payload power for this module.
- Once the payload power has been disabled, the blue HS-LED turns on solid
- It is now safe to remove the module from its slot.

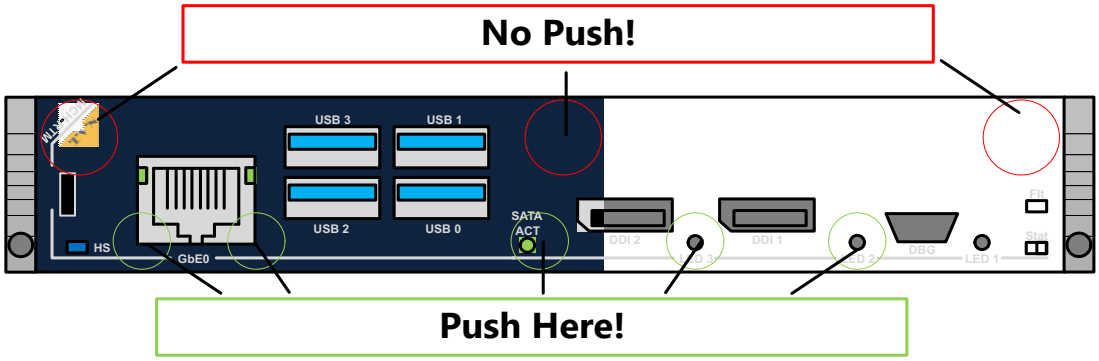
3.3. Operation with NAT-MCH-RTM

Insert the **NAT-MCH-RTM** ***first*** and ensure a proper connection, ***before*** pushing the **NAT-MCH-S4** into the system!

Important: when installing the **NAT-MCH-RTM** to an MTCA-System, make sure to avoid any torsion force impact on the PCB to prevent the module from damaging!

Therefore, always push ***in line*** with the PCB. The following figures illustrates, which spots on the rear panel are safe to use, and which areas ***must not*** be used to push the **NAT-MCH-RTM** into its mating connector.

Figure 1 – NAT-MCH-RTM: Pushing Points for Mounting



3.4. Connections to CLK I/O and GPS

When connecting cables to the CLK and GPS interfaces, make sure to use the appropriate moment of force to prevent the connectors from being damaged.

SMA connectors (CLK I/O): 0.9Nm

SMC connectors (GPS in): 0.3Nm

3.5. First steps

Please follow the instructions documented in the **NAT-MCH-G4** Quick Start Guide (see chapter 10.1 Internal Reference Documentation).

4. NAT-MCH-G4 – BASE BOARD

4.1. Functional Description

Compared to its predecessor, the **NAT-MCH-G4** base board offers significantly enhanced functionality.

The XILINX Zynq MPSoC is the processing core of the module.

The base Ethernet switch supports up to 25G link speeds at the front panel and at the backplane connectors.

There are several front panel interface options available. Please refer to section 4.3. for details.

Figure 2 – Block Diagram NAT-MCH-G4 Base Board

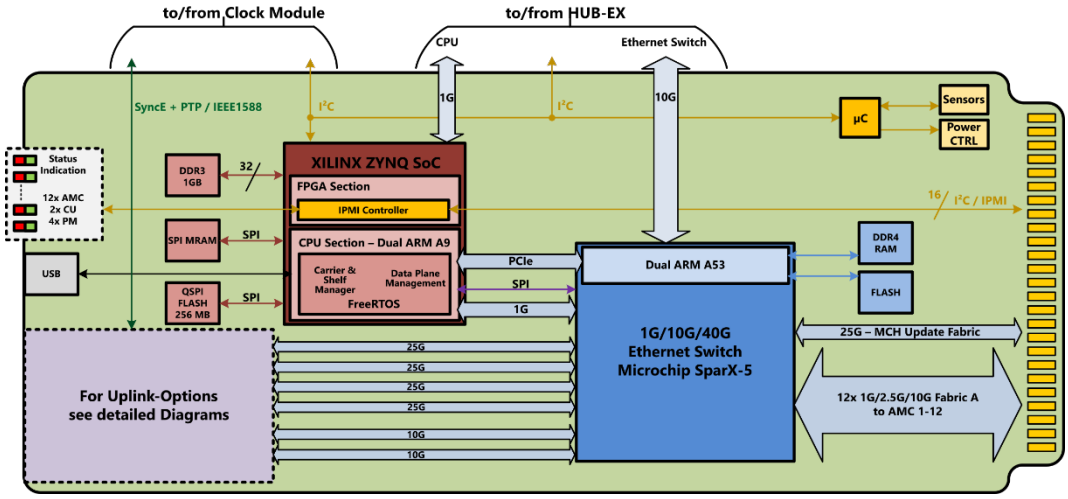
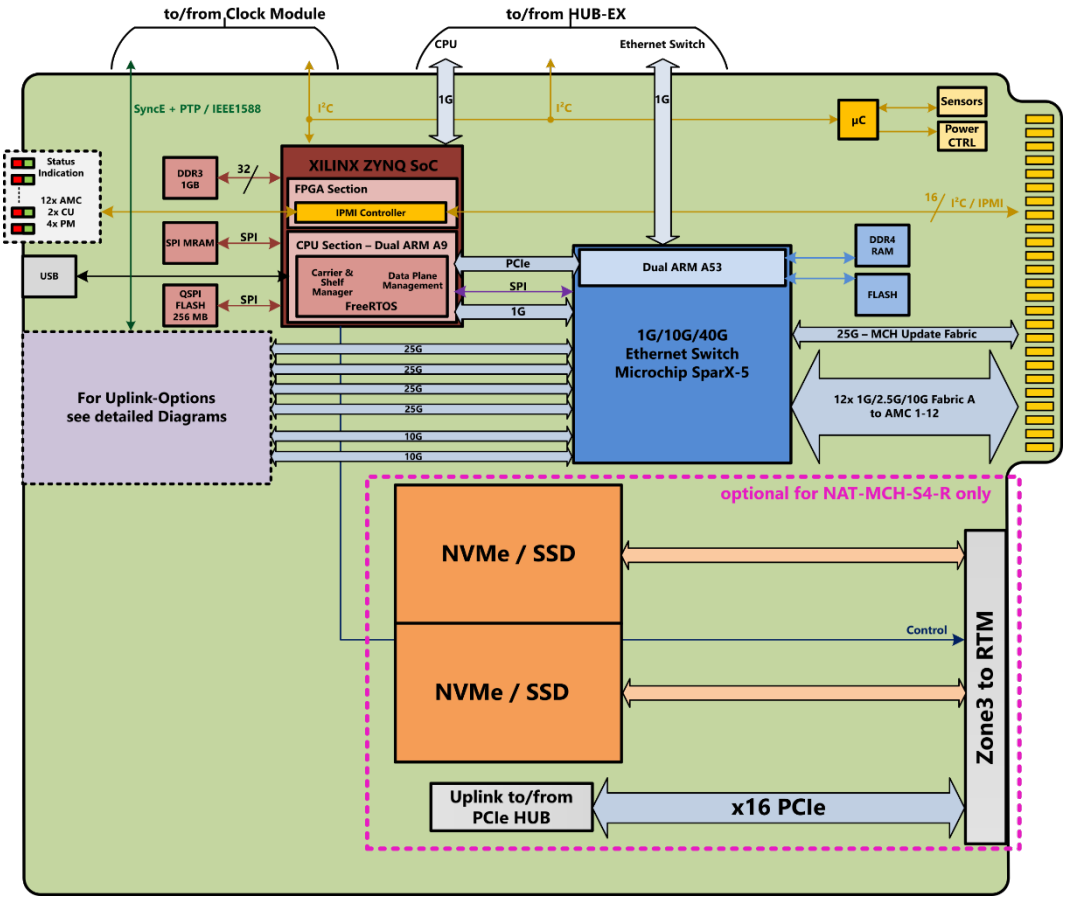


Figure 3 – Block Diagram NAT-MCH-S4 Base Board



4.1.1. XILINX ZYNQ MPSoC

The XILINX Zynq MPSoC is a combination of a Processing System (PS) and an FPGA core, often referred to as Programmable Logic (PL).

4.1.1.1. Processing System

The Processing System features two ARM A9 cores, running a FreeRTOS operating system. It is supported by SPI MRAM and QSPI FLASH.

This unit connects to the Ethernet switch and can be accessed through the front panel USB port.

4.1.1.2. Programmable Logic

Main task of the FPGA section is providing the logic for IPMI functionality.

4.1.2. Microchip Base Ethernet Switch

The **NAT-MCH-G4** owns the latest generation Microchip SparX-5 Base Ethernet switch. It features a 1G / 2.5G / 10G Fabric A connection to each of the 12 AMCs as well as a 25G Update Fabric to a second **NAT-MCH-G4** in the system.

Additionally, the switch is connected to the Fat Pipe Ethernet switch of an optional **NAT-MCH-G4-HUB-EX** via a 10G uplink.

At the front panel, up to 25G are feasible, see chapter 4.3 Front Panel Connectivity for details.

4.1.3. Clocking

The base Ethernet switch supports IEEE1588 (PTP). This feature becomes available with the precision timing assembly option of the clock module.

4.2. NAT-MCH-S4: RTM-Support and Memory Extension

As an assembly option, the double-width **NAT-MCH-S4-R** comes with a Zone3 connector for operating an optional **NAT-MCH-RTM**. In combination with a **NAT-MCH-G4-HUB-Px84**, a PCIe Gen5 x16 link can be provided to the RTM.

Moreover, the **NAT-MCH-S4-R** base board offers mounting space for memory extensions in NVMe or SSD standard.

4.3. Front Panel Connectivity

The **NAT-MCH-G4** provides several interfaces at the front panel as well as three Ethernet front uplink options.

4.3.1. Front Ethernet Uplink Option #1: SFP(-DD)

Figure 4 – Front Panel NAT-MCH-G4 Base Board with SFP(-DD) Front Uplink

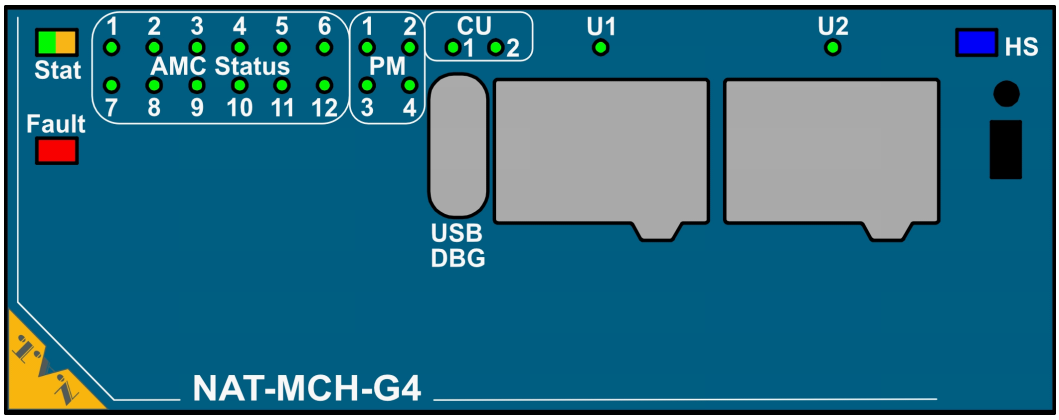
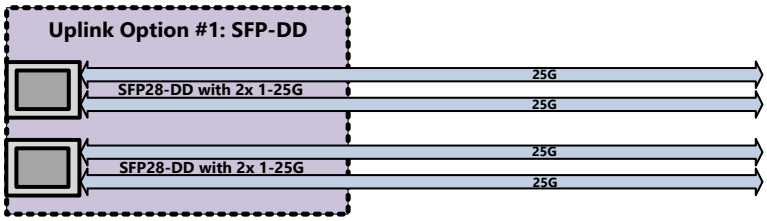


Figure 5 – Front Ethernet Uplink Option #1: SFP(-DD)



By featuring two rows of electrical pins instead of one, the SFP-DD (double density) cage and receptable offer doubled port density and increased data transfer rates within a small form factor. Data rates up to 25G per port are supported, which result in 4x 25G in total. Please consider, that these four ports cannot be combined to one port.

Nevertheless, the SFP-DD cages offer backwards compatibility to existing SFP receptables.

4.3.2. Front Ethernet Uplink Option #2: ix

Figure 6 – Front Panel NAT-MCH-G4 Base Board with iX Front Uplink

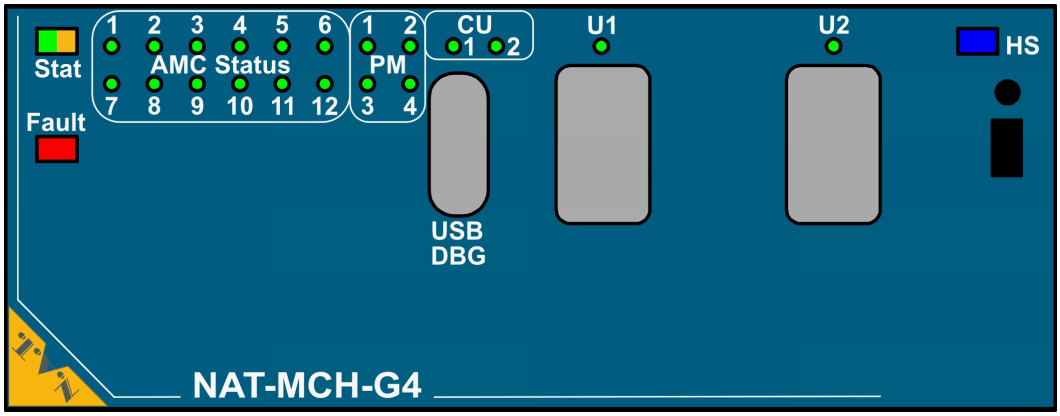
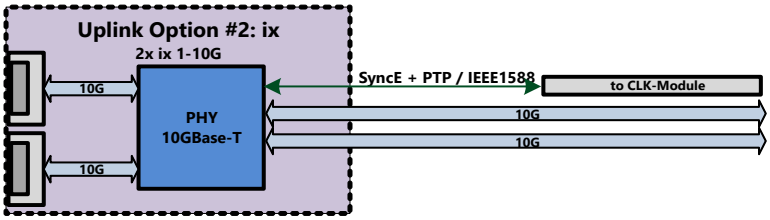


Figure 7 – Front Ethernet Uplink Option #2: ix



The ix connector is a robust alternative to the commonly used RJ45 connector. It requires much less space, and at the same time ensures a more reliable connection by two metal retention hooks snapping into the socket. It supports transmission rates up to 10G.

4.3.3. Front Ethernet Uplink Option #3: RJ45

Figure 8 – Front Panel NAT-MCH-G4 Base Board with RJ45 Front Uplink

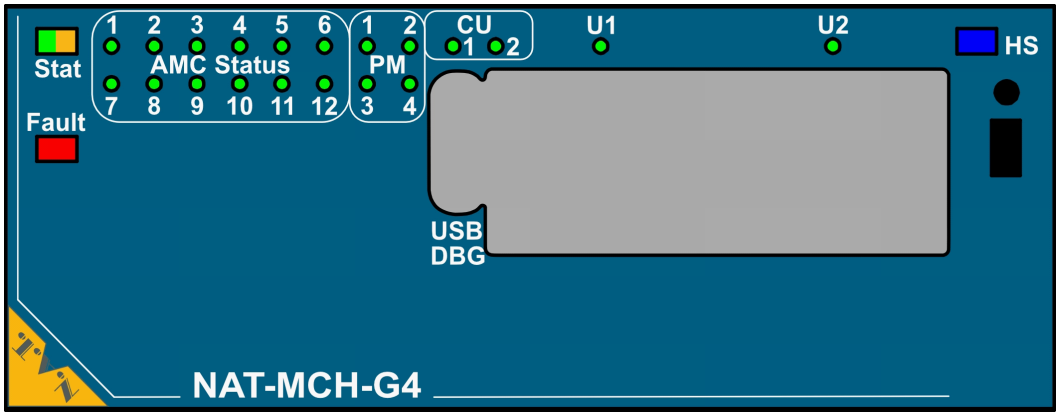
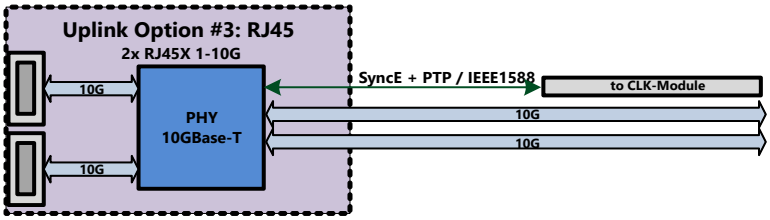


Figure 9 – Front Ethernet Uplink Option #3: RJ45



The RJ45 connector is a well-established Ethernet interface standard, supporting data rates up to 10G.

The **NAT-MCH-G4** is equipped with various LEDs, which are the same for all front uplink variants. The functionality is described in the following table.

Table 2 – LED Functionality NAT-MCH-G4 Base Board

LED	Color	Function	Control / Description
Stat LED	Green	tbd	Microcontroller
	Yellow	tbd	Microcontroller
Fault LED	Red	ON	Microcontroller Temperature exceeding / underrunning threshold level
		OFF	Microcontroller Temperature OK
AMC HS LED	Blue	ON	Microcontroller please refer to chapter 3.2 Inserting the NAT-MCH-G4
		blink	
		OFF	
AMC Status LED 1-12	Green	ON / OFF	Green ON: Unit OK Red ON: Unit Fails OFF: Unit not available
	Red		
PM LED 1-4	Green	ON / OFF	
	Red		
CU LED 1+2	Green	ON / OFF	controlled by MPSoC
	Red		
U1	Green	tbd	controlled by MPSoC
	Yellow		
U2	Green		
	Yellow		

4.4. Backplane Connectivity

The base Ethernet switch offers 1G / 2.5G / 10G towards the backplane on Fabric A. Moreover, it supports a 25G update channel to a second **NAT-MCH-G4** in the system.

As per the specification, the **NAT-MCH-G4** provides IPMI connectivity on IPMB-0 and IPMB-1 as well as IPMB-L to all AMC.

In combination with the clock module, the **NAT-MCH-G4** also provides the backplane connections for CLK1, CLK2, and CLK3.

4.5. User Guide

For a detailed description of the **NAT-MCH-G4**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

5. NAT-MCH-G4-CLKP – CLOCK MEZZANINE WITH PCIE REFERENCE CLOCK

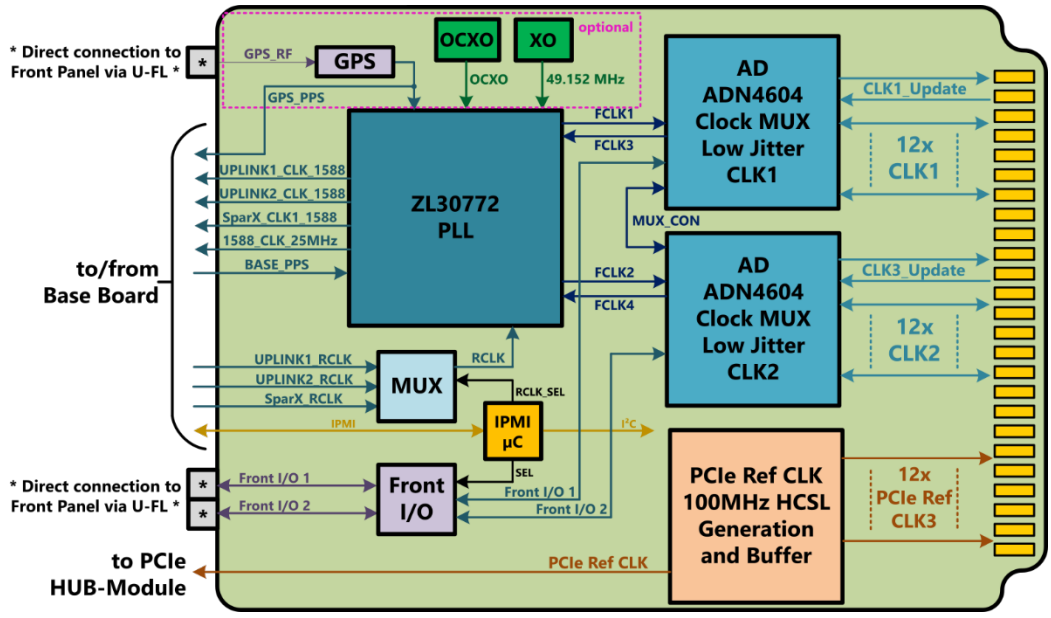
The **NAT-MCH-G4** can be optionally equipped with a clock mezzanine which then provides CLK1, CLK2, and CLK3 to the respective AMC clock connections via the backplane.

5.1. Functional Description

The **NAT-MCH-G4-CLKP** is equipped with a Microsemi ZL30772 PLL, two AD ADN4604 low jitter clock multiplexers, and PCIe clock generation and buffering.

With the precision timing option (shown in the block diagram below within the pink dotted square), the **NAT-MCH-G4-CLKP-PT** provides clock operation according to IEEE1588 standard. This assembly option comes with a GPS receiver connecting to a separate SMC interface at the front panel and an onboard OCXO.

Figure 10 – Block Diagram NAT-MCH-G4-CLKP(-PT) Mezzanine



5.1.1. Microsemi ZL30772 PLL

The onboard PLL interacts with many different units of the **NAT-MCH-G4**:

- Clock I/O at front panel
- Base Front Panel Uplink
- GPS IN at front panel (assembly option)
- OCXO oscillator (assembly option)
- Base board Ethernet Switch (IEEE1588) (assembly option)
- If mounted: **NAT-MCH-G4-HUB-EX**, **-HUB-Px52**, or **-HUB-Px84 HUB** modules

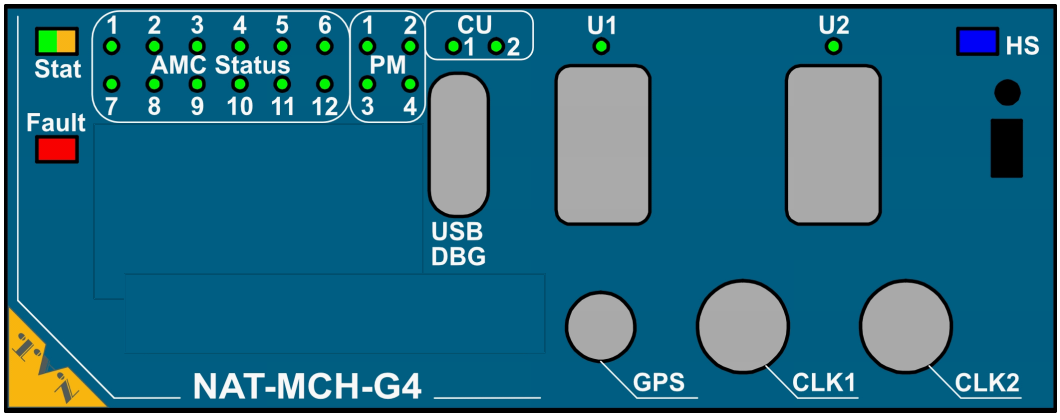
5.1.2. Clock Multiplexers

The **NAT-MCH-G4-CLKP** provides two low-jitter M-LVDS clock multiplexers connected to CLK1 and CLK2 for each AMC. CLK3 is executed as HCSL PCIe Reference Clock.

5.2. Front Panel Connectivity

The **NAT-MCH-G4-CLKP** offers several interfaces at the front panel which are described below.

Figure 11 – Front Panel NAT-MCH-G4 Base Board with iX Front Uplink / Clock Mezzanine



Please note: The appearance of the front panel differs depending on the chosen base board uplink. Nevertheless, the clock interfaces are the same for all three variants, so this drawing with the iX interface is exemplary for all options.

5.2.1. Clock I/O

Clock IN and OUT signals are available at the front panel via SMA connectors. The maximum frequency is limited as per MTCA.0 spec to 100MHz.

The following table provides input clock parameters:

Table 3 – Input Clock Parameters

Measurement	AC Coupling	DC Coupling
Minimum frequency for symmetrical sine or square wave	1 Hz @ 500mVpp	1Hz @ 2 Vpp (2 V high, 0 V low)
Maximum frequency for symmetrical sine or square wave	200 MHz @ 1Vpp	200 MHz @ (2 V high, 0 V low)
Pulse 1PPS	1Vpp (1V high, 0V low, into 50R load), 100µs high pulse-duration	1Vpp (1V high, 0V low, 50R load), 100µs high pulse-duration
Steady high or low	n/a	1Vpp (1V high, 0V low, into 50R load)

When using DC coupling, the input signals must be between 0 V and 3.3 V. Square wave or pulse signals are recommended to get clear and consistent rising edges.

5.2.2. Jitter

All jitter measurements are done using a Lecroy SDA 813Zi Oscilloscope. For the Front-I/O channels, a 100MHz clock is generated by a UNI-T UTG4202A Waveform Generator

The total peak-to-peak-jitter is then measured at different stages of the board, as well as directly on the UTG4202A, to quantify the impact of the different components on the total jitter.

Table 4 – Jitter Measurement

Measurement	Total Jitter (ps)	Added Jitter (ps)
UTG4202A Waveform Generator	25 (@ 100MHz)	-
Signal routed from FIO to TCLKA/TCLKB	33	22
TCLKA/TCLKB generated locally by the PLL	45	

5.2.3. GPS

GPS IN is available within the precision timing assembly option. Via the SMC interface at the front panel, a standard GPS antenna signal is fed directly into the **NAT-MCH-G4**.

5.3. Backplane Connectivity

At the backplane, the **NAT-MCH-G4-CLKP** provides CLK1, CLK2, and CLK3 to all AMCs in the system. CLK1 and/or CLK2 can be generated locally on the clock module or by any AMC in the system.

5.4. User Guide

For a detailed description of the **NAT-MCH-G4-CLKP**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

6. NAT-MCH-G4-CLKT – CLOCK MEZZANINE WITH 3X TELECOM CLOCK

The **NAT-MCH-G4** can be optionally equipped with a clock mezzanine which then provides CLK1, CLK2, and CLK3 to the respective AMC clock connections via the backplane.

6.1. Functional Description

The **NAT-MCH-G4-CLKT** is equipped with a Microsemi ZL30772 PLL and three AD ADN4604 low jitter clock multiplexers.

With the precision timing option, the **NAT-MCH-G4-CLKT-PT** provides clock operation according to IEEE1588 standard. This assembly option comes with a GPS receiver connecting to a separate SMC interface at the front panel and an onboard OCXO.

6.1.1. Microsemi ZL30772 PLL

The onboard PLL interacts with many different units of the **NAT-MCH-G4**:

- Clock I/O at front panel
- Base Front Panel Uplink
- GPS IN at front panel (assembly option)
- OCXO oscillator (assembly option)
- Base board Ethernet Switch (IEEE1588) (assembly option)
- If mounted: **NAT-MCH-G4-HUB-EX**, **-HUB-Px52**, or **-HUB-Px84 HUB** modules

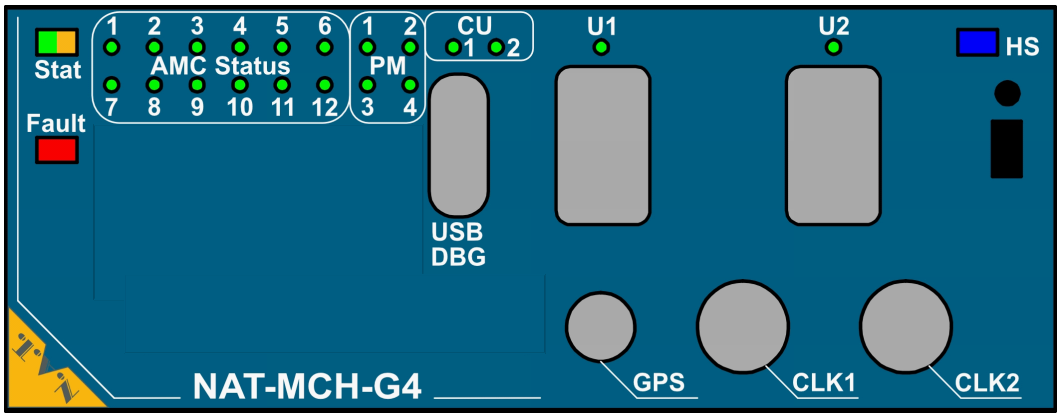
6.1.2. Clock Multiplexers

The **NAT-MCH-G4-CLKT** provides three low-jitter M-LVDS clock multiplexers connected to CLK1, CLK2, and CLK3 for each AMC.

6.2. Front Panel Connectivity

The **NAT-MCH-G4-CLKT** offers several interfaces at the front panel which are described below.

Figure 12 – Front Panel NAT-MCH-G4 Base Board with iX Front Uplink / Clock Mezzanine



Please note: The appearance of the front panel differs depending on the chosen base board uplink. Nevertheless, the clock interfaces are the same for all three variants, so this drawing with the iX interface is exemplary for all options.

6.2.1. Clock I/O

Clock IN and OUT signals are available at the front panel via SMA connectors. The maximum frequency is limited as per MTCA.0 spec to 100MHz.

The following table provides input clock parameters:

Table 5 – Input Clock Parameters

Measurement	AC Coupling	DC Coupling
Minimum frequency for symmetrical sine or square wave	1 Hz @ 500mVpp	1Hz @ 2 Vpp (2 V high, 0 V low)
Maximum frequency for symmetrical sine or square wave	200 MHz @ 1Vpp	200 MHz @ (2 V high, 0 V low)
Pulse 1PPS	1Vpp (1V high, 0V low, into 50R load), 100µs high pulse-duration	1Vpp (1V high, 0V low, 50R load), 100µs high pulse-duration
Steady high or low	n/a	1Vpp (1V high, 0V low, into 50R load)

When using DC coupling, the input signals must be between 0 V and 3.3 V. Square wave or pulse signals are recommended to get clear and consistent rising edges.

6.2.2. Jitter

All jitter measurements are done using a Lecroy SDA 813Zi Oscilloscope. For the Front-I/O channels, a 100MHz clock is generated by a UNI-T UTG4202A Waveform Generator

The total peak-to-peak-jitter is then measured at different stages of the board, as well as directly on the UTG4202A, to quantify the impact of the different components on the total jitter.

Table 6 – Jitter Measurement

Measurement	Total Jitter (ps)	Added Jitter (ps)
UTG4202A Waveform Generator	25 (@ 100MHz)	-
Signal routed from FIO to TCLKA/TCLKB	33	22
TCLKA/TCLKB generated locally by the PLL	45	

6.2.3. GPS

GPS IN is available within the precision timing assembly option. Via the SMC interface at the front panel, a standard GPS antenna signal is fed directly into the **NAT-MCH-G4**.

6.3. Backplane Connectivity

At the backplane, the **NAT-MCH-G4-CLKT** provides CLK1, CLK2, and CLK3 to all AMCs in the system. CLK1, CLK2, and/or CLK3 can be generated locally on the clock module or by any AMC in the system.

6.4. User Guide

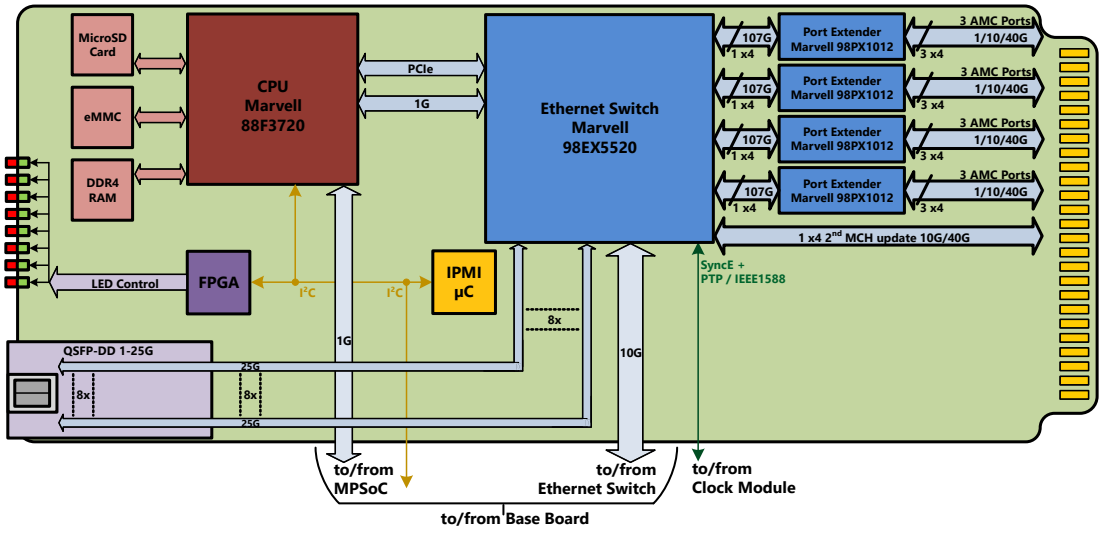
For a detailed description of the **NAT-MCH-G4-CLKT**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

7. NAT-MCH-G4-HUB-EX

7.1. Functional Description

The **NAT-MCH-G4-HUB-EX** module features various FatPipe Ethernet options to the AMCs as well as an additional uplink at the front panel. Details can be found in the following chapters.

Figure 13 – Block Diagram NAT-MCH-G4-HUB-EX Module



7.1.1. Marvell Fat-Pipe Ethernet Switch

The **NAT-MCH-G4-HUB-EX** is equipped with the latest generation Marvell Armstrong 98EX5520 Ethernet fat pipe switch.

7.2. Front Panel Connectivity

The **NAT-MCH-G4-HUB-EX** offers a QSFP-DD front uplink with 8x 1-25G.

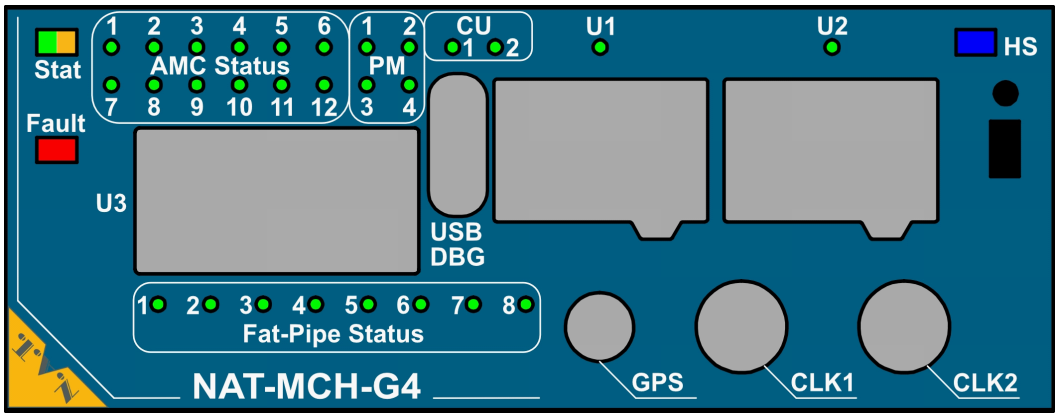
Two configuration options are possible:

- 2 x4 ports with up to 100GbE
- 8 x1 ports with up to 25GbE

Depending on the desired application, the customer can select between several standards by choosing an appropriate transceiver type:

- Optical Short Range for 100–300m
- Optical Long Range for 2–40km
- Copper

Figure 14 – Front Panel NAT-MCH-G4 Base Board with SFP(-DD) Front Uplink / Clock Mezzanine / HUB Module



Please note: The appearance of the front panel differs depending on the chosen base board uplink. All HUB Modules have the same front panel layout, so this drawing with the SFP(-DD) interface is exemplary for all three base board variants.

The functionality of the Fat-Pipe Status LEDs is described in the following table.

Table 7 – LED Functionality NAT-MCH-G4 Base Board / Clock Mezzanine / HUB Module

LED	Color	Function	Control / Description
Fat-Pipe Status LED 1-8	Green	ON / OFF	Controlled by HUB Module
	Red		

7.3. Backplane Connectivity

At the backplane, the **NAT-MCH-G4-HUB-EX** provides a 10GbE and a 40GbE infrastructure.

For a 10GbE infrastructure, the mezzanine features 12 x4 lanes @ 2.5GbE (in total 10GbE per AMC), for a 40GbE infrastructure even 12 x4 lanes @10GbE (in total 40GbE per AMC).

So different configuration options are possible:

- x4 ports with 40GbE to each AMC
- x4 ports with 10GbE (XAUI) to each AMC
- 4 x1 ports with 1-10G to each AMC

The protocol can be set for each AMC independently.

Additionally, the **NAT-MCH-G4-HUB-EX** provides a 10GbE / 40GbE update to an optional 2nd **NAT-MCH-G4** (no XAUI).

7.4. User Guide

For a detailed description of the **NAT-MCH-G4-HUB-EX**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

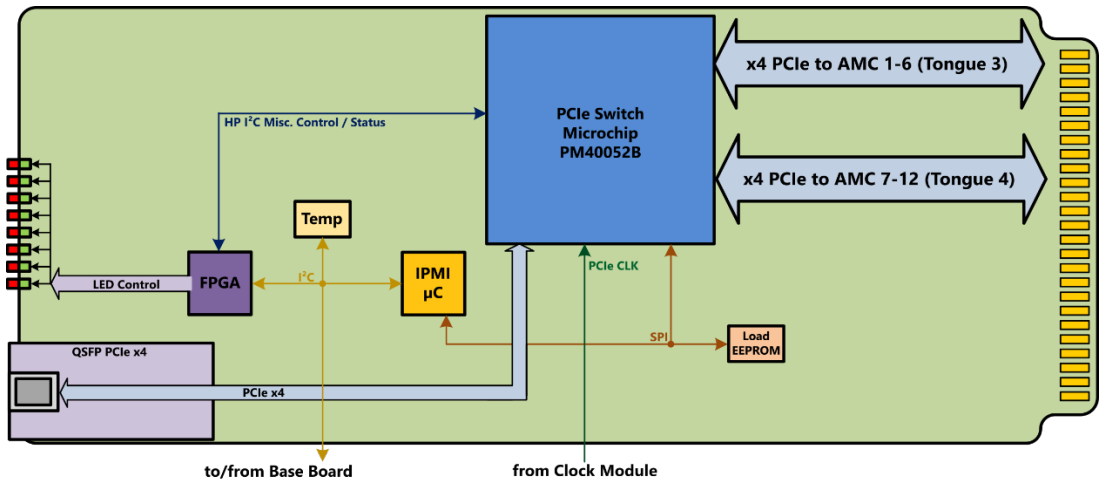
8. NAT-MCH-G4-HUB-Px52

8.1. Functional Description

The single-width **NAT-MCH-G4-HUB-Px52** PCIe module offers PCIe Gen4 switching to each AMC and a QSFP-based PCIe Gen4 x4 uplink at the front panel.

The HUB module can be operated on both base board variants.

Figure 15 – Block Diagram NAT-MCH-G4-HUB-Px52 Module



8.1.1. Microchip PCIe Switch

The **NAT-MCH-G4-HUB-Px52** is equipped with a latest generation Microchip PM40052B PCIe fat pipe switch supporting 52 lanes.

The PCIe switch can be partitioned, so that multiple PCIe domains can operate in parallel within a single MTCA system. Furthermore, non-transparent bridges can be configured to implement complex systems with multiple root-complexes through PrAMCs.

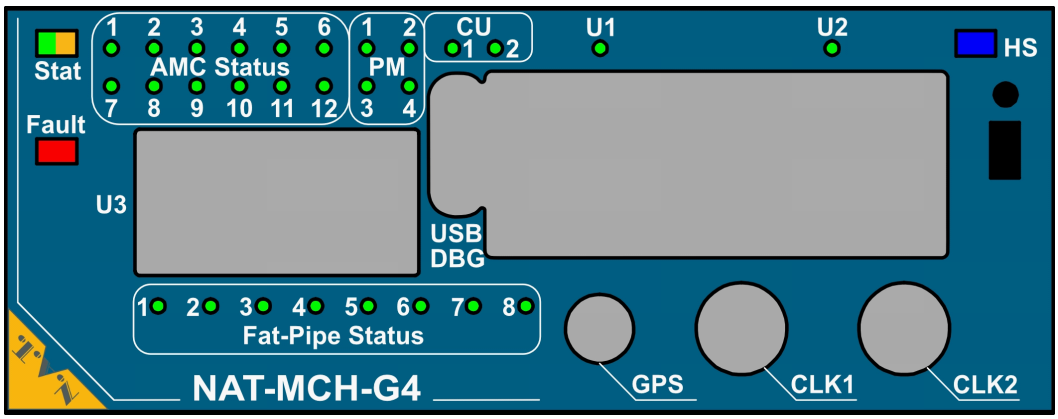
8.1.2. Clocking

In combination with the appropriate Clock Module option, a PCIe reference clock is provided to the **NAT-MCH-G4-HUB-Px52**.

8.2. Front Panel Connectivity

The **NAT-MCH-G4-HUB-Px52** offers a QSFP-based PCIe Gen4 x4 front uplink.

Figure 16 – Front Panel NAT-MCH-G4 Base Board with RJ45 Front Uplink / Clock Mezzanine / HUB Module



Please note: The appearance of the front panel differs depending on the chosen base board uplink. All HUB Modules have the same front panel layout, so this drawing with the RJ45 interface is exemplary for all three base board variants.

The functionality of the Fat-Pipe Status LEDs is described in the following table.

Table 8 – LED Functionality NAT-MCH-G4 Base Board / Clock Mezzanine / HUB Module

LED	Color	Function	Control / Description
Fat-Pipe Status LED 1-8	Green / Red	ON / OFF	Controlled by HUB Module

8.3. Backplane Connectivity

The PCIe switch of the **NAT-MCH-G4-HUB-Px52** HUB module features PCIe Gen4 switching to 12 AMCs in the system.

By standard, x4 links are provided to all 12 AMCs, but if supported by the backplane, x8 links are possible for up to six AMCs.

8.4. User Guide

For a detailed description of the **NAT-MCH-G4-HUB-Px52**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

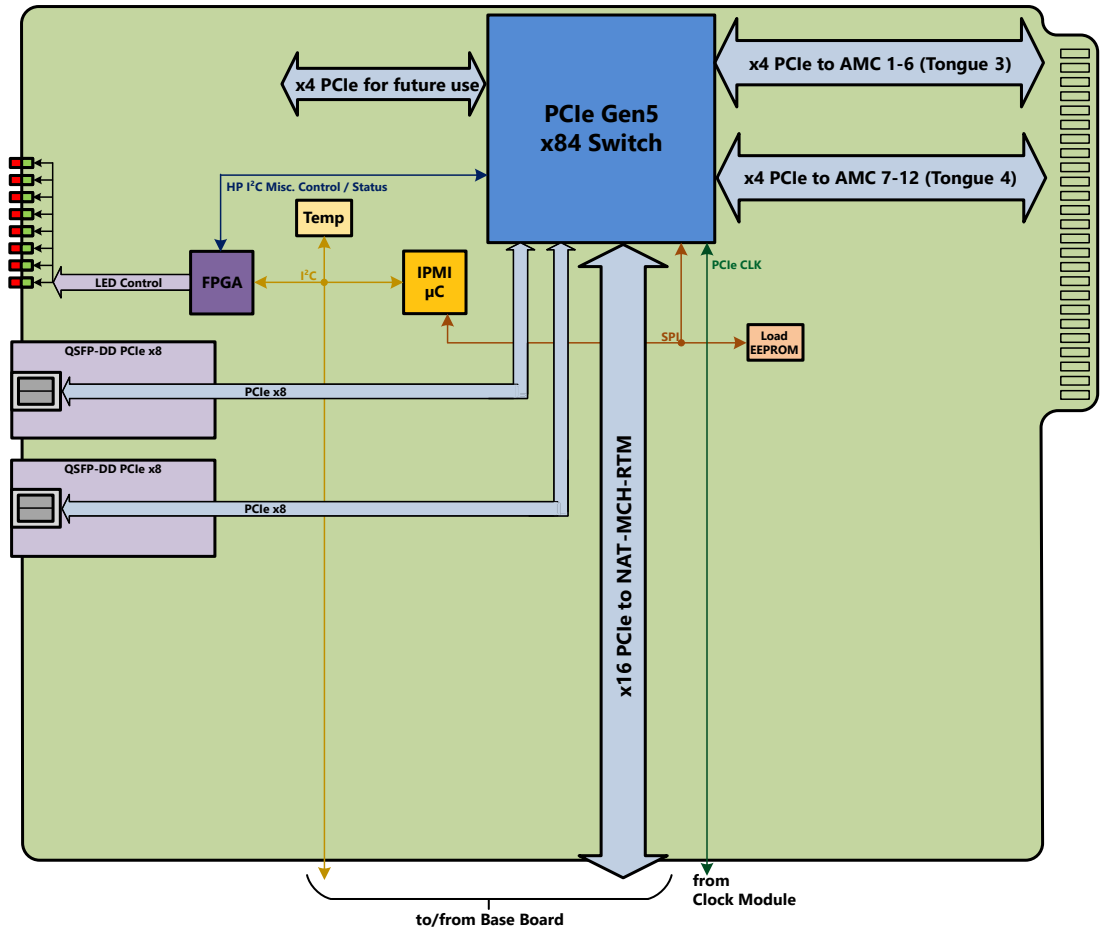
9. NAT-MCH-G4-HUB-Px84

The double-width **NAT-MCH-G4-HUB-Px84** PCIe HUB module offers PCIe Gen5 switching to each AMC. Moreover, it features one or two QSFP-DD based PCIe Gen5 x4 x8 front panel uplinks; two x8 uplinks can be combined to one x16 uplink. Please consider that the PCIe transmission standard depends on the transceiver type.

As an option, a PCIe Gen5 x16 link is available to an optional **NAT-MCH-RTM**. The connection is realized via the Zone3 connector of the **NAT-MCH-S4** base board.

Due to its double-width form factor, the HUB module can be operated on the **NAT-MCH-S4** base board variant only.

Figure 17 – Block Diagram NAT-MCH-G4-HUB-Px84 Module



9.1. Microchip Switchtec PFX PCIe Switch

The **NAT-MCH-G4-HUB-Px84** is equipped with a Microchip Switchtec PFX PCIe Gen5 switch supporting 84 lanes.

The PCIe switch can be partitioned, so that multiple PCIe domains can operate in parallel within a single MTCA system. Further, non-transparent bridges can be configured to implement complex systems with up to four independent root-complexes through PrAMCs.

Four lanes of the PCIe switch are reserved for future use e.g., operation of an M.2 interface or the MTCA NextGen standard.

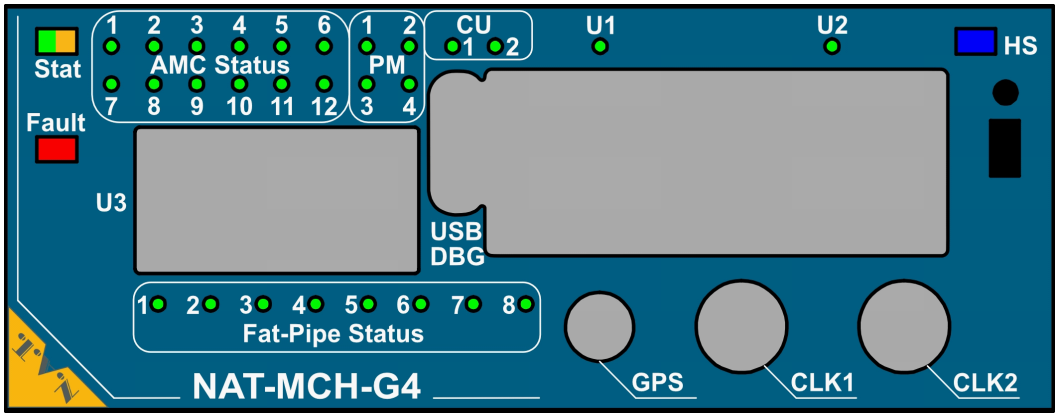
9.2. Clocking

In combination with the appropriate Clock Module option, a PCIe reference clock is provided to the **NAT-MCH-G4-HUB-Px84**.

9.3. Front Panel Connectivity

The **NAT-MCH-G4-HUB-Px84** owns two QSFP-DD interfaces with PCIe Gen5 x8 connectivity. Both uplinks can either be operated separately or can be combined to one PCIe Gen5 x16 uplink. Please consider that the PCIe transmission standard depends on the transceiver type.

Figure 18 – Front Panel NAT-MCH-G4 Base Board with RJ45 Front Uplink / Clock Mezzanine / HUB Module



Please note: The appearance of the front panel differs depending on the chosen base board uplink. All HUB Modules have the same front panel layout, so this drawing with the RJ45 interface is exemplary for all three base board variants.

The functionality of the Fat-Pipe Status LEDs is described in the following table.

Table 9 – LED Functionality NAT-MCH-G4 Base Board / Clock Mezzanine / HUB Module

LED	Color	Function	Control / Description
Fat-Pipe Status LED 1-8	Green	ON / OFF	Controlled by HUB Module
	Red		

9.4. Backplane Connectivity

The PCIe switch of the **NAT-MCH-G4-HUB-Px84** HUB module features PCIe Gen5 switching to 12 AMCs in the system.

By standard, x4 links are provided to all 12 AMCs, but if supported by the backplane, x8 links are possible for up to six AMCs.

9.5. User Guide

For a detailed description of the **NAT-MCH-G4-HUB-Px84**, please refer to the module's User Guide (see chapter 10.1 Internal Reference Documentation).

10. SPECIFICATIONS AND COMPLIANCES

10.1. Internal Reference Documentation

- **NAT-MCH-G4** User Guide
- **NAT-MCH-G4** Quick Start Guide
- **NAT-MCH-G4** Uplink Guide
- **NAT-MCH-G4** CLI
- **NAT-MCH-G4-CLKP** User Guide
- **NAT-MCH-G4-HUB-EX** User Guide will be available soon
- **NAT-MCH-G4-HUB-Px52** User Guide will be available soon
- **NAT-MCH-G4-HUB-Px84** User Guide will be available soon

Please visit our website for the latest documentation

10.2. Standards Compliance

- MTCA.0
- MTCA.4
- MTCA.4.1
- AMC.0
- AMC.1
- AMC.2
- AMC.3
- AMC.4
- IMPI V1.5
- HPM.1
- RoHS
- REACH
- CE

10.3. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

10.4. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

10.5. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

10.6. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

10.7. Abbreviation List

Table 10 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
BIOS	Basic Input/Output System
COM Express	Computer-On-Module Express
DDI	Dual Display Interface
EEPROM	Electrically Erasable PROM
EMC	Electromagnetic Compatibility
FLASH	Non-Volatile Memory
GbE	Gigabit Ethernet
HCSL	High Speed Current Steering Logic
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
LTE	Long Term Evolution
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
MMC	Module Management Controller
NVMe	Non-Volatile Memory Express
PCI(e)	Peripheral Component Interconnect (Express)
PrAMC	Processor AMC
(P)ROM	(Programmable) Read Only Memory
SATA	Serial Advanced Technology Attachment
SD-Card	Secure Digital Memory Card
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SSD	Solid State Drive
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WiFi	Wireless Fidelity – wireless network

11. DOCUMENT'S HISTORY

Table 11 – Document's History

Rev	Date	Description	Author
1.0	14.12.2023	• Initial Release	Se
1.1	16.10.2024	• Reworked	HK
1.2	27.11.2024	• Updated Block Diagrams and Front Panel Drawings • Reworked Chapter 5 NAT-MCH-G4-CLKP – Clock Mezzanine • Deleted chapter "Recovery Switch" • Editorial changes • Rearrangement of chapters due to clarity	Se
1.3	28.11.2024	• Updated chapter 4.3.1 Front Ethernet Uplink Option #1: SFP(-DD)	Se
1.4	06.02.2025	• Reworked document	Se
1.5	14.04.2025	• Reworked sections regarding PCIe HUB modules incl. board labelling • Minor corrections	Se
1.6	24.11.2025	• Editorial changes for clarification • Typo corrections • Detailed naming of clock module • Added Table 3 – Input Clock Parameters	se
	01.12.2025	• Updated CLK Module Jitter Measurements in Table 3 – Input Clock Parameters and Table 4 – Jitter Measurement	Ak
	08.12.2025	• Added title photo	Se
1.7	08.05.2026	• Added **NAT-MCH-SCIxE** • Detailed Clock Module variants • Editorial changes for clarification	Se
1.8	28.05.2026	• Minor changes (e.g. for clarification, typo corrections, or editorial changes) • added chapter 3.4 Connections to CLK I/O and GPS	se