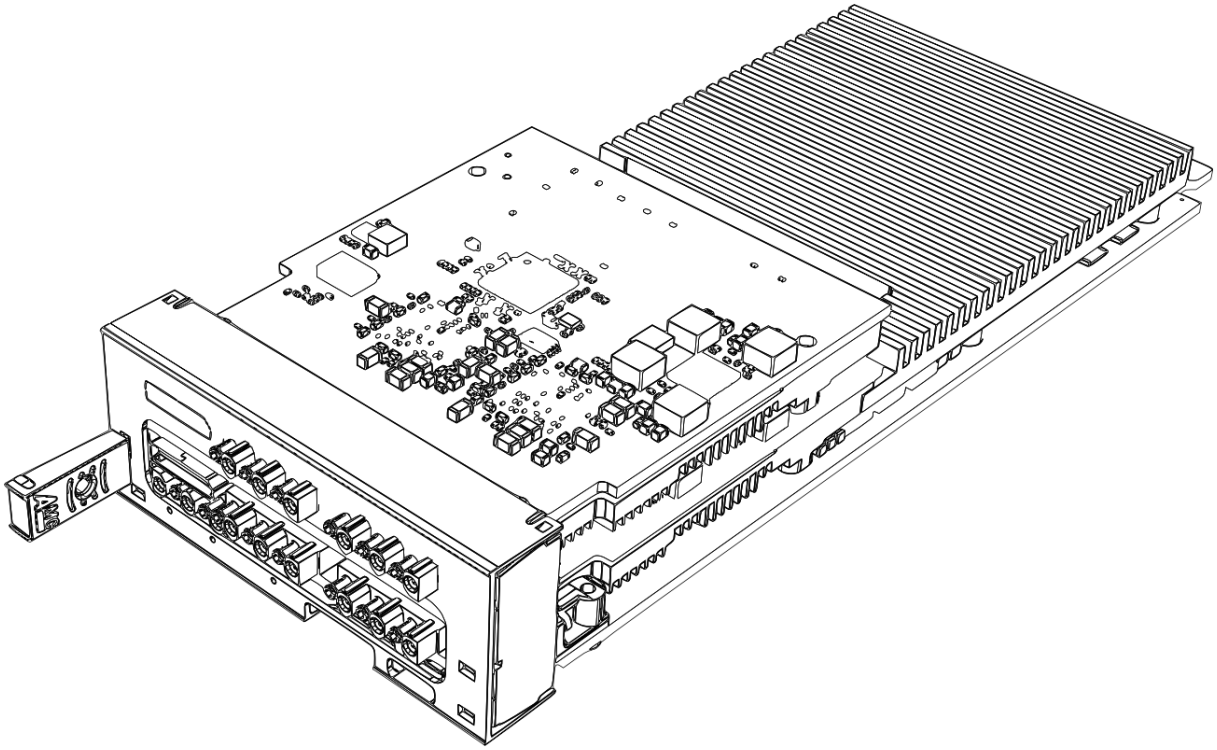
NAT-FMC-SDR4

FMC MEZZANINE BOARD

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.3

HW REVISION 1.3

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1. PREFACE

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1.2. About This Document

This document is intended to give an overview on the **NAT-FMC-SDR4's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-FMC-SDR4's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-FMC-SDR4** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-FMC-SDR4's** main features

Hardware

Description of the connectors, switches, and LEDs located on the **NAT-FMC-SDR4**

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document and standards, the **NAT-FMC-SDR4** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-FMC-SDR4** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-FMC-SDR4** is a mezzanine board in FMC form factor with integrated hardware elements, which make it the ideal platform for sophisticated wireless, machine vision, and SDR applications.

One or two of these mezzanines can be mounted on a **NAT-AMC-ZYNQUP-FMC** carrier board. This combination – named **NAT-AMC-ZYNQUP-SDR4** (one FMC, standard) or **NAT-AMC-ZYNQUP-SDR8** (two FMCs, option) – offers the flexibility to address a broad range of applications.

Important: For *4* RX/TX interfaces, one **NAT-FMC-SDR4-T** (Top) mezzanine board needs to be installed. For *8* RX/TX interfaces, one **NAT-FMC-SDR4-M** (Mid) *and* one **NAT-FMC-SDR4-T** (Top) mezzanines are mandatory.

Both FMCs are built up similar, differences are explained in the relevant sections.

2.1. Wireless Applications

Due to its powerful FPGA for baseband processing (using **NAT-AMC-ZYNQUP-FMC** as base board) and the flexible RF-frontend on the FMCs, the **NAT-AMC-ZYNQUP-SDR4/8** is ideal for Software Defined Radio applications.

The on-board JESD204B clocking simplifies the integration of high-speed ADC/DAC FMCs.

Inputs for reference clock, sync, trigger, and 1pps signals enable multi-board baseband and RF-phase synchronization for massive MIMO and phased antenna arrays.

2.2. Main Features

Table 1 – Technical Data

Form Factor		
	NAT-FMC-SDR4-M	**NAT-FMC-SDR4-T**

	• FMC Mezzanine Board
	  • Width: 69.0mm, depth: 81.1mm
	• In combination with **NAT-AMC-ZYNQUP-FMC**: Single-wide, Full-size AMC
	  • Width: 73.5mm, depth: 180.6mm	

Processing Resources		
	• On carrier board **NAT-AMC-ZYNQUP-FMC**	
RF-Interface		
	• 2x Analog Devices ADRV9009 RF Transceiver	
Clock		
	• -	• Analog Devices HMC7044 with JESD204B • 19.2MHz oscillator • 122.88MHz oscillator
FMC Slot(s)		
	• 2 FMC slots (male/female) to connect to carrier board / Top-FMC	• 1 FMC slot (male) to connect to carrier board or Mid-FMC
Backplane Interconnect		
	• Via carrier board **NAT-AMC-ZYNQUP-FMC**	
Front Panel *(including NAT-AMC-ZYNQUP-FMC carrier board)*		

	• 4x Tx, 4x Rx, 4x ORx
	• GPIO RF-Control
	  • 2x 7 GPIO 1V8 to RF Transceiver
	  • 2x 3 GPIO 3V3 to RF Transceiver
	  • 6x GPIO 1V8 to FPGA
	• *CLK OUT*
	• *CLK IN (JESD204b)*
	• *SYNC for JESD204b*
	• *PPS IN*
	• *Trigger IN/OUT to FPGA*
	• *SD card holder*
	• *UART-USB serial console for ARM core and MMC*
	• *AMC standard LEDs and hot swap handle*
	• *Application LEDs*	

Compliance		
	• AMC.0 R2.0, AMC.1, AMC.2, AMC.3, AMC.4, IMPI V1.5, HPM.1 • RoHS • VITA 57.1	
Environmental		
Operating Environment	• 0 to +55 degrees Celsius (extended temperature range on request) • Humidity: 5% to 95% (non-condensing) • Temperature of the ADRV9009 RF Transceivers may not exceed 110°C!	
Storage Environment	• -40 to +100 degrees Celsius • Humidity: 5% to 95% (non-condensing)	

3. QUICK START

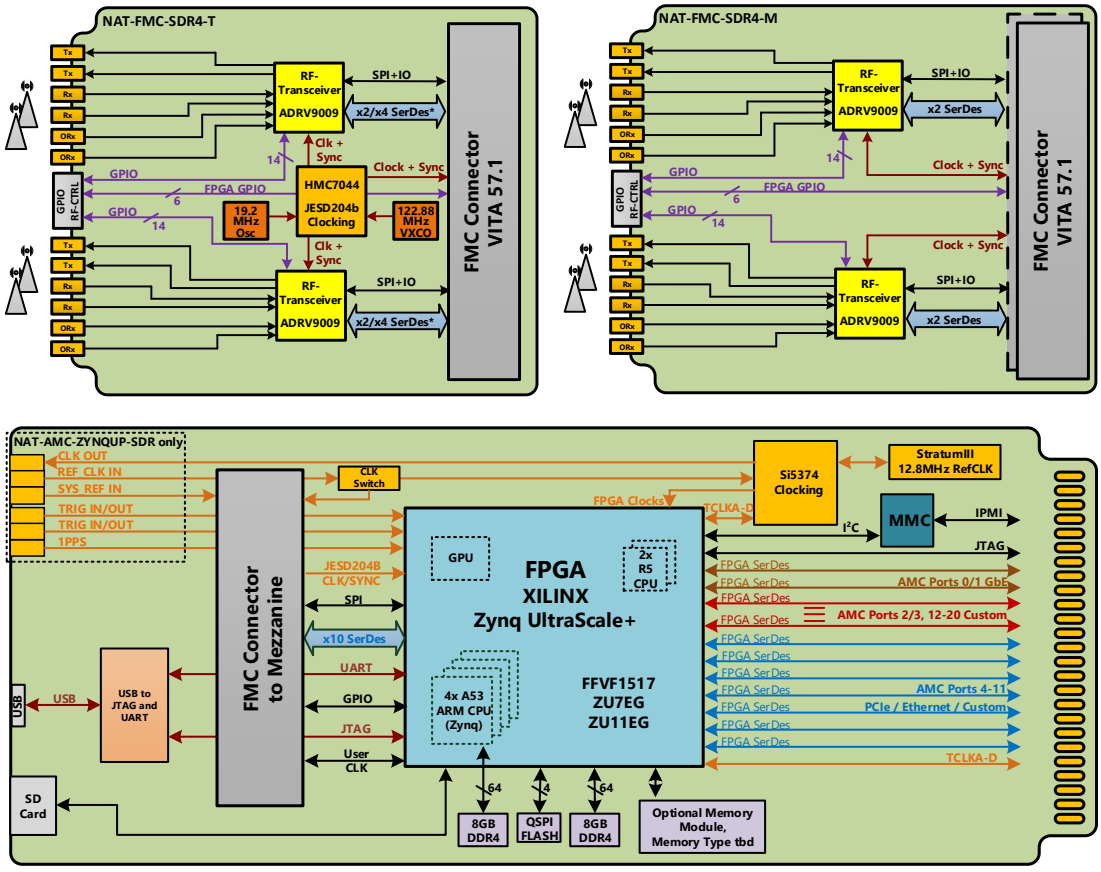
For bring-up information, please refer to the **NAT-AMC-ZYNQUP-FMC** Technical Reference Manual (see chapter 6.1 Internal Reference Documentation for details).

4. FUNCTIONAL DESCRIPTION

The **NAT-FMC-SDR4** can be divided into a number of functional blocks, which are described in the following paragraphs.

As the **NAT-FMC-SDR4** is intended to be operated with the **NAT-AMC-ZYNQUP-FMC** carrier only, the following figure gives an overview on the functional blocks of the whole combination.

Figure 1 – Block Diagram



Note: The number of available SerDes connections per RF-Transceiver varies with the number of installed FMCs. Equipped with two FMCs (**NAT-AMC-ZYNQUP-SDR8** option), each FMC owns four SerDes connections, ***two*** for every RF-Transceiver. If only one FMC is mounted (**NAT-AMC-ZYNQUP-SDR4** option), a total of eight SerDes connections is available on one FMC, which means ***four*** for every RF-Transceiver.

4.1. RF-Transceiver

Both variants of the **NAT-FMC-SDR4** feature two Analog Devices ADRV9009 transceiver units. Every transceiver offers two transmitter-, two receiver-, and two observation receiver-interfaces.

Table 2 – Key Data RF-Transceivers

Parameter	Value
Maximum receiver bandwidth	200 MHz
Maximum tuneable transmitter synthesis bandwidth	450 MHz
Maximum observation receiver bandwidth	450 MHz
Multichip phase synchronization for RF- and baseband signals	Supported
Multiboard synchronization	Supported
JESD204B IQ sample data interface to FPGA	Supported
Tuning range (center frequency)	75 MHz to 6000 MHz
RX gain range	30dB in 0.5dB steps
Rx Noise Figure	2dB @ 800 MHz 3dB @ 2.4 GHz 3.8 dBm @ 5.5 GHz
Maximum output power	9 dBm @ 75 MHz < f ≤ 600 MHz 7 dBm @ 600 MHz < f ≤ 4000 MHz 6 dBm @ 4000 MHz < f ≤ 4800 MHz 4.5 dBm @ 4800 MHz < f ≤ 6000 MHz
Tx Error Vector Magnitude (EVM)	0.5% @ 75 MHz LO 0.7% @ 1900 MHz LO 0.7% @ 3800 MHz LO 1.1% @ 5900 MHz LO
3rd order output intermodulation OIP3	23 dBm @ 800 MHz 19 dBm @ 2.4 GHz 17 dBm @ 5.5 GHz

Important: The temperature of the ADRV9009 RF transceiver may not exceed 110°C!

4.2. Clocking (NAT-FMC-SDR4-T only)

The **NAT-FMC-SDR4-T** features an Analog Devices HMC7044 device, which offers JESD204b interfaces.

A 19.2MHz oscillator and a 122.88MHz VXCO are connected to the clock device.

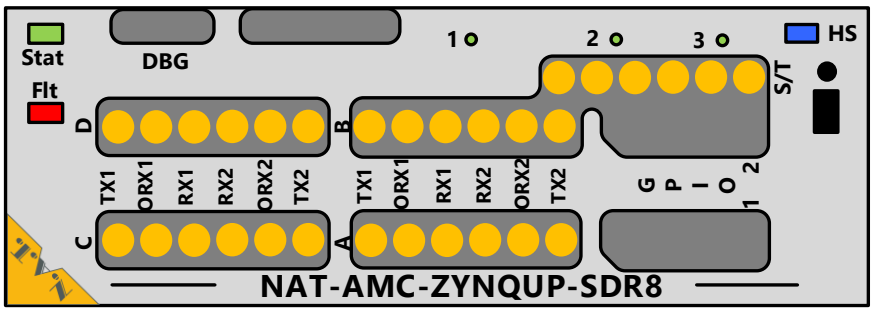
5. HARDWARE

5.1. Front Panel and LEDs

The front plate appearance and the labelling vary depending on the number and variant(s) of installed FMCs.

The figure below shows the full-size version, the **NAT-AMC-ZYNQUP-SDR8**, which is fully equipped with two FMCs.

Figure 2 – Front Panel NAT-AMC-ZYNQUP-SDR8



The LEDs, debug interface, and SD-Card holder are accessible via the **NAT-AMC-ZYNQUP-FMC**. Please check the carrier board's Technical Reference Manual for details (refer to 6.1 Internal Reference Documentation).

5.2. Component-, Connector-, and Switch-Location

Figure 3 – NAT-FMC-SDR4-T Location Diagram – Top

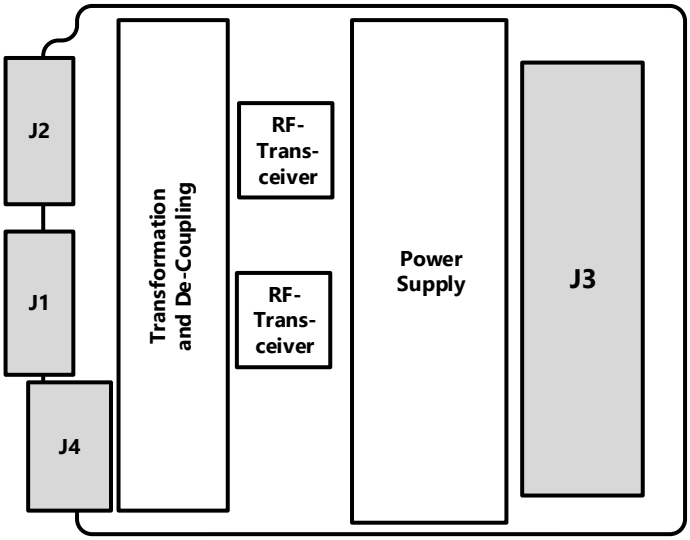


Figure 4 – NAT-FMC-SDR4-T Location Diagram – Bottom

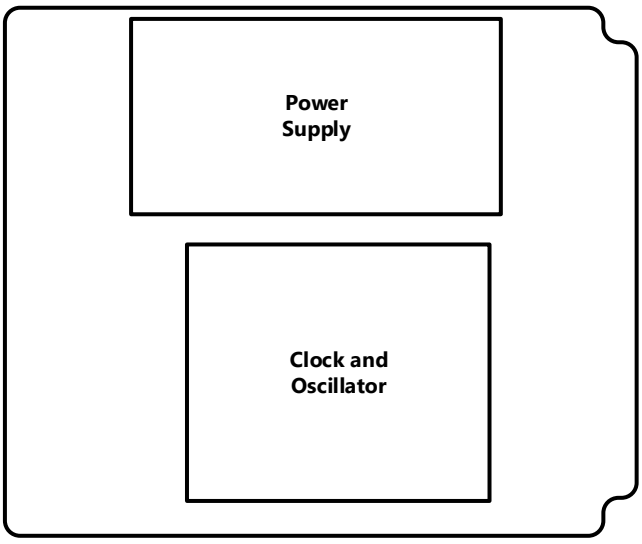


Figure 5 – NAT-FMC-SDR4-M Location Diagram – Top

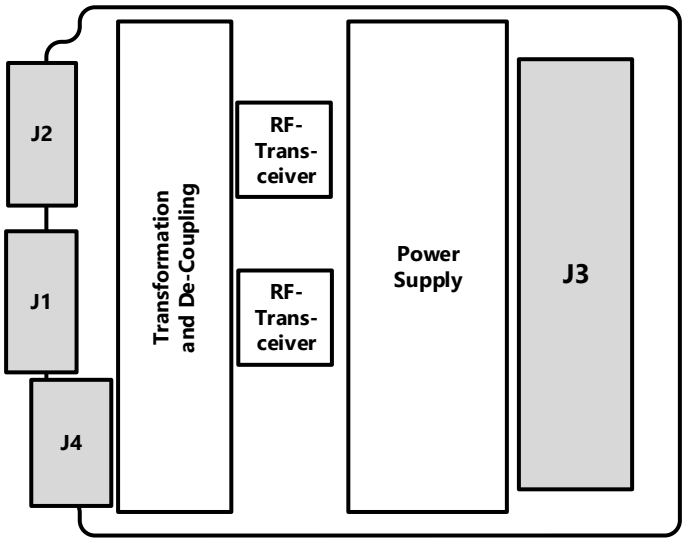
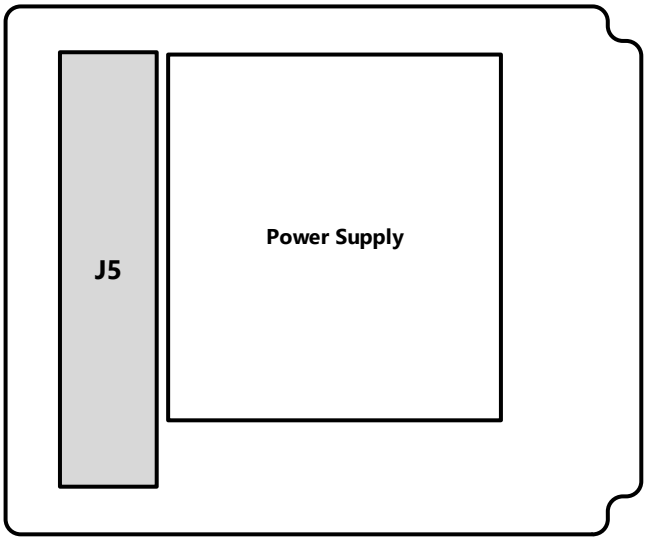


Figure 6 – NAT-FMC-SDR4-M Location Diagram – Bottom



Connectors on top side: drawings imply the board is orientated with the front panel interfaces to the left side

Connectors on bottom side: drawings imply the board is orientated with the front panel interfaces to the right side

Please refer to the following tables to look up the connector pin assignment of the **NAT-FMC-SDR4**.

5.2.1. J1/J2: Multi-Coax Connectors

Connectors J1 and J2 offer access to the RF-transceiver interfaces towards the front panel with the signals routed via the pins and ground connected to the shield.

Note: An associated cable set is available as order option.

Figure 7 – J1/J2: Multi-Coax Connectors

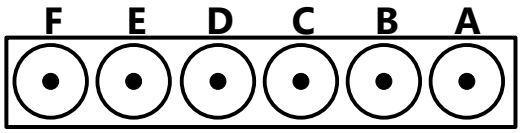


Table 3 – J1/J2: Multi-Coax Connectors – Pin Assignment

Pin #	Signal	Signal	Pin #
J1A	TX2_OUT_A	TX2_OUT_B	J2A
J1B	ORX2_IN_A	ORX2_IN_B	J2B
J1C	RX2_IN_A	RX2_IN_B	J2C
J1D	RX1_IN_A	RX1_IN_B	J2D
J1E	ORX1_IN_A	ORX1_IN_B	J2E
J1F	TX1_OUT_A	TX1_OUT_B	J2F

5.2.2. J3: FMC Connector (NAT-FMC-SDR4-M)

Connector J3 connects the FMC to the carrier board.

Table 4 – J3: FMC Connector NAT-FMC-SDR4-M

	A	B	C	D	E	F	G	H	J	K
1	GND	GND	GND	FMC_PWR_EN	GND	nc	GND	nc	GND	nc
2	DP1_M2C_P	GND	DP0_C2M_P	GND	nc	GND	CLK1_M2C_P	GND	CLK3_BIDIR_P	GND
3	DP1_M2C_N	GND	DP0_C2M_N	GND	nc	GND	CLK1_M2C_N	GND	CLK3_BIDIR_N	GND
4	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND	HA00_P_CC	GND	CLK0_M2C_P	GND	CLK2_BIDIR_P
5	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND	HA00_N_CC	GND	CLK0_M2C_N	GND	CLK2_BIDIR_N
6	SERDOUT0_A_P	GND	DP0_M2C_P	GND	SYNCIN1_A_P	GND	LA00_P_CC	GND	nc	GND
7	SERDOUT0_A_N	GND	DP0_M2C_N	GND	SYNCIN1_A_N	HA04_P	LA00_N_CC	LA02_P	nc	GP_INTERRUPT_A
8	GND	DP8_M2C_P	GND	LA01_P_CC	GND	HA04_N	GND	LA02_N	GND	RX1_ENABLE_A
9	GND	DP8_M2C_N	GND	LA01_N_CC	SYNCIN0_A_P	GND	LA03_P	GND	nc	GND
10	SERDOUT1_A_P	GND	LA06_P	GND	SYNCIN0_A_N	HA08_P	LA03_N	LA04_P	nc	RX2_ENABLE_A
11	SERDOUT1_A_N	GND	LA06_N	LA05_P	GND	HA08_N	GND	LA04_N	GND	TX1_ENABLE_A

	A	B	C	D	E	F	G	H	J	K
12	GND	SERDOUT1_B_P	GND	LA05_N	SYNCOUT0_A_P	GND	LA08_P	GND	nc	GND
13	GND	SERDOUT1_B_N	GND	GND	SYNCOUT0_A_N	SPI_SDIO_A	LA08_N	LA07_P	nc	nc
14	DP4_M2C_P	GND	LA010_P	LA09_P	GND	SPI_SDO_A	GND	LA07_N	GND	nc
15	DP4_M2C_N	GND	LA010_N	LA09_N	SYNCOUT1_A_P	GND	LA12_P	GND	nc	GND
16	GND	SERDOUT0_B_P	GND	GND	SYNCOUT1_A_N	SPI_CS_A	LA12_N	LA11_P	nc	nc
17	GND	SERDOUT0_B_N	GND	LA13_P	GND	SPI_SCLK_A	GND	LA11_N	GND	nc
18	DP5_M2C_P	GND	LA14_P	LA13_N	SYNCOUT0_B_P	GND	LA16_P	GND	SYNCOUT1_B_P	GND
19	DP5_M2C_N	GND	LA14_N	GND	SYNCOUT0_B_N	SPI_CS_B	LA16_N	LA15_P	SYNCOUT1_B_N	GPIO_11_1V8_A
20	GND	GBTCLK1_M2C_P	GND	LA17_P_CC	GND	SPI_SCLK_B	GND	LA15_N	GND	GPIO_13_1V8_A
21	GND	GBTCLK1_M2C_N	GND	LA17_N_CC	SYNCIN0_B_P	GND	LA20_P	GND	SYNCIN1_B_P	GND
22	DP1_C2M_P	GND	LA18_P_CC	GND	SYNCIN0_B_N	nc	LA20_N	LA19_P	SYNCIN1_B_N	nc
23	DP1_C2M_N	GND	LA18_N_CC	LA23_P	GND	nc	GND	LA19_N	GND	nc
24	GND	DP9_C2M_P	GND	LA23_N	GPIO_14_1V8_A	GND	LA22_P	GND	FPGA_GPIO_2_1V8_A	GND
25	GND	DP9_C2M_N	GND	GND	GPIO_15_1V8_A	nc	LA22_N	LA21_P	FPGA_GPIO_3_1V8_A	nc
26	SERDIN0_A_P	GND	LA27_P	LA26_P	GND	nc	GND	LA21_N	GND	nc
27	SERDIN0_A_N	GND	LA27_N	LA26_N	RESET_N_A	GND	LA25_P	GND	FPGA_GPIO_4_1V8_A	GND
28	GND	DP8_C2M_P	GND	GND	TX2_ENABLE_	GPIO_10_1V8	LA25_N	LA24_P	FPGA_GPIO_	nc

	A	B	C	D	E	F	G	H	J	K
					A	_B			0_1V8_A	
29	GND	DP8_C2M_N	GND	nc	GND	GPIO_12_1V8_B	GND	LA24_N	GND	nc
30	SERDIN1_A_P	GND	FMC_SCL	nc	GPIO_8_1V8_A	GND	LA29_P	GND	GP_INTERRUPT_B	GND
31	SERDIN1_A_N	GND	FMC_SDA	nc	GPIO_9_1V8_A	GPIO_9_1V8_B	LA29_N	LA28_P	RESET_N_B	GPIO_15_1V8_A
32	GND	SERDIN1_B_P	GND	3P3VAUX	GND	GPIO_10_1V8_B	GND	LA28_N	GND	GPIO_14_1V8_A
33	GND	SERDIN1_B_N	GND	nc	FPGA_GPIO_1_1V8_A	GND	LA31_P	GND	RX1_ENABLE_B	GND
34	DP4_C2M_P	GND	I2C_DEV_A0	nc	FPGA_GPIO_5_1V8_A	SPI_SDIO_B	LA31_N	LA30_P	RX2_ENABLE_B	GPIO_12_1V8_B
35	DP4_C2M_N	GND	FMC_12POV	I2C_DEV_A1	GND	SPI_SDO_B	GND	LA30_N	GND	GPIO_11_1V8_B
36	GND	SERDIN0_B_P	GND	FMC_3P3V	nc	GND	LA33_P	GND	TX1_ENABLE_B	GND
37	GND	SERDIN0_B_N	FMC_12POV	GND	nc	HB20_P	LA33_N	LA32_P	TX2_ENABLE_B	GPIO_13_1V8_B
38	DP5_C2M_P	GND	GND	FMC_3P3V	GND	HB20_N	GND	LA32_N	GND	GPIO_8_1V8_B
39	DP5_C2M_N	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C	GND
40	GND	nc	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C

5.2.3. J3: FMC Connector (NAT-FMC-SDR4-T)

Connector J3 connects the FMC to the carrier board or the **NAT-FMC-SDR4-M** mezzanine.

Table 5 – J3: FMC Connector NAT-FMC-SDR4-T

	A	B	C	D	E	F	G	H	J	K
1	GND	GND	GND	FMC_PWR_EN	GND	nc	GND	nc	GND	nc
2	SERDOUT1_A_P	GND	SERDIN0_A_P	GND	nc	GND	nc	GND	nc	GND
3	SERDOUT1_A_N	GND	SERDIN0_A_N	GND	nc	GND	nc	GND	nc	GND
4	GND	nc	GND	JESD_DEVCLK_E_P	GND	CLK_HMC7044_FPGA_P	GND	HMC7044_OUT10_P	GND	CLK_HMC7044_SYS_PLL_P
5	GND	nc	GND	JESD_DEVCLK_E_N	GND	CLK_HMC7044_FPGA_N	GND	HMC7044_OUT10_N	GND	CLK_HMC7044_SYS_PLL_N
6	SERDOUT2_A_P	GND	SERDOUT0_A_P	GND	nc	GND	GPIO14_1V8_A	GND	nc	GND
7	SERDOUT2_A_N	GND	SERDOUT0_A_N	GND	nc	GPIO1_HMC7044	GPIO15_1V8_A	SYNCOUT0_A_P	nc	nc
8	GND	nc	GND	JESD_SYSREF_F_P	GND	GPIO3_HMC7044	GND	SYNCOUT0_A_N	GND	nc
9	GND	nc	GND	JESD_SYSREF_F_N	nc	GND	GP_INTERRUPT_A	GND	nc	GND
10	SERDOUT3_A_P	GND	SPI_SDO_A	GND	nc	GPIO2_HMC7044	RX1_ENABLE_A	SYNCOUT1_A_P	nc	nc
11	SERDOUT3_A_N	GND	SPI_SDIO_A	GPIO8_1V8_A	GND	nc	GND	SYNCOUT1_A_N	GND	nc
12	GND	SERDOUT3_B_P	GND	GPIO4_HMC7044	nc	GND	RX2_ENABLE_A	GND	JESD_SYSREF_C_P	GND

	A	B	C	D	E	F	G	H	J	K
13	GND	SERDOUT3_B_N	GND	GND	nc	nc	TX1_ENABLE_A	SYNCIN0_A_P	JESD_SYSREF_C_PN	JESD_DEVCLK_D_P
14	SERDOUT0_B_P	GND	SPI_SCLK_A	RESET_HMC7044	GND	nc	GND	SYNCIN0_A_N	GND	JESD_DEVCLK_D_N
15	SERDOUT0_B_N	GND	SPI_CS_A	SYNC_HMC7044	nc	GND	TX2_ENABLE_A	GND	JESD_DEVCLK_C_P	GND
16	GND	SERDOUT2_B_P	GND	GND	nc	nc	RESET_N_A	SYNCIN1_A_P	JESD_DEVCLK_C_N	JESD_SYSREF_D_P
17	GND	SERDOUT2_B_N	GND	GPIO_9_1V8_A	GND	nc	GND	SYNCIN1_A_N	GND	JESD_SYSREF_D_N
18	SERDOUT1_B_P	GND	SPI_CSn	GPIO_10_1V8_A	nc	GND	GPIO_11_1V8_A	GND	nc	GND
19	SERDOUT1_B_N	GND	SPI_CLK	GND	nc	nc	GPIO_12_1V8_A	LA15_P	nc	nc
20	GND	JESD_DEVCLK_F_P	GND	JESD_SYSREF_E_P	GND	nc	GND	LA15_N	GND	nc
21	GND	JESD_DEVCLK_F_N	GND	JESD_SYSREF_E_N	nc	GND	GPIO_12_1V8_B	GND	nc	GND
22	SERDIN1_A_P	GND	GPIO_14_1V8_A	GND	nc	nc	GPIO_11_1V8_B	FPGA_GPIO_2_1V8	nc	nc
23	SERDIN1_A_N	GND	GPIO_15_1V8_A	GPIO12_1V8_B	GND	nc	GND	FPGA_GPIO_3_1V8	GND	nc
24	GND	nc	GND	GPIO13_1V8_B	nc	GND	GP_INTERRUPT_B	GND	nc	GND
25	GND	nc	GND	GND	nc	nc	RESET_N_B	FPGA_GPIO_4_1V8	nc	nc
26	SERDIN2_A_P	GND	SPI_SDO_B	TX1_ENABLE_B	GND	nc	GND	FPGA_GPIO_5_1V8	GND	nc
27	SERDIN2_A_N	GND	SPI_SDIO_B	TX2_ENABLE_B	nc	GND	RX1_ENABLE_B	GND	nc	GND

	A	B	C	D	E	F	G	H	J	K
28	GND	nc	GND	GND	nc	nc	RX2_ENABLE_B	GPIO_8_1V8_B	nc	nc
29	GND	nc	GND	nc	GND	nc	GND	GPIO_9_1V8_B	GND	nc
30	SERDIN3_A_P	GND	FMC_SCL	nc	nc	GND	SPI_SCLK_B	GND	nc	GND
31	SERDIN3_A_N	GND	FMC_SDA	nc	nc	nc	SPI_CS_B	SPI_MOSI	nc	nc
32	GND	SERDIN3_B_P	GND	3P3VAUX	GND	nc	GND	GPIO_10_1V8_B	GND	nc
33	GND	SERDIN3_B_N	GND	nc	nc	GND	SYNCOUT0_B_P	GND	nc	GND
34	SERDIN0_B_P	GND	I2C_DEV_A0	nc	nc	nc	SYNCOUT0_B_N	SYNCIN1_B_P	nc	nc
35	SERDIN0_B_N	GND	FMC_12POV	I2C_DEV_A1	GND	nc	GND	SYNCIN1_B_N	GND	nc
36	GND	SERDIN2_B_P	GND	FMC_3P3V	nc	GND	SYNCOUT1_B_P	GND	nc	GND
37	GND	SERDIN2_B_N	FMC_12POV	GND	nc	FP_JESD_REFSYNC_IN	SYNCOUT1_B_N	SYNCIN0_B_P	nc	nc
38	SERDIN1_B_P	GND	GND	FMC_3P3V	GND	FP_JESD_CLK_IN	GND	SYNCIN0_B_N	GND	nc
39	SERDIN1_B_N	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C	GND
40	GND	nc	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C

5.2.4. J4: GPIO Connector

Connector J4 offers a GPIO connector interface e.g., for controlling external RF components.

Figure 8 – J4: GPIO Connector

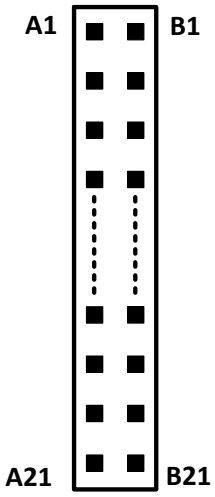


Table 6 – J4: GPIO Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	GPIO_0_3V3_A	GPIO_0_3V3_B	B1
A2	GND	GND	B2
A3	GPIO_0_1V8_A	GPIO_0_1V8_B	B3
A4	GPIO_1_1V8_A	GPIO_1_1V8_B	B4
A5	GND	GND	B5
A6	GPIO_2_1V8_A	GPIO_2_1V8_B	B6
A7	GPIO_3_1V8_A	GPIO_3_1V8_B	B7
A8	GND	GND	B8
A9	GPIO_4_1V8_A	GPIO_4_1V8_B	B9
A10	GPIO_5_1V8_A	GPIO_5_1V8_B	B10
A11	GPIO_1_3V3_A	GPIO_1_3V3_B	B11
A12	GPIO_6_1V8_A	GPIO_6_1V8_B	B12
A13	GPIO_7_1V8_A	GPIO_7_1V8_B	B13
A14	GND	GND	B14
A15	GPIO_2_3V3_A	GPIO_2_3V3_B	B15
A16	VDDA_1P8_A	FMC_3P3V	B16
A17	GND	GND	B17
A18	FPGA_GPIO_0_1V8_FP	FPGA_GPIO_3_1V8_FP	B18
A19	FPGA_GPIO_1_1V8_FP	FPGA_GPIO_4_1V8_FP	B19
A20	GND	GND	B20
A21	FPGA_GPIO_2_1V8_FP	FPGA_GPIO_5_1V8_FP	B21

5.2.5. J5: FMC Connector (NAT-FMC-SDR4-M only)

Connector J5 connects the **NAT-FMC-SDR4-M** to the **NAT-FMC-SDR4-T** mezzanine board.

Table 7 – J5: FMC Connector (NAT-FMC-SDR4-M only)

	A	B	C	D	E	F	G	H	J	K
1	GND	GND	GND	FMC_PWR_EN	GND	nc	GND	nc	GND	nc
2	DP1_M2C_P	GND	DP0_C2M_P	GND	nc	GND	CLK1_M2C_P	GND	CLK3_BIDIR_P	GND
3	DP1_M2C_N	GND	DP0_C2M_N	GND	nc	GND	CLK1_M2C_N	GND	CLK3_BIDIR_N	GND
4	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND	HA00_P_CC	GND	CLK0_M2C_P	GND	CLK2_BIDIR_P
5	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND	HA00_N_CC	GND	CLK0_M2C_N	GND	CLK2_BIDIR_N
6	100R Term.	GND	DP0_M2C_P	GND	nc	GND	LA00_P_CC	GND	nc	GND
7	100R Term.	GND	DP0_M2C_N	GND	nc	HA04_P	LA00_N_CC	LA02_P	nc	nc
8	GND	DP8_M2C_P	GND	LA01_P_CC	GND	HA04_N	GND	LA02_N	GND	nc
9	GND	DP8_M2C_N	GND	LA01_N_CC	nc	GND	LA03_P	GND	nc	GND
10	100R Term.	GND	LA06_P	GND	nc	HA08_P	LA03_N	LA04_P	nc	nc
11	100R Term.	GND	LA06_N	LA05_P	GND	HA08_N	GND	LA04_N	GND	nc
12	GND	100R Term.	GND	LA05_N	nc	GND	LA08_P	GND	JESD_SYSREF_A_P	GND
13	GND	100R Term.	GND	GND	nc	nc	LA08_N	LA07_P	JESD_SYSREF_A_N	JESD_DEVCLK_B_P
14	DP4_M2C_P	GND	LA10_P	LA09_P	GND	nc	GND	LA07_N	GND	JESD_DEVCLK_B_N

	A	B	C	D	E	F	G	H	J	K
15	DP4_M2C_P N	GND	LA10_N	LA09_N	nc	GND	LA12_P	GND	JESD_DEVCL K_A_P	GND
16	GND	100R Term.	GND	GND	nc	nc	LA12_N	LA11_P	JESD_DEVCL K_A_N	JESD_SYSREF _B_P
17	GND	100R Term.	GND	LA13_P	GND	nc	GND	LA11_N	GND	JESD_SYSREF _B_N
18	DP5_M2C_P	GND	LA14_P	LA13_N	nc	GND	LA16_P	GND	nc	GND
19	DP5_M2C_P N	GND	LA14_N	GND	nc	nc	LA16_N	LA15_P	nc	nc
20	GND	GBTCLK1_M2 C_P	GND	LA17_P_CC	GND	nc	GND	LA15_N	GND	nc
21	GND	GBTCLK1_M2 C_N	GND	LA17_N_CC	nc	GND	LA20_P	GND	nc	GND
22	DP1_C2M_P	GND	LA18_P_CC	GND	nc	nc	LA20_N	LA19_P	nc	nc
23	DP1_C2M_N	GND	LA18_N_CC	LA23_P	GND	nc	GND	LA19_N	GND	nc
24	GND	DP9_C2M_P	GND	LA23_N	nc	GND	LA22_P	GND	nc	GND
25	GND	DP9_C2M_N	GND	GND	nc	nc	LA22_N	LA21_P	nc	nc
26	DP2_C2M_P	GND	LA27_P	LA26_P	GND	nc	GND	LA21_N	GND	nc
27	DP2_C2M_N	GND	LA27_N	LA26_N	nc	GND	LA25_P	GND	nc	GND
28	GND	DP8_C2M_P	GND	GND	nc	nc	LA25_N	LA24_P	nc	nc
29	GND	DP8_C2M_N	GND	nc	GND	nc	GND	LA24_N	GND	nc
30	nc	GND	FMC_SCL	nc	nc	GND	LA29_P	GND	nc	GND
31	nc	GND	FMC_SDA	nc	nc	nc	LA29_N	LA28_P	nc	nc
32	GND	nc	GND	3P3VAUX	GND	nc	GND	LA28_N	GND	nc
33	GND	nc	GND	nc	nc	GND	LA31_P	GND	nc	GND
34	DP4_C2M_P	GND	I2C_DEV_A0	nc	nc	nc	LA31_N	LA30_P	nc	nc
35	DP4_C2M_N	GND	FMC_12POV	I2C_DEV_A1	GND	nc	GND	LA30_N	GND	nc
36	GND	nc	GND	FMC_3P3V	nc	GND	LA33_P	GND	nc	GND

	A	B	C	D	E	F	G	H	J	K
37	GND	nc	FMC_12POV	GND	nc	HB20_P	LA33_N	LA32_P	nc	nc
38	DP5_C2M_P	GND	GND	FMC_3P3V	GND	HB20_N	GND	LA32_N	GND	nc
39	DP5_C2M_N	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C	GND
40	GND	nc	GND	FMC_3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

Please find our internal reference documentation on our website by choosing the desired product or solution: https://www.nateurope.com

- **NAT-AMC-ZYNQUP-FMC**, Technical Reference Manual
- **NAT-AMC-ZYNQUP-SDR,** User's Guide
  This document is under NDA, please contact NAT

6.2. External Reference Documentation

- Analog Devices ADRV9009 Dual RF Transmitter Data Sheet, Rev. B, 05/2019
- Analog Devices HMC7044 Jitter Attenuator Data Sheet, Rev. B, 11/2016

6.3. Standards Compliance

- AMC.0 R2.0
- AMC.1
- AMC.2
- AMC.3
- AMC.4
- IMPI V1.5
- HPM.1
- VITA 57.1

6.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the

RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.6. Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

6.7. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of

the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6.8. Abbreviation List

Table 8 – Abbreviation List

Abbreviation	Description
ADC	Analog-Digital-Converter
AMC	Advanced Mezzanine Card
ARM	Processor Architecture with reduced instruction set
CPU	Central Processing Unit
DAC	Digital-Analog-Converter
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input / Output
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
MicroSD-Card	Micro Secure Digital Memory Card
MIMO	Multiple-Input and Multiple-Output
OIP	Output Intercept Point
ORx	Observation Receiver
PCB	Printed Circuit Board
RF	Radio Frequency
RX	Receiver
SDR	Software Defined Radio
Tx	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

7. DOCUMENT'S HISTORY

Table 9 – Document's History

Rev	Date	Description	Author
1.0	16.01.2020	• initial release	se
	11.02.2020	• added title foto	se
	26.08.2020	• Minor changes	Se

1.1	21.10.2020	• Added Missing pin assignment of FMC-Connector J3 for **NAT-FMC-SDR4-M**
		• Adaption to HW-Version 1.1:
		  • Omission of Connectors J5/J6
		  • Modified pin assignment of FMC-Connectors J3/J5
			Se

1.2	27.10.2021	• Updated Table 6 – J4: GPIO Connector – Pin Assignment	se
	13.06.2023	• Adaption to HW-Version V1.3	se
1.3	15.06.2023	• Corrected Table 1 – Technical Data regarding number of GPIOs	se