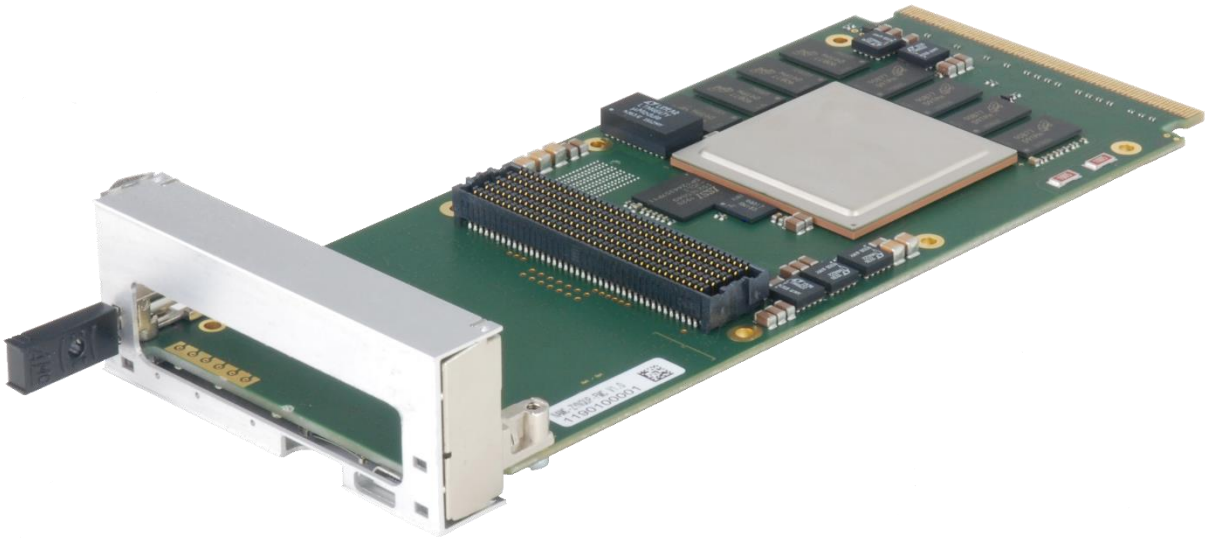
NAT-AMC-ZYNQUP-FMC

FMC CARRIER BOARD

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.3

HW REVISION 1.2

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1. PREFACE

1.1. Disclaimer

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-AMC-ZYNQUP-FMC's** functional capabilities.

Note: This Technical Reference Manual is valid for hardware version V1.2 and higher only! For prior hardware versions, please refer to Technical Reference Manual V1.0/1.1.

Preface

General information about this document

Introduction

Abstract on the **NAT-AMC-ZYNQUP-FMC's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-AMC-ZYNQUP-FMC** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-AMC-ZYNQUP-FMC's** main features

Hardware

Description of the connectors, switches, and LEDs located on the **NAT-AMC-ZYNQUP-FMC**

FMC Operation

Special information on mounting and operating a FMC module on the **NAT-AMC-ZYNQUP-FMC**

Known Issues

List of known issues of the current PCB version

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document and standards, the **NAT-AMC-ZYNQUP-FMC** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-AMC-ZYNQUP-FMC** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-AMC-ZYNQUP-FMC** is a FMC carrier board in AMC form factor with an on-board Xilinx® Zynq® UltraScale+™ MPSoC (in this document referred to as "ZynqUP"), which provides a powerful general-purpose ARM-CPU, field-programmable hardware accelerators (FPGA, DSP, and GPU), and flexible I/O for signal and base band processing.

Depending on the target application, the carrier board can be expanded be several types of FMC modules, and an optional clock input/output at the front panel. Hence, it offers the flexibility to address a broad range of applications; especially sophisticated wireless, machine vision, and SDR tasks.

Two prominent fields of application the **NAT-AMC-ZYNQUP-FMC** is ideally suited for, are image processing (NATvision) and SDR/wireless (NATwireless) applications.

Detailed information can be found on our website, please refer to (chapter 8.1 Internal Reference Documentation) for links.

2.1. Main Features

Table 1 – Technical Data

Form Factor	
	• Single-width, mid- or full-size AMC, expandable with one or two FMC(s) • Width: 73.5 mm, Depth: 180.6 mm
Processing Resources	

MPSoc	• Xilinx Zynq Ultrascale+ FPGA MPSoC (speed grade -2)
	  • ZU7EG (standard) ***or***
	  • ZU11EG (on request)
	• Quad-core ARM Cortex-A53 processor (application processing unit)
	• Dual-core ARM Cortex-R5 (real-time processing unit)
	• GPU
	• GTH transceiver speed: 16.3GHz

Memory	• 8 GB DDR4 SDRAM (x64) for PS • 8 GB DDR4 SDRAM (x64) for PL • 1 Gb QSPI or 4GB eMMC boot flash memory • MicroSD card slot • Memory extension slot for additional SRAM or DDR4
Microcontroller	• Atmel ATxmega128 as MMC
Software / Firmware	• IPMI 1.5 compliant • Linux boot – Linux drivers • API for all external/internal interfaces
FPGA Programming Interface	
	• Front panel USB/JTAG connector • JTAG over backplane connections • Onboard Xilinx header connector
FMC Slot	
	• Single HPC FMC slot • VITA 57.1 compliant (with limitations, see chapter 5.3.1) • HPC differential pairs (LA/HA/HB) are routed to the FPGA • DP0 to DP9 are routed to the FPGA • Support of region 1,2, and 3 FMC modules
Backplane Interconnect	
	• Ports 0/1: Dual 1GbE connect • Ports 2/3: FPGA-LVDS-I/Os • Ports 4-15: PCIe/Ethernet/custom protocol • Ports 17-20: Custom protocol FPGA-LVDS-I/Os – RX only • Any combinations of PCIe, SRIO, 10/40GbE (on request) • AMC TCLKA-D and FCLKA connectivity • IPMI for module management • JTAG
Front Panel	
	• Optional Sync-/ Triger IN/OUT (assembly option) • USB/JTAG-Connector • SD card slot • AMC front panel elements and application LEDs
Compliance	
	• AMC.0 R2.0, AMC.1, AMC.2, AMC.3, AMC.4, IMPI V1.5, HPM.1 • EN60950, UL1950, RoHS

Environmental	
Operating Environment	• 0 to +55 degrees Celsius (extended temperature range on request) • Humidity: 5% to 95% (non-condensing)
Storage Environment	• -40 to +100 degrees Celsius • Humidity: 5% to 95% (non-condensing)

3. QUICK START

To ensure proper functioning of the **NAT-AMC-ZYNQUP-FMC** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the AMC-Edge-Connector to ensure proper contact when inserting the **NAT-AMC-ZYNQUP-FMC** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAT-AMC-ZYNQUP-FMC** is designed to meet the requirements of µTCA systems, but can be plugged onto any ATCA carrier board supporting AMC standards as well. So the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAT-AMC-ZYNQUP-FMC**, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-AMC-ZYNQUP-FMC**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-swap-capable, if you do not switch off the power.

Ensure that the **NAT-AMC-ZYNQUP-FMC** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-AMC-ZYNQUP-FMC** must meet the following specifications:

+12V / 7A max.

+ 3,3V / 0.15A max.

3.3.2. Hot-Swap

The **NAT-AMC-ZYNQUP-FMC** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-AMC-ZYNQUP-FMC** or the system it is plugged into from damage!

Insertion of a hot-swap-capable Module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-AMC-ZYNQUP-FMC** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAT-AMC-ZYNQUP-FMC** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable Module

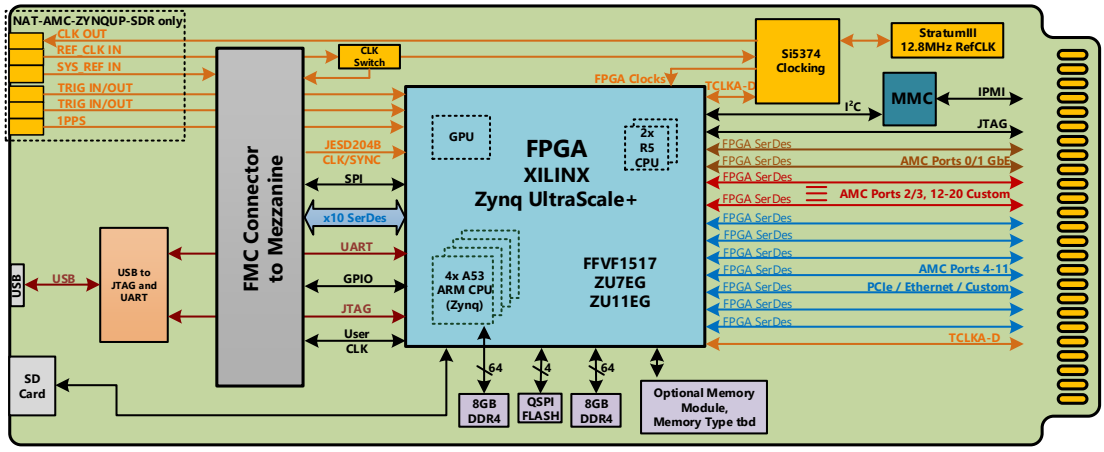
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAT-AMC-ZYNQUP-FMC** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

The **NAT-AMC-ZYNQUP-FMC** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 1 – Block Diagram



4.1. SoC

The central component on the **NAT-AMC-ZYNQUP-FMC** is a Xilinx Zynq MPSoC Ultrascale+ FPGA device (ZynqUP). This SoC provides a powerful general-purpose ARM-CPU, field-programmable hardware accelerators (FPGA, DSP, and GPU), and flexible I/O.

Two different types of MPSoCs are available: ZU7EG or ZU11EG with speed grade -2; GTH transceiver speed is 16.3GHz.

4.1.1. Processing System (CPU)

The CPU core of the ZynqUP features a quad-core ARM Cortex-A53 processor as application processing unit and a dual-core ARM Cortex-R5 for real-time processing. Moreover, it is equipped with a dedicated GPU, realized by a Mali-400 MP2 graphics processing unit.

4.1.1.1. Memory

The Processing System is accompanied by up to 8GB DDR4 RAM (x64, 1600-2400Mb/s). On board NAND and NOR flashes can be used for booting and configuring the ZynqUP. The additional MicroSD-Card slot at the front panel can also be used for that purpose, but offers quicker physical access, which is useful during the development.

Please note: the assembled memory may vary in size and type due to availability und customer preferences

4.1.2. Programmable Logic (FPGA)

4.1.2.1. Programming

The Programmable Logic of the ZynqUP can be accessed via an onboard Xilinx Programming Module (JTAG-SMT3). It allows to program and debug the FPGA using a Micro-USB Cable, while it serves the same functionality as the Xilinx Platform Cable II programmer. Moreover, it features a side UART channel that is connected to the PS UART0.

For more information, please refer to chapter 8.2 8.2External Reference Documentation.

4.1.2.2. Memory

The Programmable Logic is accompanied by up to 8GB DDR4 RAM (x64, 1600-2400Mb/s). The memory to FPGA pin assignment is shown in the tables below.

Table 2 – DDR4-Memory to FPGA Pin Assignment – Address CMD, REFCLK, RESET

DDR4 Pin#	FPGA Bank 65 Pin#	DDR4 Pin#	FPGA Bank 65 Pin#
DDR4_adr[16]	AR13	DDR4_bg[0]	AR15
DDR4_adr[15]	AR12	DDR4_bg[1]	AN13
DDR4_adr[14]	AP12	DDR4_ba[0]	AT13
DDR4_adr[13]	AT11	DDR4_ba[1]	AP15
DDR4_adr[12]	AT12	DDR4_cs_n[0]	AN12
DDR4_adr[11]	AU10	DDR4_odt[0]	AP16
DDR4_adr[10]	AT10	DDR4_cke[0]	AN16
DDR4_adr[9]	AW12	DDR4_act_n	AL15
DDR4_adr[8]	AV12	DDR4_ck_t[0]	AV14
DDR4_adr[7]	AU13	DDR4_ck_c[0]	AV13
DDR4_adr[6]	AU14	get_ports DDR4_REFCLK_B65_clk_p	AP14
DDR4_adr[5]	AW10	get_ports DDR4_REFCLK_B65_clk_n	AR14
DDR4_adr[4]	AW11	get_ports DDR4_reset_n	AN14
DDR4_adr[3]	AW14		
DDR4_adr[2]	AW15		
DDR4_adr[1]	AV11		
DDR4_adr[0]	AU11		

Table 3 – DDR4-Memory to FPGA Pin Assignment – DATA and Strobe

DDR4 Pin#	FPGA Bank 65 Pin#	DDR4 Pin#	FPGA Bank 64 Pin#	DDR4 Pin#	FPGA Bank 66 Pin#
DDR4_dqs_t[0]	AW24	DDR4_dq[0]	AU24	DDR4_dq[32]	AP5
DDR4_dqs_c[0]	AW25	DDR4_dq[1]	AU25	DDR4_dq[33]	AR7
DDR4_dqs_t[1]	AR23	DDR4_dq[2]	AV22	DDR4_dq[34]	AT6
DDR4_dqs_c[1]	AT23	DDR4_dq[3]	AV27	DDR4_dq[35]	AU9
DDR4_dqs_t[2]	AL22	DDR4_dq[4]	AV23	DDR4_dq[36]	AT5
DDR4_dqs_c[2]	AL23	DDR4_dq[5]	AV26	DDR4_dq[37]	AP7
DDR4_dqs_t[3]	AH22	DDR4_dq[6]	AW22	DDR4_dq[38]	AP4
DDR4_dqs_c[3]	AJ22	DDR4_dq[7]	AV24	DDR4_dq[39]	AU8
DDR4_dqs_t[4]	AR5	DDR4_dq[8]	AT22	DDR4_dq[40]	AR10
DDR4_dqs_c[4]	AR4	DDR4_dq[9]	AR22	DDR4_dq[41]	AL11
DDR4_dqs_t[5]	AP11	DDR4_dq[10]	AR25	DDR4_dq[42]	AM10
DDR4_dqs_c[5]	Ap10	DDR4_dq[11]	AP25	DDR4_dq[43]	AM11
DDR4_dqs_t[6]	AV4	DDR4_dq[12]	AR24	DDR4_dq[44]	AR9
DDR4_dqs_c[6]	AW4	DDR4_dq[13]	AP26	DDR4_dq[45]	AK10
DDR4_dqs_t[7]	AT1	DDR4_dq[14]	AT25	DDR4_dq[46]	AL10
DDR4_dqs_c[7]	AU1	DDR4_dq[15]	AP24	DDR4_dq[47]	AN11
DDR4_dm_n[0]	AW26	DDR4_dq[16]	AP22	DDR4_dq[48]	AU4
DDR4_dm_n[1]	AT26	DDR4_dq[17]	AL25	DDR4_dq[49]	AV7
DDR4_dm_n[2]	AN23	DDR4_dq[18]	AM25	DDR4_dq[50]	AU6
DDR4_dm_n[3]	AK24	DDR4_dq[19]	AM24	DDR4_dq[51]	AW7
DDR4_dm_n[4]	AT8	DDR4_dq[20]	AN22	DDR4_dq[52]	AU5
DDR4_dm_n[5]	AP9	DDR4_dq[21]	AN26	DDR4_dq[53]	AW6
DDR4_dm_n[6]	AV9	DDR4_dq[22]	AM23	DDR4_dq[54]	AV6
DDR4_dm_n[7]	AU3	DDR4_dq[23]	AM26	DDR4_dq[55]	AV8
		DDR4_dq[24]	AK23	DDR4_dq[56]	AV2
		DDR4_dq[25]	AJ26	DDR4_dq[57]	AT3
		DDR4_dq[26]	AK22	DDR4_dq[58]	AW2
		DDR4_dq[27]	AJ25	DDR4_dq[59]	AP1
		DDR4_dq[28]	AG23	DDR4_dq[60]	AT2
		DDR4_dq[29]	AH24	DDR4_dq[61]	AR3
		DDR4_dq[30]	AG22	DDR4_dq[62]	AR2
		DDR4_dq[31]	AJ24	DDR4_dq[63]	AP2

On request, the **NAT-AMC-ZYNQUP-FMC** can be equipped with several memory extension cards. Depending on the target application, different memory types can offer advantages; QDR4 and RLDRAM3 memory offers low latency random access, which is useful for applications requiring RAM look up tables (LUTs).

Currently, the **NAT-MEM-DDR4-2x8** (Dual Channel, x8, 2 GB DDR4 memory card) is available. The memory to FPGA pin assignment is described in the following tables.

Table 4 – Memory Card: DDR4-Memory to FPGA Pin Assignment – FPGA Bank 27

Address CMD, REFCLK, RESET, LED				DATA and Strobe	
DDR4 Pin#	**FPGA Pin#**	**DDR4 Pin#**	**FPGA Pin#**	**DDR4 Pin#**	**FPGA Pin#**
DDR4_B27_adr[16]	F32	DDR4_B27_ba[0]	F33	DDR4_B27_dm_n[0]	D36
DDR4_B27_adr[15]	G34	DDR4_B27_ba[1]	F35	DDR4_B27_dq[0]	C38
DDR4_B27_adr[14]	G33	DDR4_B27_bg [0]	F36	DDR4_B27_dq[1]	C39
DDR4_B27_adr[13]	H32	DDR4_B27_bg[1]	E35	DDR4_B27_dq[2]	C37
DDR4_B27_adr[12]	H31	DDR4_B27_cke[0]	E34	DDR4_B27_dq[3]	B38
DDR4_B27_adr[11]	H33	DDR4_B27_cs_n[0]	D35	DDR4_B27_dq[4]	C34
DDR4_B27_adr[10]	J32	DDR4_B27_odt[0]	D34	DDR4_B27_dq[5]	B35
DDR4_B27_adr[9]	E37	DDR4_B27_act_n	E32	DDR4_B27_dq[6]	A37
DDR4_B27_adr[8]	F37	DDR4_B27_ck_t[0]	E39	DDR4_B27_dq[7]	A38
DDR4_B27_adr[7]	G39	DDR4_B27_ck_c[0]	D39	DDR4_B27_dqs_t[0]	A35
DDR4_B27_adr[6]	G38	get_ports {DDR4_REFCLK_B27 _clk_p[0]	G35	DDR4_B27_dqs_c[0]	A36
DDR4_B27_adr[5]	H37	get_ports {DDR4_REFCLK_B27 _clk_n[0]	G36		
DDR4_B27_adr[4]	H36	get_ports DDR4_B27_reset_n	E33		
DDR4_B27_adr[3]	E38	get_ports DDR4_B27_CALIB_ COMP_LED	A32		
DDR4_B27_adr[2]	F38				
DDR4_B27_adr[1]	H39				
DDR4_B27_adr[0]	H38				

Table 5 – Memory Card: DDR4-Memory to FPGA Pin Assignment – FPGA Bank 28

Address CMD, RESET, LED				DATA and Strobe	
DDR4 Pin#	**FPGA Pin#**	**DDR4 Pin#**	**FPGA Pin#**	**DDR4 Pin#**	**FPGA Pin#**
DDR4_B28_adr[16]	D26	DDR4_B28_ba[0]	D27	DDR4_B27_dm_n[0]	K29
DDR4_B28_adr[15]	D30	DDR4_B28_ba[1]	F27	DDR4_B27_dq[0]	K25
DDR4_B28_adr[14]	D29	DDR4_B28_bg [0]	F28	DDR4_B27_dq[1]	J25
DDR4_B28_adr[13]	E30	DDR4_B28_bg[1]	G28	DDR4_B27_dq[2]	K28
DDR4_B28_adr[12]	E29	DDR4_B28_cke[0]	H28	DDR4_B27_dq[3]	J29
DDR4_B28_adr[11]	F31	DDR4_B28_cs_n[0]	G29	DDR4_B27_dq[4]	L27
DDR4_B28_adr[10]	F30	DDR4_B28_odt[0]	H29	DDR4_B27_dq[5]	L28
DDR4_B28_adr[9]	B28	DDR4_B28_act_n	G30	DDR4_B27_dq[6]	M25
DDR4_B28_adr[8]	C27	DDR4_B28_ck_t[0]	C28	DDR4_B27_dq[7]	L25
DDR4_B28_adr[7]	B30	DDR4_B28_ck_c[0]	C29	DDR4_B27_dqs_t[0]	M26
DDR4_B28_adr[6]	B29	get_ports DDR4_B28_reset_n	G31	DDR4_B27_dqs_c[0]	L26
DDR4_B28_adr[5]	A31	get_ports DDR4_B28_CALIB_ COMP_LED	B34		
DDR4_B28_adr[4]	A30				
DDR4_B28_adr[3]	A28				
DDR4_B28_adr[2]	A27				
DDR4_B28_adr[1]	B31				
DDR4_B28_adr[0]	C31				

Please note: the assembled memory may vary in size and type due to availability und customer preferences

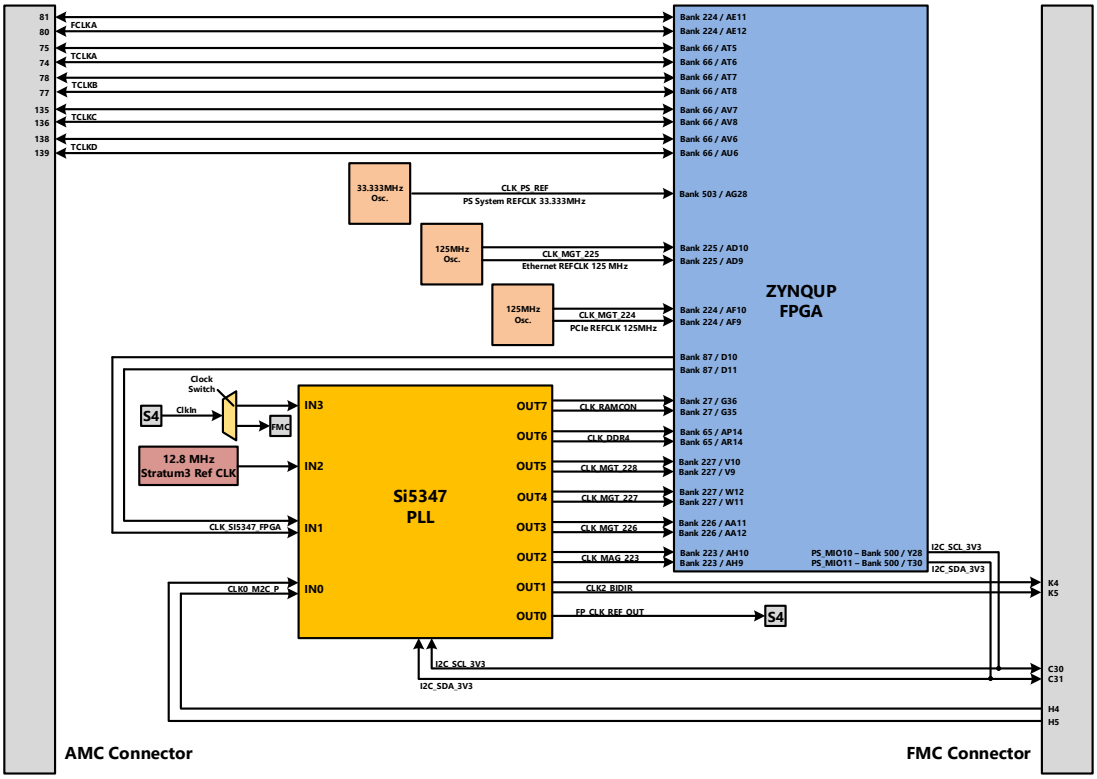
4.2. PLL and Clocking

The **NAT-AMC-ZYNQUP-FMC** features a SI5347 PLL, which is user-configurable by the FPGA via I²C.

When configured as **NAT-AMC-ZYNQUP-SDR**, the **NAT-AMC-ZYNQUP-FMC** carrier is equipped with clock interfaces (see). For reasons of readability, in this chapter these interfaces are just referred to as "S4".

The clock switch becomes relevant in combination with one or two **NAT-FMC-SDR4** board(s): it allows the incoming clock signal from S4 to be directly switched to the FMC, or to the Si5347 PLL instead.

Figure 2 – PLL and Clocking



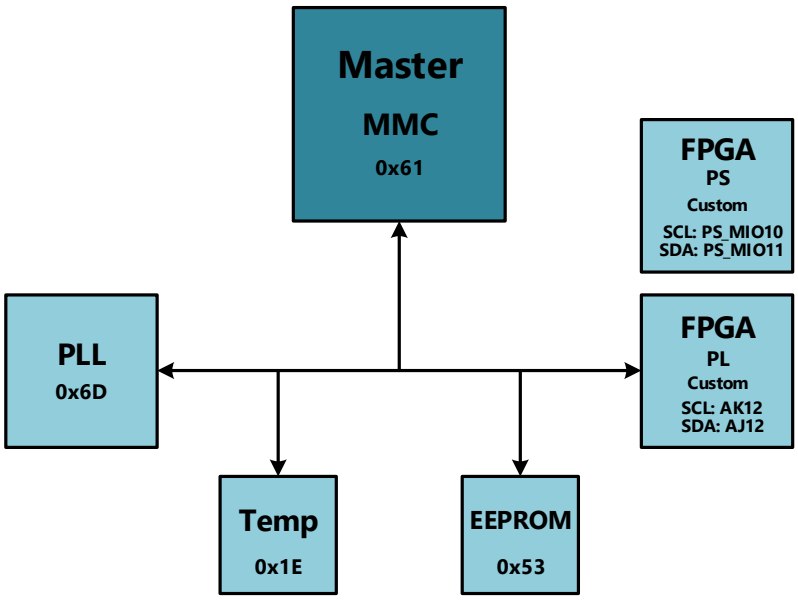
By default, the signal is routed to the PLL and is used as a 10 MHz reference input. In combination with one or two **NAT-FMC-SDR4** modules, this offers the opportunity for multiboard synchronization via an external clock source (e.g., GPS).

4.3. IPMB-Interface and I²C-Devices

The **NAT-AMC-ZYNQUP-FMC** implements an IPMB interface consisting of an IPMI-µC (ATXMega128) and a couple of I²C devices connected via I²C.

The following figure shows the architecture in detail.

Figure 3 – IPMB-Interface



The external channel of the temperature sensor monitors the FPGA temperature, the internal channel measures the local PCB temperature.

The IPMI controller also manages the geographical address as requested by the AMC specification.

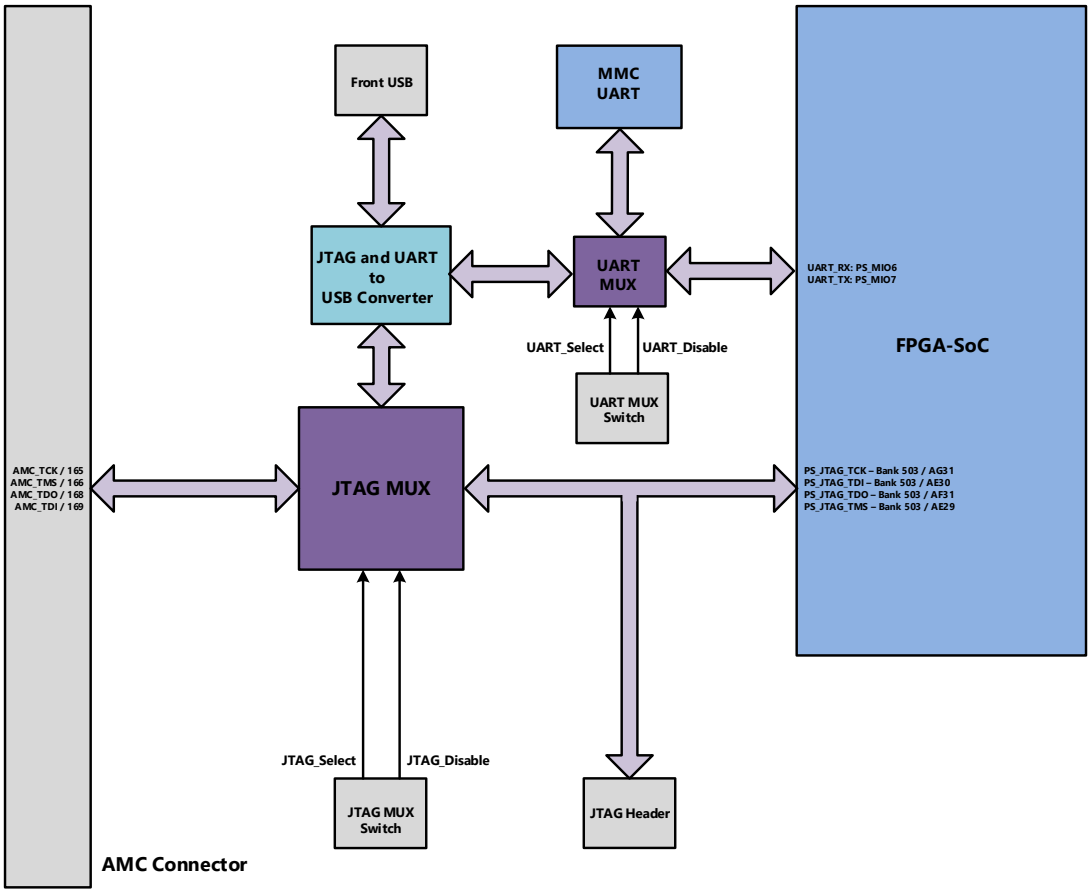
4.4. JTAG and UART

The **NAT-AMC-ZYNQUP-FMC** supports JTAG and serial UART via the front panel USB connector or the on-board JTAG programming header. Both interfaces can be used simultaneously and can be configured using on-board DIP switches.

Configuration of the JTAG Master is possible via the JTAG MUX Switch; for detailed information on this switch, please refer to chapter 5.3.11 SW3: JTAG MUX.

Configuration of the UART Master is possible via the UART MUX Switch; for detailed information on this switch, please refer to chapter 5.3.13 SW6: UART MUX.

Figure 4 – JTAG Architecture



4.5. Interconnect

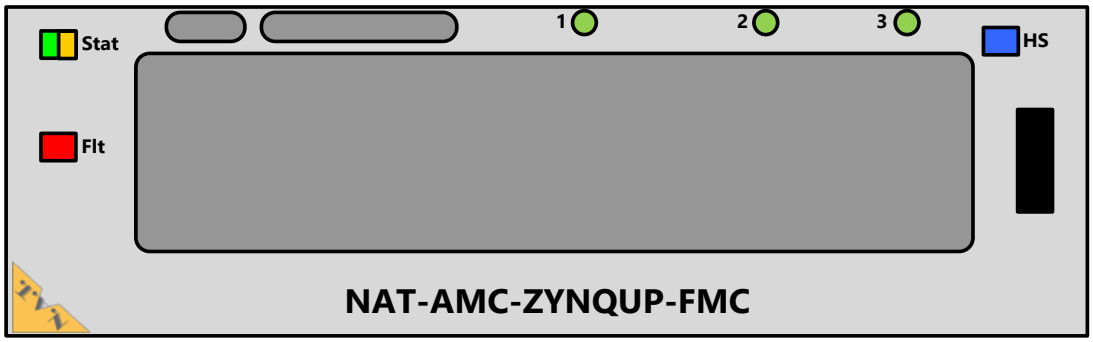
The ZynqUP interfaces directly to the FMC slot via a VITA 57.1 compliant High Pin Count (HPC) connector, and to the µTCA backplane via its high-speed SerDes lanes.

5. HARDWARE

5.1. Front Panel and LEDs

The front plate appearance and the labelling vary depending on the number and variant(s) of installed FMCs. The figure below shows the full-size version of the **NAT-AMC-ZYNQUP-FMC** carrier board.

Figure 5 – Front Panel – Full Size



Colour, behaviour, and function of the front panel LEDs are described in the table below.

Table 6 – LED Functionality

LED	Color	Signal Level / Pins	Function
1 (User)	Green	FPGA_LED5 – AR17 VADJ	User defined
	Red	FPGA_LED4 – AM20 VADJ	No FPGA image loaded
2 (User)	Green	FPGA_LED2 – AT21 VADJ	User defined ***default:*** PCIe link
3 (User)	Green	FPGA_LED3 – AU21 VADJ	User defined
HS (Hot Swap)	Blue ON	n/a	AMC Management power (3V3) present Ready for hot-swap
	Blue Blinking	n/a	IPMI-Controller disables payload power
	OFF	n/a	Payload Power (12V) present
Stat (User)	Green	FPGA_LED1 – AT17 VADJ	User defined ***default:*** DRAM Progr. successful
	Yellow	FPGA_LED0 – AH18 VADJ	User defined
Flt (Fault Indication)	Red ON	n/a	Board over temperature or error during board initialization
	OFF	n/a	Normal operation

5.2. AMC Port Definition

Table 7 – AMC Port Definition

Connector Region		AMC Port #	Signal
Basic Side	**Clocks**	CLK1/TCLKA	Telecom Clock
		CLK2/TCLKB	Telecom Clock
		CLK3/TCLKC	Telecom Clock
		CLK4/TCLKD	Telecom Clock
		CLK5/FCLKA	Fabric Clock
	Common Options	0	GbE
		1	
		2	Custom
		3	
	Fat Pipe	4	PCIe / Ethernet / Custom
		5	
		6	
		7	
Extended Side	**Extended Fat Pipe**	8	PCIe / Ethernet / Custom
		9	
		10	
		11	
	Extended Options	12	Custom
		13	
		14	
		15	
		16	
		17	
		18	
		19	
		20	

5.3. Component-, Connector-, and Switch-Location

Figure 6 – Location Diagram – Top

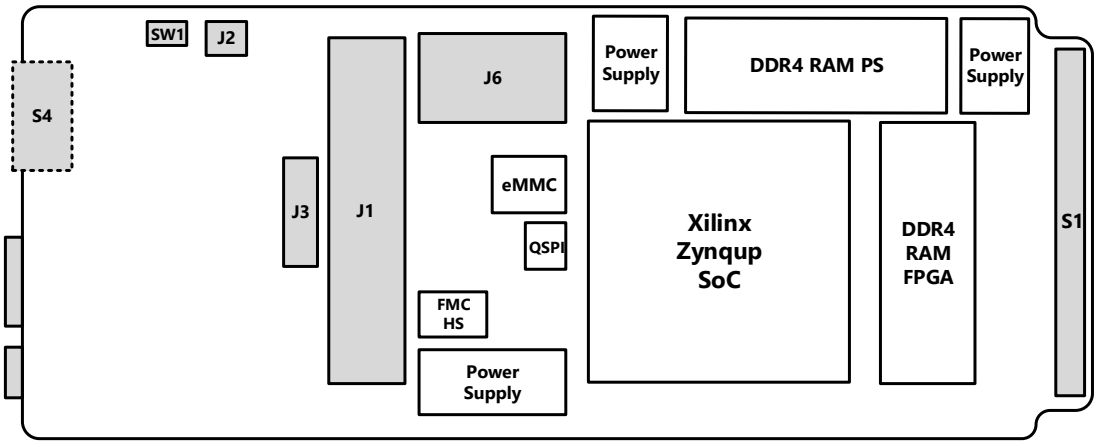
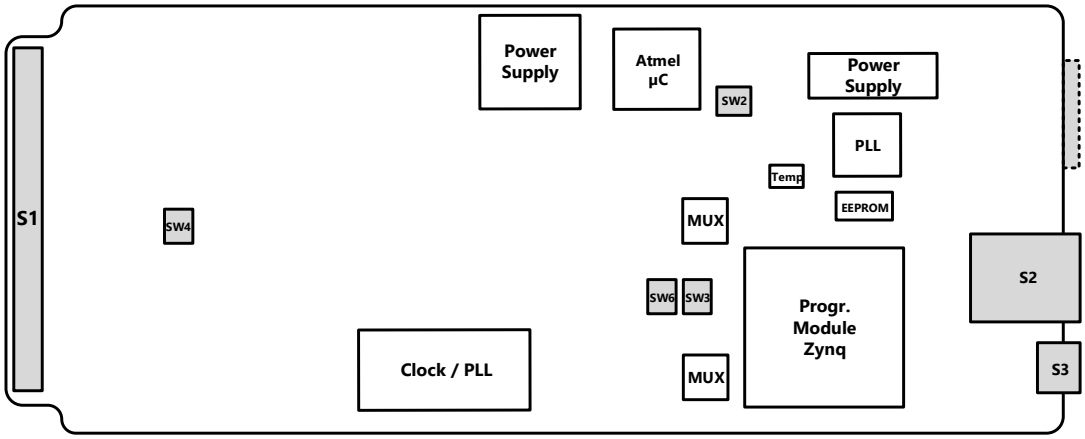


Figure 7 – Location Diagram – Bottom



Connectors on top side: drawings imply the board is orientated with the AMC Edge Connector to the right side

Connectors on bottom side: drawings imply the board is orientated with the AMC Edge Connector to the left side

Please refer to the following tables to look up the connector pin assignment of the **NAT-AMC-ZYNQUP-FMC**.

5.3.1. J1: FMC Connector

Connector J1 connects to an optional FMC mezzanine board

Known limitations:

- LA27, LA21, LA11, HA06 cannot be used for differential pair operation (on Rev 1.0)
- HB20, HB21 are not connected
- CLK2_BIDIR: Direction is fixed to C2M
- HA14, HA10: P-/N-Labelling at FPGA is switched (on Rev 1.0)

Table 8 – J1: FMC Connector – Overview

	A	B	C	D	E	F	G	H	I	J
1	GND	FMC_CLK_DIR	GND	FMC_PG_C2M	GND	FSIG_PG_M2C	GND	VREF_A_M2C	GND	nc
2	DP1_M2C_P	GND	DP0_C2M_P	GND	HA01_CC_P	GND	CLK1_M2C_P	FMC_PRSNT_M2C_L	CLK3_BIDIR_P	GND
3	DP1_M2C_N	GND	DP0_C2M_N	GND	HA01_CC_N	GND	CLK1_M2C_N	GND	CLK3_BIDIR_N	GND
4	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND	HA00_CC_P	GND	CLK0_M2C_P	GND	CLK2_BIDIR_P
5	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND	HA00_CC_N	GND	CLK0_M2C_N	GND	CLK2_BIDIR_N
6	DP2_M2C_P	GND	DP0_M2C_P	GND	HA05_P	GND	LA00_CC_P	GND	HA03_P	GND
7	DP2_M2C_N	GND	DP0_M2C_N	GND	HA05_N	HA04_P	LA00_CC_N	LA02_P	HA03_N	HA02_P
8	GND	DP8_M2C_P	GND	LA01_CC_P	GND	HA04_N	GND	LA02_N	GND	HA02_N
9	GND	DP8_M2C_N	GND	LA01_CC_N	HA09_P	GND	LA03_P	GND	HA07_P	GND
10	DP3_M2C_P	GND	LA06_P	GND	HA09_N	HA08_P	LA03_N	LA04_P	HA07_N	HA06_P
11	DP3_M2C_N	GND	LA06_N	LA05_P	GND	HA08_N	GND	LA04_N	GND	HA06_N

	A	B	C	D	E	F	G	H	I	J
12	GND	DP7_M2C_P	GND	LA05_N	HA13_P	GND	LA08_P	GND	HA11_P	GND
13	GND	DP7_M2C_N	GND	GND	HA13_N	HA12_P	LA08_N	LA07_P	HA11_N	HA10_P
14	DP4_M2C_P	GND	LA10_P	LA09_P	GND	HA12_N	GND	LA07_N	GND	HA10_N
15	DP4_M2C_N	GND	LA10_N	LA09_N	HA16_P	GND	LA12_P	GND	HA14_P	GND
16	GND	DP6_M2C_P	GND	GND	HA16_N	HA15_P	LA12_N	LA11_P	HA14_N	HA17_CC_P
17	GND	DP6_M2C_N	GND	LA13_P	GND	HA15_N	GND	LA11_N	GND	HA17_CC_N
18	DP5_M2C_P	GND	LA14_P	LA13_N	HA20_P	GND	LA16_P	GND	HA18_P	GND
19	DP5_M2C_N	GND	LA14_N	GND	HA20_N	HA19_P	LA16_N	LA15_P	HA18_N	HA21_P
20	GND	GBTCLK1_M2C_P	GND	LA17_CC_P	GND	HA19_N	GND	LA15_N	GND	HA21_N
21	GND	GBTCLK1_M2C_N	GND	LA17_CC_N	HB03_P	GND	LA20_P	GND	HA22_P	GND
22	DP1_C2M_P	GND	LA18_CC_P	GND	HB03_N	HB02_P	LA20_N	LA19_P	HA22_N	HA23_P
23	DP1_C2M_N	GND	LA18_CC_N	LA23_P	GND	HB02_N	GND	LA19_N	GND	HA23_N
24	GND	DP9_C2M_P	GND	LA23_N	HB05_P	GND	LA22_P	GND	HB01_P	GND
25	GND	DP9_C2M_N	GND	GND	HB05_N	HB0_P	LA22_N	LA21_P	HB01_N	HB00_CC_P
26	DP2_C2M_P	GND	LA27_P	LA26_P	GND	HB04_N	GND	LA21_N	GND	HB00_CC_N
27	DP2_C2M_N	GND	LA27_N	LA26_N	HB09_P	GND	LA25_P	GND	HB07_P	GND
28	GND	DP8_C2M_P	GND	GND	HB09_N	HB08_P	LA25_N	LA24_P	HB07_N	HB06_CC_P
29	GND	DP8_C2M_N	GND	FMC_JTAG_TCK	GND	HB08_N	GND	LA24_N	GND	HB06_CC_N
30	DP3_C2M_P	GND	I2C_SCL_3V3	FMC_JTAG_TDI	HB13_P	GND	LA29_P	GND	HB11_P	GND
31	DP3_C2M_N	GND	I2C_SDA_3V3	FMC_JTAG_TDO	HB13_N	HB12_P	LA29_N	LA28_P	HB11_N	HB10_P
32	GND	DP7_C2M_P	GND	3P3VAUX	GND	HB12_N	GND	LA28_N	GND	HB10_N
33	GND	DP7_C2M_N	GND	FMC_JTAG_TMS	HB19_P	GND	LA31_P	GND	HB15_P	GND

	A	B	C	D	E	F	G	H	I	J
34	DP4_C2M_P	GND	FMC_GA0	FMC_JTAG_ TRSTn	HB19_N	HB16_P	LA31_N	LA30_P	HB15_N	HB14_P
35	DP4_C2M_N	GND	12POV	FSIG_GA1	GND	HB16_N	GND	LA30_N	GND	HB14_N
36	GND	DP6_C2M_P	GND	3P3V	HB21_P	GND	LA33_P	GND	HB18_P	GND
37	GND	DP6_C2M_N	12POV	GND	HB21_N	HB20_P	LA33_N	LA32_P	HB18_N	HB17_CC_P
38	DP5_C2M_P	GND	GND	3P3V	GND	HB20_N	GND	LA32_N	GND	HB17_CC_N
39	DP5_C2M_N	GND	3P3V	GND	Vadj	GND	Vadj	GND	VIO_B_M2C	GND
40	GND	nc	GND	3P3V	GND	Vadj	GND	Vadj	GND	VIO_B_M2C

Table 9 – J1A: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
A1	GND	GND				
A2	DP1_M2C_P	DP1_M2C_P	228	1V2_ MGTA VTT	MGTHRXP2_228	K2
A3	DP1_M2C_N	DP1_M2C_N			MGTHRXN2_228	K1
A4	GND	GND				
A5	GND	GND				
A6	DP2_M2C_P	DP2_M2C_P	228	1V2_ MGTA VTT	MGTHRXP1_228	L4
A7	DP2_M2C_N	DP2_M2C_N			MGTHRXN1_228	L3
A8	GND	GND				
A9	GND	GND				
A10	DP3_M2C_P	DP3_M2C_P	228	1V2_ MGTA VTT	MGTHRXP0_228	M2
A11	DP3_M2C_N	DP3_M2C_N			MGTHRXN0_228	M1
A12	GND	GND				
A13	GND	GND				
A14	DP4_M2C_P	DP4_M2C_P	227	1V2_ MGTA VTT	MGTHRXP3_227	N4
A15	DP4_M2C_N	DP4_M2C_N			MGTHRXN3_227	N3
A16	GND	GND				
A17	GND	GND				
A18	DP5_M2C_P	DP5_M2C_P	227	1V2_ MGTA VTT	MGTHRXP2_227	P2
A19	DP5_M2C_N	DP5_M2C_N			MGTHRXN2_227	P1
A20	GND	GND				
A21	GND	GND				
A22	DP1_C2M_P	DP1_C2M_P	228	1V2_ MGTA VTT	MGTHTXP2_228	K6
A23	DP1_C2M_N	DP1_C2M_N			MGTHTXN2_228	K5
A24	GND	GND				
A25	GND	GND				
A26	DP2_C2M_P	DP2_C2M_P	228	1V2_ MGTA VTT	MGTHTXP1_228	L8
A27	DP2_C2M_N	DP2_C2M_N			MGTHTXN1_228	L7
A28	GND	GND				
A29	GND	GND				
A30	DP3_C2M_P	DP3_C2M_P	228	1V2_ MGTA VTT	MGTHTXP0_228	M6
A31	DP3_C2M_N	DP3_C2M_N			MGTHTXN0_228	M5
A32	GND	GND				
A33	GND	GND				
A34	DP4_C2M_P	DP4_C2M_P	227	1V2_ MGTA VTT	MGTHTXP3_227	N8
A35	DP4_C2M_N	DP4_C2M_N			MGTHTXN3_227	N7
A36	GND	GND				

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
A37	GND	GND				
A38	DP5_C2M_P	DP5_C2M_P	227	1V2_ MGTA VTT	MGTHTXP2_227	P6
A39	DP5_C2M_N	DP5_C2M_N			MGTHTXN2_227	P5
A40	GND	GND				

Table 10 – J1B: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
B1	CLK_DIR	FMC_CLK_DIR	501	3V3	PS_MIO34	L32
B2	GND	GND				
B3	GND	GND				
B4	DP9_M2C_P	DP9_M2C_P	226	1V2_ MGTA VTT	MGTHRXP2_226	V2
B5	DP9_M2C_N	DP9_M2C_N			MGTHRXN2_226	V1
B6	GND	GND				
B7	GND	GND				
B8	DP8_M2C_P	DP8_M2C_P	226	1V2_ MGTA VTT	MGTHRXP3_226	U4
B9	DP8_M2C_N	DP8_M2C_N			MGTHRXN3_226	U3
B10	GND	GND				
B11	GND	GND				
B12	DP7_M2C_P	DP7_M2C_P	227	1V2_ MGTA VTT	MGTHRXP0_227	T2
B13	DP7_M2C_N	DP7_M2C_N			MGTHRXN0_227	T1
B14	GND	GND				
B15	GND	GND				
B16	DP6_M2C_P	DP6_M2C_P	227	1V2_ MGTA VTT	MGTHRXP1_227	R4
B17	DP6_M2C_N	DP6_M2C_N			MGTHRXN1_227	R3
B18	GND	GND				
B19	GND	GND				
B20	GBTCLK1_M2C_P	GBTCLK1_M2C_P	228	1V2_ MGTA VTT	GBTCLK1_M2C_C_P	T10
B21	GBTCLK1_M2C_N	GBTCLK1_M2C_N			GBTCLK1_M2C_C_N	T9
B22	GND	GND				
B23	GND	GND				
B24	DP9_C2M_P	DP9_C2M_P	226	1V2_ MGTA VTT	MGTHTXP2_226	V6
B25	DP9_C2M_N	DP9_C2M_N			MGTHTXN2_226	V5
B26	GND	GND				
B27	GND	GND				
B28	DP8_C2M_P	DP8_C2M_P	226	1V2_ MGTA VTT	MGTHTXP3_226	U8
B29	DP8_C2M_N	DP8_C2M_N			MGTHTXN3_226	U7

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
B30	GND	GND				
B31	GND	GND				
B32	DP7_C2M_P	DP7_C2M_P	227	1V2_ MGTA VTT	MGTHTXP0_227	T6
B33	DP7_C2M_N	DP7_C2M_N			MGTHTXN0_227	T5
B34	GND	GND				
B35	GND	GND				
B36	DP6_C2M_P	DP6_C2M_P	227	1V2_ MGTA VTT	MGTHTXP1_227	R8
B37	DP6_C2M_N	DP6_C2M_N			MGTHTXN1_227	R7
B38	GND	GND				
B39	GND	GND				
B40	RES0	FMC-RES0				

Table 11 – J1C: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
C1	GND	GND				
C2	DP0_C2M_P	DP0_C2M_P	228	1V2_ MGTA VTT	MGTHTXP3_228	J8
C3	DP0_C2M_N	DP0_C2M_N			MGTHTXN3_228	J7
C4	GND	GND				
C5	GND	GND				
C6	DP0_M2C_P	DP0_M2C_P	228	1V2_ MGTA VTT	MGTHRXP3_228	J4
C7	DP0_M2C_N	DP0_M2C_N			MGTHRXN3_228	J3
C8	GND	GND				
C9	GND	GND				
C10	LA06_P	LA06_P	68	VADJ	IO_L18P_T2U_N10_AD 2N_68	J22
C11	LA06_N	LA06_N			IO_L18N_T2U_N11_AD 2P_68	H22
C12	GND	GND				
C13	GND	GND				
C14	LA10_P	LA10_P	67	VADJ	IO_L18P_T2U_N10_AD 2P_67	F20
C15	LA10_N	LA10_N			IO_L18N_T2U_N11_AD 2N_67	E20
C16	GND	GND				
C17	GND	GND				
C18	LA14_P	LA14_P	67	VADJ	IO_L19P_T3L_N0_DBC _AD9P_67	C19
C19	LA14_N	LA14_N			IO_L19N_T3L_N1_DBC _AD9N_67	C18
C20	GND	GND				

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
C21	GND	GND				
C22	LA18_P_CC	LA18_CC_P	68	VADJ	IO_L12P_T1U_N10_GC_68	F23
C23	LA18_N_CC	LA18_CC_N			IO_L12N_T1U_N11_GC_68	E23
C24	GND	GND				
C25	GND	GND				
C26	LA27_P	LA27_P	63	VADJ	IO_L15P_T2L_N4_AD11P_63	AR18
C27	LA27_N	LA27_N			IO_L15N_T2L_N5_AD11N_63	AT18
C28	GND	GND				
C29	GND	GND				
C30	SCL	I2C_SCL_3V3	500	3V3	PS-MIO10	Y28
C31	SDA	I2C_SDA_3V3			PS_MIO11	T30
C32	GND	GND				
C33	GND	GND				
C34	GA0	FMC_GA0				
C35	12POV	12POV				
C36	GND	GND				
C37	12POV	12POV				
C38	GND	GND				
C39	3P3V	3P3V				
C40	GND	GND				

Table 12 – J1D: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
D1	PG_C2M	FMC_PG_C2M				
D2	GND	GND				
D3	GND	GND				
D4	GBTCLK0_M2C_P	GBTCLK0_M2C_P	228	1V2_MGTAVTT	MGTREFCLK0P_228	U12
D5	GBTCLK0_M2C_N	GBTCLK0_M2C_N			MGTREFCLK0N_228	U11
D6	GND	GND				
D7	GND	GND				
D8	LA01_P_CC	LA01_CC_P	68	VADJ	IO_L13P_T2L_N0_GC_QBC_68	H23
D9	LA01_N_CC	LA01_CC_N			IO_L13N_T2L_N1_GC_QBC_68	G23
D10	GND	GND				
D11	LA05_P	LA05_P	68	VADJ	IO_L1P_T0L_N0_DBC_68	A22

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
D12	LA05_N	LA05_N			IO_L1N_T0L_N1_DBC_68	A23
D13	GND	GND				
D14	LA09_P	LA09_P	68	VADJ	IO_L17P_T2U_N8_AD10P_68	J21
D15	LA09_N	LA09_N			IO_L17N_T2U_N9_AD10N_68	H21
D16	GND	GND				
D17	LA13_P	LA13_P	67	VADJ	IO_L24P_T3U_N10_67	B20
D18	LA13_N	LA13_N			IO_L24N_T3U_N11_67	A20
D19	GND	GND				
D20	LA17_P_CC	LA17_CC_P	68	VADJ	IO_L11P_T1U_N8_GC_68	F21
D21	LA17_N_CC	LA17_CC_N			IO_L11N_T1U_N9_GC_68	F22
D22	GND	GND				
D23	LA23_P	LA23_P	68	VADJ	IO_L3P_T0L_N4_AD15P_68	B21
D24	LA23_N	LA23_N			IO_L3N_T0L_N5_AD15N_68	A21
D25	GND	GND				
D26	LA26_P	LA26_P	68	VADJ	IO_L15P_T2L_N4_AD11P_68	G20
D27	LA26_N	LA26_N			IO_L15N_T2L_N5_AD11N_68	G21
D28	GND	GND				
D29	TCK	FMC_JTAG_TCK				
D30	TDI	FMC_JTAG_TDI				
D31	TDO	FMC_JTAG_TDO				
D32	3P3VAUX	3P3VAUX				
D33	TMS	FMC_JTAG_TMS				
D34	TRST_L	FMC_JTAG_TRSTn				
D35	GA1	FMC_GA1				
D36	3P3V	3P3V				
D37	GND	GND				
D38	3P3V	3P3V				
D39	GND	GND				
D40	3P3V	3P3V				

Table 13 – J1E: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
E1	GND	GND				
E2	HA01_P_CC	HA01_CC_P	67	VADJ	IO_L13P_T2L_N0_GC_QBC_67	F17
E3	HA01_N_CC	HA01_CC_N			IO_L13N_T2L_N1_GC_QBC_67	F16
E4	GND	GND				
E5	GND	GND				
E6	HA05_P	HA05_P	67	VADJ	IO_L10P_T1U_N6_QBC_AD4P_67	K19
E7	HA05_N	HA05_N			IO_L10N_T1U_N7_QBC_AD4N_67	J19
E8	GND	GND				
E9	HA09_P	HA09_P	67	VADJ	IO_L11P_T1U_N8_GC_67	H17
E10	HA09_N	HA09_N			IO_L11N_T1U_N9_GC_67	G16
E11	GND	GND				
E12	HA13_P	HA13_P	67	VADJ	IO_L9P_T1L_N4_AD12P_67	J16
E13	HA13_N	HA13_N			IO_L9N_T1L_N5_AD12N_67	H16
E14	GND	GND				
E15	HA16_P	HA16_P	67	VADJ	IO_L4P_T0U_N6_DBC_AD7P_67	L17
E16	HA16_N	HA16_N			IO_L4N_T0U_N7_DBC_AD7N_67	L16
E17	GND	GND				
E18	HA20_P	HA20_P	63	VADJ	IO_L8P_T1L_N2_AD5P_63	AM21
E19	HA20_N	HA20_N			IO_L8N_T1L_N3_AD5N_63	AL21
E20	GND	GND				
E21	HB03_P	HB03_P	88	VIO_B_M2C	IO_L4P_AD12P_88	H14
E22	HB03_N	HB03_N			IO_L4N_AD12N_88	G14
E23	GND	GND				
E24	HB05_P	HB05_P	88	VIO_B_M2C	IO_L10P_AD10P_88	C14
E25	HB05_N	HB05_N			IO_L10N_AD10N_88	B14
E26	GND	GND				
E27	HB09_P	HB09_P	88	VIO_B_M2C	IO_L9P_AD11P_88	D14
E28	HB09_N	HB09_N			IO_L9N_AD11N_88	C13
E29	GND	GND				
E30	HB13_P	HB13_P	87	VIO_B_M2C	IO_L9P_AD3P_87	D12
E31	HB13_N	HB13_N			IO_L9N_AD3N_87	C12
E32	GND	GND				
E33	HB19_P	HB19_P	87	VIO_B_M2C	IO_L2P_AD10P_87	K12
E34	HB19_N	HB19_N			IO_L2N_AD10N_87	J11

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
E35	GND	GND				
E36	HB21_P	HB21_P			nc	
E37	HB21_N	HB21_N			nc	
E38	GND	GND				
E39	VADJ	Vadj				
E40	GND	GND				

Table 14 – J1F: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
F1	PG_M2C	FMC_PG_M2C				
F2	GND	GND				
F3	GND	GND				
F4	HA00_P_CC	HA00_CC_P	67	VADJ	IO_L14P_T2L_N2_GC_67	G19
F5	HA00_N_CC	HA00_CC_N			IO_L14N_T2L_N3_GC_67	G18
F6	GND	GND				
F7	HA04_P	HA04_P	67	VADJ	IO_L16P_T2U_N6_QBC_AD3P_67	E19
F8	HA04_N	HA04_N			IO_L16N_T2U_N7_QBC_AD3N_67	E18
F9	GND	GND				
F10	HA08_P	HA08_P	67	VADJ	IO_L15P_T2L_N4_AD11P_67	F18
F11	HA08_N	HA08_N			IO_L15N_T2L_N5_AD11N_67	E17
F12	GND	GND				
F13	HA12_P	HA12_P	67	VADJ	IO_L8P_T1L_N2_AD5P_67	K17
F14	HA12_N	HA12_N			IO_L8N_T1L_N3_AD5N_67	J17
F15	GND	GND				
F16	HA15_P	HA15_P	67	VADJ	IO_L1P_T0L_N0_DBC_67	N14
F17	HA15_N	HA15_N			IO_L1N_T0L_N1_DBC_67	M14
F18	GND	GND				
F19	HA19_P	HA19_P	63	VADJ	IO_L10P_T1U_N6_QBC_AD4P_63	AN21
F20	HA19_N	HA19_N			IO_L10N_T1U_N7_QBC_AD4N_63	AP21
F21	GND	GND				
F22	HB02_P	HB02_P	88	VIO_B_M2C	IO_L8P_HDGC_88	E15
F23	HB02_N	HB02_N			IO_L8N_HDGC_88	D15

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
F24	GND	GND				
F25	HB04_P	HB04_P	88	VIO_B_M2C	IO_L11P_AD9P_88	B13
F26	HB04_N	HB04_N			IO_L11N_AD9N_88	A13
F27	GND	GND				
F28	HB08_P	HB08_P	87	VIO_B_M2C	IO_L10P_AD2P_87	C11
F29	HB08_N	HB08_N			IO_L10N_AD2N_87	B11
F30	GND	GND				
F31	HB12_P	HB12_P	87	VIO_B_M2C	IO_L3P_AD9P_87	J12
F32	HB12_N	HB12_N			IO_L3N_AD9N_87	H12
F33	GND	GND				
F34	HB16_P	HB16_P	88	VIO_B_M2C	IO_L1P_AD15P_88	L13
F35	HB16_N	HB16_N			IO_L1N_AD15N_88	L12
F36	GND	GND				
F37	HB20_P	HB20_P			nc	
F38	HB20_N	HB20_N			nc	
F39	GND	GND				
F40	VADJ	Vadj				

Table 15 – J1G: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
G1	GND	GND				
G2	CLK1_M2C_P	CLK1_M2C_P	87	VIO_B_M2C	IO_L5P_HDGC_AD7P_87	G11
G3	CLK1_M2C_N	CLK1_M2C_N			IO_L5N_HDGC_AD7N_87	F11
G4	GND	GND				
G5	GND	GND				
G6	LA00_P_CC	LA00_CC_P	68	VADJ	IO_L14P_T2L_N2_GC_68	G24
G7	LA00_N_CC	LA00_CC_N			IO_L14N_T2L_N3_GC_68	G25
G8	GND	GND				
G9	LA03_P	LA03_P	68	VADJ	IO_L2P_T0L_N2_68	B25
G10	LA03_N	LA03_N			IO_L2N_T0L_N3_68	B26
G11	GND	GND				
G12	LA08_P	LA08_P	68	VADJ	IO_L5P_T0U_N8_AD14P_68	C21
G13	LA08_N	LA08_N			IO_L5N_T0U_N9_AD14N_68	C22
G14	GND	GND				
G15	LA12_P	LA12_P	68	VADJ	IO_L7P_T1L_N0_QBC_AD13P_68	E24

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
G16	LA12_N	LA12_N			IO_L7N_T1L_N1_QBC_AD13N_68	D25
G17	GND	GND				
G18	LA16_P	LA16_P	68	VADJ	IO_L10P_T1U_N6_QBC_AD4P_68	D24
G19	LA16_N	LA16_N			IO_L10N_T1U_N7_QBC_AD4N_68	C24
G20	GND	GND				
G21	LA20_P	LA20_P	67	VADJ	IO_L21P_T3L_N4_AD8P_67	C17
G22	LA20_N	LA20_N			IO_L21N_T3L_N5_AD8N_67	C16
G23	GND	GND				
G24	LA22_P	LA22_P	68	VADJ	IO_L9P_T1L_N4_AD12P_68	D21
G25	LA22_N	LA22_N			IO_L9N_T1L_N5_AD12N_68	D22
G26	GND	GND				
G27	LA25_P	LA25_P	67	VADJ	IO_L20P_T3L_N2_AD1P_67	B19
G28	LA25_N	LA25_N			IO_L20N_T3L_N3_AD1N_67	B18
G29	GND	GND				
G30	LA29_P	LA29_P	68	VADJ	IO_L23P_T3U_N8_68	L20
G31	LA29_N	LA29_N			IO_L23N_T3U_N9_68	K20
G32	GND	GND				
G33	LA31_P	LA31_P	68	VADJ	IO_L19P_T3L_N0_DBC_AD9P_68	N21
G34	LA31_N	LA31_N			IO_L19N_T3L_N1_DBC_AD9N_68	M21
G35	GND	GND				
G36	LA33_P	LA33_P	68	VADJ	IO_L16P_T2U_N6_QBC_AD3P_68	J24
G37	LA33_N	LA33_N			IO_L16N_T2U_N7_QBC_AD3N_68	H24
G38	GND	GND				
G39	VADJ	Vadj				
G40	GND	GND				

Table 16 – J1H: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
H1	VREF_A_M2C	VREF_A_M2C	66	VADJ	VREF_66	AK11
H2	PRSNT_M2C_L	PRSNT_M2C_L				
H3	GND	GND				
H4	CLK0_M2C_P	CLK0_M2C_P				
H5	CLK0_M2C_N	CLK0_M2C_N				
H6	GND	GND				
H7	LA02_P	LA02_P	68	VADJ	IO_L4P_T0U_N6_DBC_AD7P_68	A25
H8	LA02_N	LA02_N			IO_L4N_T0U_N7_DBC_AD7N_68	A26
H9	GND	GND				
H10	LA04_P	LA04_P	68	VADJ	IO_L6P_T0U_N10_AD6P_68	B23
H11	LA04_N	LA04_N			IO_L6N_T0U_N11_AD6N_68	B24
H12	GND	GND				
H13	LA07_P	LA07_P	68	VADJ	IO_L8P_T1L_N2_AD5P_68	F25
H14	LA07_N	LA07_N			IO_L8N_T1L_N3_AD5N_68	E25
H15	GND	GND				
H16	LA11_P	LA11_P	67	VADJ	IO_L18P_T2U_N10_AD2P_63	AT20
H17	LA11_N	LA11_N			IO_L18N_T2U_N11_AD2N_63	AU20
H18	GND	GND				
H19	LA15_P	LA15_P	67	VADJ	IO_L22P_T3U_N6_DBC_AD0P_67	A18
H20	LA15_N	LA15_N			IO_L22N_T3U_N7_DBC_AD0N_67	A17
H21	GND	GND				
H22	LA19_P	LA19_P	67	VADJ	IO_L23P_T3U_N8_67	B16
H23	LA19_N	LA19_N			IO_L23N_T3U_N9_67	A16
H24	GND	GND				
H25	LA21_P	LA21_P	63	VADJ	IO_L24P_T3U_N10_63	AK19
H26	LA21_N	LA21_N			IO_L24N_T3U_N11_63	AK18
H27	GND	GND				
H28	LA24_P	LA24_P	68	VADJ	IO_L22P_T3U_N6_DBC_AD0P_68	L22
H29	LA24_N	LA24_N			IO_L22N_T3U_N7_DBC_AD0N_68	L23
H30	GND	GND				
H31	LA28_P	LA28_P	68	VADJ	IO_L24P_T3U_N10_68	N22
H32	LA28_N	LA28_N			IO_L24N_T3U_N11_68	N23
H33	GND	GND				

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
H34	LA30_P	LA30_P	68	VADJ	IO_L20P_T3L_N2_AD1P_68	K23
H35	LA30_N	LA30_N			IO_L20N_T3L_N3_AD1N_68	K24
H36	GND	GND				
H37	LA32_P	LA32_P	68	VADJ	IO_L21P_T3L_N4_AD8P_68	M20
H38	LA32_N	LA32_N			IO_L21N_T3L_N5_AD8N_68	L21
H39	GND	GND				
H40	VADJ	VADJ				

Table 17 – J1I: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
J1	GND	GND				
J2	CLK3_BIDIR_P	CLK3_BIDIR_P	87	VIO_B_M2C	IO_L6P_HDGC_AD6P_87	F10
J3	CLK3_BIDIR_N	CLK3_BIDIR_N			IO_L6N_HDGC_AD6N_87	E10
J4	GND	GND				
J5	GND	GND				
J6	HA03_P	HA03_P	67	VADJ	IO_L2P_T0L_N2_67	N19
J7	HA03_N	HA03_N			IO_L2N_T0L_N3_67	N18
J8	GND	GND				
J9	HA07_P	HA07_P	67	VADJ	IO_L6P_T0U_N10_AD6P_67	M18
J10	HA07_N	HA07_N			IO_L6N_T0U_N11_AD6N_67	L18
J11	GND	GND				
J12	HA11_P	HA11_P	67	VADJ	IO_L7P_T1L_N0_QBC_AD13P_67	K15
J13	HA11_N	HA11_N			IO_L7N_T1L_N1_QBC_AD13N_67	J15
J14	GND	GND				
J15	HA14_P	HA14_P	67	VADJ	IO_L3N_T0L_N5_AD15N_67	M16
J16	HA14_N	HA14_N			IO_L3P_T0L_N4_AD15P_67	N16
J17	GND	GND				
J18	HA18_P	HA18_P	63	VADJ	IO_L6P_T0U_N10_AD6P_63	AV19
J19	HA18_N	HA18_N			IO_L6N_T0U_N11_AD6N_63	AU10
J20	GND	GND				

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
J21	HA22_P	HA22_P	63	VADJ	IO_L9P_T1L_N4_AD12P_63	AL18
J22	HA22_N	HA22_N			IO_L9N_T1L_N5_AD12N_63	AL17
J23	GND	GND				
J24	HB01_P	HB01_P	88	VIO_B_M2C	IO_L12P_AD8P_88	B15
J25	HB01_N	HB01_N			IO_L12N_AD8N_88	A15
J26	GND	GND				
J27	HB07_P	HB07_P	87	VIO_B_M2C	IO_L12P_AD0P_87	A12
J28	HB07_N	HB07_N			IO_L12N_AD0N_87	A11
J29	GND	GND				
J30	HB11_P	HB11_P	87	VIO_B_M2C	IO_L11P_AD1P_87	B10
J31	HB11_N	HB11_N			IO_L11N_AD1N_87	A10
J32	GND	GND				
J33	HB15_P	HB15_P	87	VIO_B_M2C	IO_L4P_AD8P_87	H11
J34	HB15_N	HB15_N			IO_L4N_AD8N_87	G10
J35	GND	GND				
J36	HB18_P	HB18_P	87	VIO_B_M2C	IO_L1P_AD11P_87	K10
J37	HB18_N	HB18_N			IO_L1N_AD11N_87	J10
J38	GND	GND				
J39	VIO_B_M2C	VIO_B_M2C				
J40	GND	GND				

Table 18 – J1J: FMC Connector

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
K1	VREF_B_M2C	nc				
K2	GND	GND				
K3	GND	GND				
K4	CLK2_BIDIR_P	CLK2_BIDIR_P				
K5	CLK2_BIDIR_N	CLK2_BIDIR_N				
K6	GND	GND				
K7	HA02_P	HA02_P	67	VADJ	IO_L17P_T2U_N8_AD10P_67	D17
K8	HA02_N	HA02_N			IO_L17N_T2U_N9_AD10N_67	D16
K9	GND	GND				
K10	HA06_P	HA06_P	63	VADJ	IO_L21P_T3L_N4_AD8P_63	AJ21
K11	HA06_N	HA06_N			IO_L21N_T3L_N5_AD8N_63	AJ20
K12	GND	GND				
K13	HA10_P	HA10_P	67	VADJ	IO_L5N_T0U_N9_AD14N_67	L15

FMC Pin#	FMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
K14	HA10_N	HA10_N			IO_L5P_T0U_N8_AD14P_67	M15
K15	GND	GND				
K16	HA17_P_CC	HA17_CC_P	67	VADJ	IO_L12P_T1U_N10_GC_67	H19
K17	HA17_N_CC	HA17_CC_N			IO_L12N_T1U_N11_GC_67	H18
K18	GND	GND				
K19	HA21_P	HA21_P	63	VADJ	IO_L5P_T0U_N8_AD14P_63	AV16
K20	HA21_N	HA21_N			IO_L5N_T0U_N9_AD14N_63	AW16
K21	GND	GND				
K22	HA23_P	HA23_P	63	VADJ	IO_L7P_T1L_N0_QBC_AD13P_63	AM19
K23	HA23_N	HA23_N			IO_L7N_T1L_N1_QBC_AD13N_63	AM18
K24	GND	GND				
K25	HB00_P_CC	HB00_CC_P	88	VIO_B_M2C	IO_L6P_HDGC_88	G15
K26	HB00_N_CC	HB00_CC_N			IO_L6N_HDGC_88	F15
K27	GND	GND				
K28	HB06_P_CC	HB06_CC_P	88	VIO_B_M2C	IO_L5P_HDGC_88	G13
K29	HB06_N_CC	HB06_CC_N			IO_L5N_HDGC_88	F13
K30	GND	GND				
K31	HB10_P	HB10_P	88	VIO_B_M2C	IO_L2P_AD14P_88	K14
K32	HB10_N	HB10_N			IO_L2N_AD14N_88	K13
K33	GND	GND				
K34	HB14_P	HB14_P	88	VIO_B_M2C	IO_L3P_AD13P_88	J14
K35	HB14_N	HB14_N			IO_L3N_AD13N_88	H13
K36	GND	GND				
K37	HB17_P_CC	HB17_CC_P	87	VIO_B_M2C	IO_L7P_HDGC_AD5P_87	F12
K38	HB17_N_CC	HB17_CC_N			IO_L7N_HDGC_AD5N_87	E12
K39	GND	GND				
K40	VIO_B_M2C	VIO_B_M2C				

5.3.2. J2: Microcontroller Programming Header

Connector J2 features a programming interface for the Atmel microcontroller.

Figure 8 – J2: Microcontroller Programming Interface

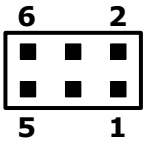


Table 19 – J2: Microcontroller Programming Header

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V_MP	2
3	nc	nc	4
5	PDI_CLK	GND	6

5.3.3. J3: JTAG Programming Header

Connector J3 offers a JTAG programming interface.

Figure 9 – J3: JTAG Programming Header

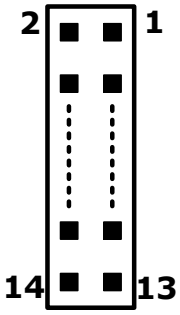


Table 20 – J3: JTGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	V_PROG	JTAG_DISABLE	2
3	FPGA_TMS	GND	4
5	FPGA_TCK	GND	6
7	FPGA_TDO	GND	8
9	FPGA_TDI	GND	10
11	nc	GND	12
13	PS_ARM_SRST	GND	14

5.3.4. J6: Memory Connector

Connector J6 offers the option to connect additional memory, e.g. RLDRAM, QDR4-SRAM, or another DDR4 RAM.

The memory to FPGA pin assignment varies depending on the installed memory type, so a general specification cannot be given. Please refer to chapter 4.1.2.2 Memory for details.

5.3.5. S1: AMC Connector

Figure 10 – S1: AMC-Connector (top view)

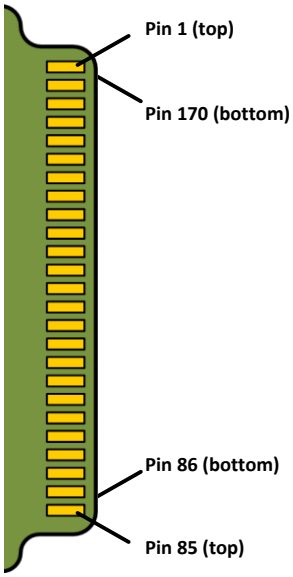


Table 21 – S1A: AMC-Connector Top – Pin-Assignment

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
1	GND	GND				
2	PWR	+12V_PP				
3	PS1#	/AMC_PS1				
4	MP	+3.3V_MP				
5	GA0	AMC_GA0				
6	RSVD6	nc				
7	GND	GND				
8	RSVD8	nc				
9	PWR	+12V_PP				
10	GND	GND				
11	TX0+	PORT0-Tx_P	225	1V2_ MGTA VTT	MGTHTXP1_225	AC8
12	TX0-	PORT0-Tx_N			MGTHTXN1_225	AC7
13	GND	GND				
14	RX0+	PORT0-Rx_P	225	1V2_ MGTA VTT	MGTHRXP1_225	AC4
15	RX0-	PORT0-Rx_N			MGTHRXN1_225	AC3
16	GND	GND				
17	GA1	AMC_GA1				
18	PWR	+12V_PP				

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
19	GND	GND				
20	TX1+	PORT1-Tx_P	225	1V2_ MGTA VTT	MGTHTXP0_225	AD6
21	TX1-	PORT1-Tx_N			MGTHTXN0_225	AD5
22	GND	GND				
23	RX1+	PORT1-Rx_P	225	1V2_ MGTA VTT	MGTHRXP0_225	AD2
24	RX1-	PORT1-Rx_N			MGTHRXN0_225	AD1
25	GND	GND				
26	GA2	AMC_GA2				
27	PWR	+12V_PP				
28	GND	GND				
29	TX2+	PORT2-Tx_P	63	VADJ	IO_L22P_T3U_N6_DBC _AD0P_63	AH19
30	TX2-	PORT2-Tx_N			IO_L22N_T3U_N7_DBC _AD0N_63	AJ19
31	GND	GND				
32	RX2+	PORT2-Rx_P	63	VADJ	IO_L19P_T3L_N0_DBC _AD9P_63	AK20
33	RX2-	PORT2-Rx_N			IO_L19N_T3L_N1_DBC _AD9N_63	AL20
34	GND	GND				
35	TX3+	PORT3-Tx_P	63	VADJ	IO_L23P_T3U_N8_63	AG21
36	TX3-	PORT3-Tx_N			IO_L23N_T3U_N9_63	AH21
37	GND	GND				
38	RX3+	PORT3-Rx_P	63	VADJ	IO_L20P_T3L_N2_AD1 P_63	AG20
39	RX3-	PORT3-Rx_N			IO_L20N_T3L_N3_AD1 N_63	AG19
40	GND	GND				
41	ENABLE#	AMC_ENABLEn				
42	PWR	+12V_PP				
43	GND	GND				
44	TX4+	PORT4-Tx_P	224	1V2_ MGTA VTT	MGTHTXP3_224	AE8
45	TX4-	PORT4-Tx_N			MGTHTXN3_224	AE7
46	GND	GND				
47	RX4+	PORT4-Rx_P	224	1V2_ MGTA VTT	MGTHRXP3_224	AE4
48	RX4-	PORT4-Rx_N			MGTHRXN3_224	AE3
49	GND	GND				
50	TX5+	PORT5-Tx_P	224	1V2_ MGTA VTT	MGTHTXP2_224	AF6
51	TX5-	PORT5-Tx_N			MGTHTXN2_224	AF5
52	GND	GND				
53	RX5+	PORT5-Rx_P	224	1V2_ MGTA VTT	MGTHRXP2_224	AF2
54	RX5-	PORT5-Rx_N			MGTHRXN2_224	AF1

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
55	GND	GND				
56	SCL	AMC_SCL				
57	PWR	+12V_PP				
58	GND	GND				
59	TX6+	PORT6-Tx_P	224	1V2_ MGTA VTT	MGTHTXP1_224	AG8
60	TX6-	PORT6-Tx_N			MGTHTXN1_224	AG7
61	GND	GND				
62	RX6+	PORT6-Rx_P	224	1V2_ MGTA VTT	MGTHRXP1_224	AG4
63	RX6-	PORT6-Rx_N			MGTHRXN1_224	AG3
64	GND	GND				
65	TX7+	PORT7-Tx_P	224	1V2_ MGTA VTT	MGTHTXP0_224	AH6
66	TX7-	PORT7-Tx_N			MGTHTXN0_224	AH5
67	GND	GND				
68	RX7+	PORT7-Rx_P	224	1V2_ MGTA VTT	MGTHRXP0_224	AH2
69	RX7-	PORT7-Rx_N			MGTHRXN0_224	AH1
70	GND	GND				
71	SDA	AMC_SDA				
72	PWR	+12V_PP				
73	GND	GND				
74	TCLKA+	AMC_TCLKA_P	63	VADJ	IO_L12P_T1U_N10_GC_63	AN19
75	TCLKA-	AMC_TCLKA_N			IO_L12N_T1U_N11_GC_63	AN18
76	GND	GND				
77	TCLKB+	AMC_TCLKB_P	63	VADJ	IO_L14P_T2L_N2_GC_63	AP20
78	TCLKB-	AMC_TCLKB_N			IO_L14N_T2L_N3_GC_63	AR20
79	GND	GND				
80	FCLKA+	AMC_FCLKA_P	224	1V2_ MGTA VTT	MGTREFCLK1P_224	AE12
81	FCLKA-	AMC_FCLKA_N			MGTREFCLK1N_224	AE11
82	GND	GND				
83	PS0#	/AMC_PS0				
84	PWR	+12V_PP				
85	GND	GND				

Table 22 – S1B: AMC-Connector Bottom – Pin-Assignment

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
86	GND	GND				
87	RX8-	PORT8-Rx_N	223	1V2_ MGTA VTT	MGTHRXN3_223	AJ3
88	RX8+	PORT8-Rx_P			MGTHRXP3_223	AJ4
89	GND	GND				
90	TX8-	PORT8-Tx_N	223	1V2_ MGTA VTT	MGTHTXN3_223	AJ7
91	TX8+	PORT8-Tx_P			MGTHTXP3_223	AJ8
92	GND	GND				
93	RX9-	PORT9-Rx_N	223	1V2_ MGTA VTT	MGTHRXN2_223	AK1
94	RX9+	PORT9-Rx_P			MGTHRXP2_223	AK2
95	GND	GND				
96	TX9-	PORT9-Tx_N	223	1V2_ MGTA VTT	MGTHTXN2_223	AK5
97	TX9+	PORT9-Tx_P			MGTHTXP2_223	AK6
98	GND	GND				
99	RX10-	PORT10-Rx_N	223	1V2_ MGTA VTT	MGTHRXN1_223	AL3
100	RX10+	PORT10-Rx_P			MGTHRXP1_223	AL4
101	GND	GND				
102	TX10-	PORT10-Tx_N	223	1V2_ MGTA VTT	MGTHTXN1_223	AL7
103	TX10+	PORT10-Tx_P			MGTHTXP1_223	AL8
104	GND	GND				
105	RX11-	PORT11-Rx_N	223	1V2_ MGTA VTT	MGTHRXN0_223	AM1
106	RX11+	PORT11-Rx_P			MGTHRXP0_223	AM2
107	GND	GND				
108	TX11-	PORT11-Tx_N	223	1V2_ MGTA VTT	MGTHTXN0_223	AM5
109	TX11+	PORT11-Tx_P			MGTHTXP0_223	AM6
110	GND	GND				
111	RX12-	PORT12-Rx_N	225	1V2_ MGTA VTT	MGTHRXN2_225	AB1
112	RX12+	PORT12-Rx_P			MGTHRXP2_225	AB2
113	GND	GND				
114	TX12-	PORT12-Tx_N	225	1V2_ MGTA VTT	MGTHTXN2_225	AB5
115	TX12+	PORT12-Tx_P			MGTHTXP2_225	AB6
116	GND	GND				
117	RX13-	PORT13-Rx_N	225	1V2_ MGTA VTT	MGTHRXN3_225	AA3
118	RX13+	PORT13-Rx_P			MGTHRXP3_225	AA4
119	GND	GND				

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
120	TX13-	PORT13-Tx_N	225	1V2_MGTAVTT	MGTHTXN3_225	AA7
121	TX13+	PORT13-Tx_P			MGTHTXP3_225	AA8
122	GND	GND				
123	RX14-	PORT14-Rx_N	226	1V2_MGTAVTT	MGTHRXN0_226	Y1
124	RX14+	PORT14-Rx_P			MGTHRXP0_226	Y2
125	GND	GND				
126	TX14-	PORT14-Tx_N	226	1V2_MGTAVTT	MGTHTXN0_226	Y5
127	TX14+	PORT14-Tx_P			MGTHTXP0_226	Y6
128	GND	GND				
129	RX15-	PORT15-Rx_N	226	1V2_MGTAVTT	MGTHRXN1_226	W3
130	RX15+	PORT15-Rx_P			MGTHRXP1_226	W4
131	GND	GND				
132	TX15-	PORT15-Tx_N	226	1V2_MGTAVTT	MGTHTXN1_226	W7
133	TX15+	PORT15-Tx_P			MGTHTXP1_226	W8
134	GND	GND				
135	TCLKC-	AMC_TCLKC_N	63	VADJ	IO_L13N_T2L_N1_GC_QBC_63	AR19
136	TCLKC+	AMC_TCLKC_P			IO_L13P_T2L_N0_GC_QBC_63	AP19
137	GND	GND				
138	TCLKD-	AMC_TCLKD_N	63	VADJ	IO_L11N_T1U_N9_GC_63	AP17
139	TCLKD+	AMC_TCLKD_P			IO_L11P_T1U_N8_GC_63	AN17
140	GND	GND				
141	RX17-	PORT17-Rx_N	63	VADJ	IO_L3N_T0L_N5_AD15N_63	AW17
142	RX17+	PORT17-Rx_P			IO_L3P_T0L_N4_AD15P_63	AV17
143	GND	GND				
144	TX17-	PORT17-Tx_N				
145	TX17+	PORT17-Tx_P				
146	GND	GND				
147	RX18-	PORT18-Rx_N	63	VADJ	IO_L4N_T0U_N7_DBC_AD7N_63	AW19
148	RX18+	PORT18-Rx_P			IO_L4P_T0U_N6_DBC_AD7P_63	AW20
149	GND	GND				
150	TX18-	PORT18-Tx_N				
151	TX18+	PORT18-Tx_P				
152	GND	GND				
153	RX19-	PORT19-Rx_N	63	VADJ	IO_L1N_T0L_N1_DBC_63	AV18

AMC Pin#	AMC Label	NAT-AMC-ZYNQUP-FMC Label	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
154	RX19+	PORT19-Rx_P			IO_L1P_T0L_N0_DBC_63	AU18
155	GND	GND				
156	TX19-	PORT19-Tx_N				
157	TX19+	PORT19-Tx_P				
158	GND	GND				
159	RX20-	PORT20-Rx_N	63	VADJ	IO_L2N_T0L_N3_63	AW21
160	RX20+	PORT20-Rx_P			IO_L2P_T0L_N2_63	AV21
161	GND	GND				
162	TX20-	PORT20-Tx_N				
163	TX20+	PORT20-Tx_P				
164	GND	GND				
165	TCK	AMC_TCK				
166	TMS	AMC_TMS				
167	TRST#	nc				
168	TDO	AMC_TDO				
169	TDI	AMC_TDI				
170	GND	GND				

5.3.6. S2: MicroSD-Card Slot

The **NAT-AMC-ZYNQUP-FMC** includes a secure digital input/output (SDIO) interface to provide user-logic access to general-purpose nonvolatile MicroSD-Cards. To boot from a MicroSD-Card, insert a card with a bootable image and set the boot mode switches (see chapter 5.3.12 SW4 : Boot Mode Select Switch for details) to MicroSD-Card position.

Figure 11 – S2: MicroSD-Card Slot

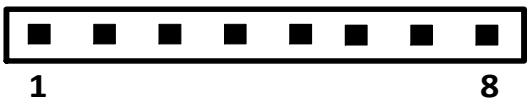


Table 23 – S2: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SD_DAT2	SD_DAT3	2
3	SD_CMD	3V3	4
5	SD_CLK	GND	6
7	SD_DAT0	SD_DAT1	8

5.3.7. S3: USB-/ UART Connector

The **NAT-AMC-ZYNQUP-FMC** features an USB-/ UART interface via a Micro-USB connector at the front panel. It is necessary to use a cable with a long micro-USB connector (7mm+).

Figure 12 – S3: USB-/ UART Connector

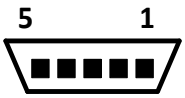


Table 24 – S3: USB-/ UART Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	V_USB	USB_N	2
3	USB_P	nc	4
5	GND		

5.3.8. S4: Sync- and Trigger Interfaces

Connector S4 is assembly only when the **NAT-AMC-ZYNQUP-FMC** works as carrier board in the **NAT-AMC-ZYNQUP-SDR** combination. It provides sync- and trigger signals towards the front panel.

Figure 13 – S4: Sync- and Trigger Interfaces

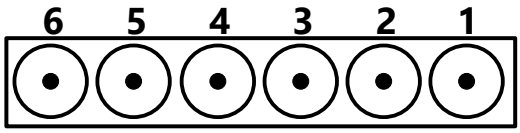


Table 25 – Sync- and Trigger Interfaces

Pin #	Signal	Signal	Pin #
1	TRIG OUT	CLK REF OUT	2
3	PPS IN	TRIG IN	4
5	JESD CLK IN	JESD RFSYNC IN	6

5.3.9. SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

5.3.10. SW2: FMC Configuration Switch

The tables below provide information on the operating parameters and configuration options of SW2.

Figure 14 – SW2: FMC Configuration Switch

Table 26 – SW2 – Operating Parameters

Switch #	Function
SW2-1	Reserved for future
SW2-2	FMC record generation

Table 27 – SW2 – Configuration

Switch #	ON	OFF
SW2-1	Reserved for future	***Reserved future***
SW2-2	Start FMC record wizard within 5 seconds by pressing a random key in terminal	***Normal operation.***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3.11. SW3: JTAG MUX Switch

The tables below provide information on the operating parameters and configuration options of SW3.

Figure 15 – SW3: JTAG MUX Switch

Table 28 – SW3 – Operating Parameters

Switch #	Function
SW3-1	JTAG Select – FPGA or JTAG-SMT3 module as Master
SW3-2	JTAG Disable

Table 29 – SW3 – Configuration

Switch #	ON	OFF
SW3-1	Use Backplane as FPGA JTAG Master	***Use JTAG-SMT3 as FPGA JTAG Master***
SW3-2	JTAG Circuits are disabled	***JTAG Circuits are enabled***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3.12. SW4 : Boot Mode Select Switch

The **NAT-AMC-ZYNQUP-FMC** supports several boot options:

- Boot from SD card
- Boot from on-board QSPI FLASH
- Boot from JTAG

The configuration options are printed on PCB according to the figure and the table below.

Figure 16 – SW4: Positions of Boot Select Switch

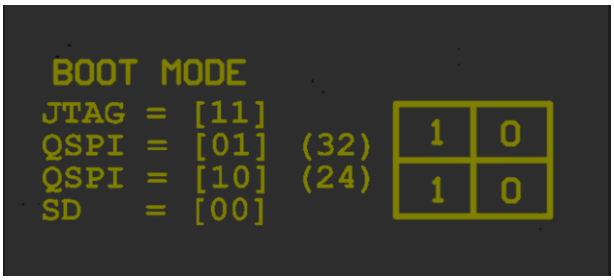
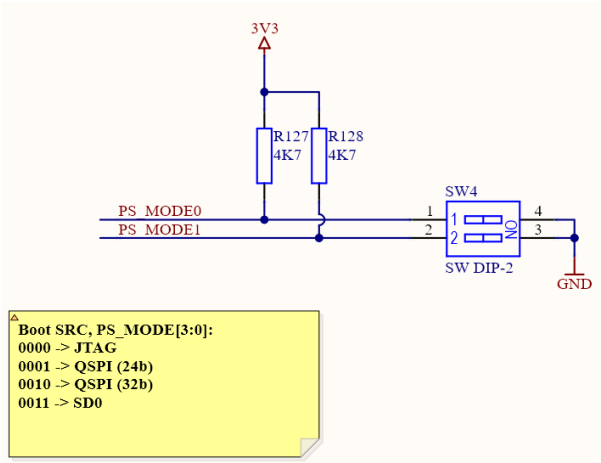


Table 30 – SW4: Boot Mode Select Switch HW v1.2

Boot Mode	SW4-2	SW4-1
JTAG	ON	ON
QSPI(32)	***OFF***	***ON***
QSPI(24)	ON	OFF
SD Card	OFF	OFF

Note:

Default configuration is labelled with ***bold, italic letters***.



5.3.13. SW6: UART MUX

The tables below provide information on the operating parameters and configuration options of SW6.

Figure 17 – SW6: UART MUX

Table 31 – SW6 – Operating Parameters

Switch #	Function
SW6-1	UART Select
SW6-2	UART Disable

Table 32 – SW6 – Configuration

Switch #	ON	OFF
SW6-1	Use MMC UART	***Use FPGA UART***
SW6-2	UART disabled	***UART enabled***

Note:

Default configuration is labelled with ***bold, italic letters***.

6. FMC OPERATION

6.1. Front panel

Depending on the used FMC, the front panel metalwork may not fit and needs to be reworked. This is needed in case FMCs with 8.5 mm stacking height are used that do not fit into the standard front panel cut out which is made for 100 mm stacking height FMCs. Please contact N.A.T. in case specialized front panel needs to be made.

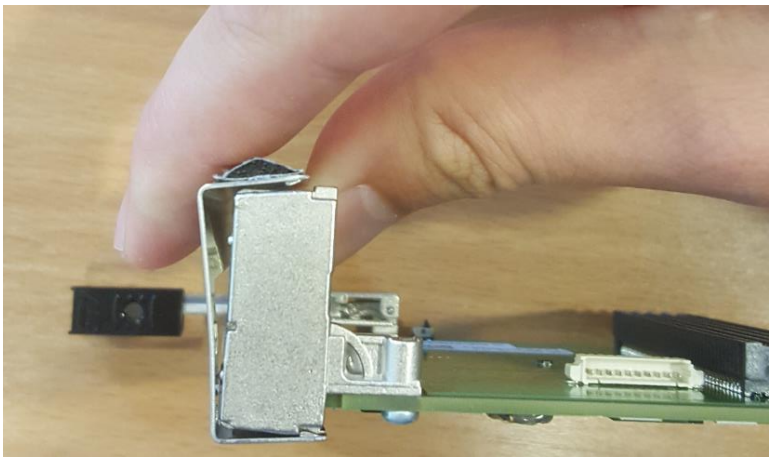
6.2. Supported FMC's

All FMCs compliant to VITA 57.1 are supported, including region 1, 2, and 3 FMC modules. VADJ and VIO_B_M2C are limited to 1.8V. Please check I/O 5.3.1 table for constraints to make sure your FMC is supported.

6.3. Installing a FMC Module

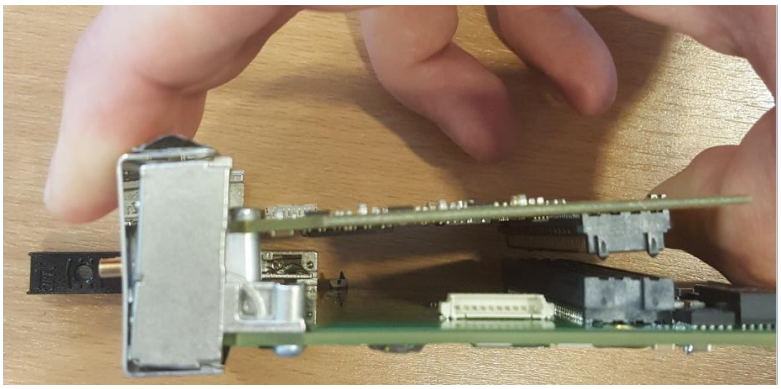
When applying a FMC module it could be necessary to remove or to untighten the front metal in order for the FMC front to fit into the cut-out.

Figure 18 – Installing FMC Module Part 1



After fitting the FMC module to the carrier, the front panel needs to be restored.

Figure 19 – Installing FMC Module Part 2



6.4. FMC EEPROM Wizard

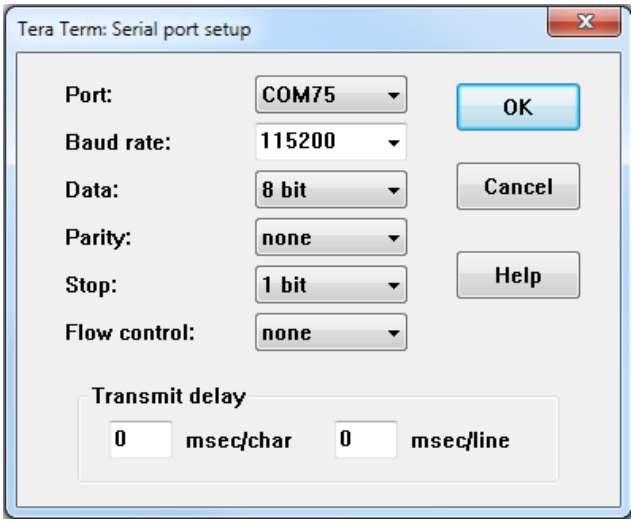
Per default, the carrier will try to parse the FMC FRU records from the modules EEPROM contents to set the carrier's power supply and clock direction. In case there is an FMC without records, there are two options:

1) Generate and program the records with the carrier. Set SW2-3 2 to "ON".

2) Ignore the FRU EEPROM. This is automatically done when no valid FRU content is detected. ***Warning:*** In this case, a default VADJ voltage of 1.8V is applied to the FMC module. Please check the capabilities of your FMC in this case.

In case the records for the FMC should be generated with the carrier, the Micro USB cable has to be connected to the front plate's USB port. The host should detect a USB-Hub and two COM ports. The first enumerated COM port is the serial console of the MMC. Open it with a tool (e.g. TeraTerm) and set the COM settings according to the following figure.

Figure 20 – Serial Console COM Port Settings



The MMC has to be rebooted with triggering the HS-Handle. The console output should output the following line:

```
Press any key to generate FMC FRU file ... 5.0
```

Within five seconds time press any key to enter the FMC programming mode. This mode is guided and will lead through the steps to program the FMC records. At the end of the wizard, it will ask to program the EEPROM file of the FMC.

7. KNOWN ISSUES

PCB V1.2 has the following known issues:

- LA27, LA21, LA11, HA06 cannot be used for differential pair operation
- Clock Direction of CLK2_BIDIR is fixed at C2M
- HA14, HA10: P-/N-Labelling at FPGA is switched

8. SPECIFICATIONS AND COMPLIANCES

8.1. Internal Reference Documentation

- **NAT-AMC-ZYNQUP-FMC**
- **NAT-AMC-ZYNQUP-SDR**
- https://nateurope.com/solution/natwireless/
- https://nateurope.com/solution/natvision/

8.2. External Reference Documentation

- Atmel ATxmega128 µC Product Datasheet, Rev A, 08/2018
- Micron MT40A512M16LY-062 DDR4 SDRAM Datasheet, Rev. P, 04/2019
- Xilinx Zynq UltraScale+ MPSoC DS891, V1.10, 11/2022
- Xilinx Programming Module: https://reference.digilentinc.com/reference/programmers/jtag-smt3/reference-manual

8.3. Standards Compliance

- AMC.0 R2.0
- AMC.1
- AMC.2
- AMC.3
- AMC.4
- IMPI V1.5
- HPM.1

8.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

8.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

8.6. Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

8.7. Product Safety

The board complies with EN60950 and UL1950.

8.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8.9. Abbreviation List

Table 33 – Abbreviation List

Abbreviation	Description
ADC	Analog-Digital-Converter
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
CPU	Central Processing Unit
DAC	Digital-Analog-Converter
DDR4 SDRAM	Double Data Rate Synchronous DRAM
(D)RAM	(Dynamic) Random Access Memory
eMMC	Embedded Multimedia Card
FCLK	Fabric Clock
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FRU	Field-Replaceable Unit
GbE	Gigabit Ethernet
GPU	Graphics Processing Unit
HPC	High Pin-Count
HPM	Hardware Platform Management
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
MicroSD-Card	Micro Secure Digital Memory Card
MIMO	Multiple-Input and Multiple-Output
MUX	Multiplexer
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
QDR4 RAM	Quad Data Rate RAM
(Q)SPI (FLASH)	(Quad) Serial Peripheral Interface (FLASH)
RF	Radio Frequency
RL DRAM	Reduced Latency DRAM
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SDR	Software Defined Radio
SoC	System on a Chip
SRIO	Serial Rapid I/O
TCKL	Telecom Clock
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

9. DOCUMENT'S HISTORY

Table 34 – Document's History

Rev	Date	Description	Author
1.0	12.12.2019	• initial release	se
	11.02.2020	• Added title foto	se
	22.04.2020	• Added FMC-Signal routing information • Added PLL-/Clocking information	se
	29.04.2020	• Minor changes	mm
1.1	20.01.2021	• Updated Block Diagram in chapter 4 Functional Description • Updated chapter 4.1.2 Programmable Logic (FPGA) • Added chapter 4.3 IPMB-Interface and I^2C-Devices	se
	27.01.2021	• Updated chapter 4.3 IPMB-Interface and I^2C-Devices	mm
	04.05.2021	• Updated Figure 7– Location Diagram – Bottom • Updated 5.3.12 SW4 : Boot Mode Select Switch	se
1.2	3.11.2021	• Reworked chapter 2 Introduction • Updated block diagrams in chapter 4 Functional Description • Updated Colour, behaviour, and function of the front panel LEDs are described in the table below. • Table 6 – LED Functionality • Updated chapter 4.2 PLL and Clocking • Updated chapter 5.3 Component-, Connector-, and Switch-Location • Minor updates in layout, typo correction, etc.	Se
	09.08.2022	• Updated Colour, behaviour, and function of the front panel LEDs are described in the table below. • Table 6 – LED Functionality	se
	31.05.2023	• Removed information related to prior hardware versions • Updated Table 1 – Technical Data • Updated chapter 4.1 SoC with regards to memory size and speed grade • Updated Table 3 – DDR4-Memory to FPGA Pin Assignment – DATA and Strobe • Updated Tables 11, 13, 14, 16, 17, 18 – Pin Assignment J1 • Updated Table 20, 21 – Pin Assignment S1 • Hyperlink update to new website • Minor changes in wording etc.	se
1.3	15.06.2023	• Added J2 connector description • Added S4 connector description	se