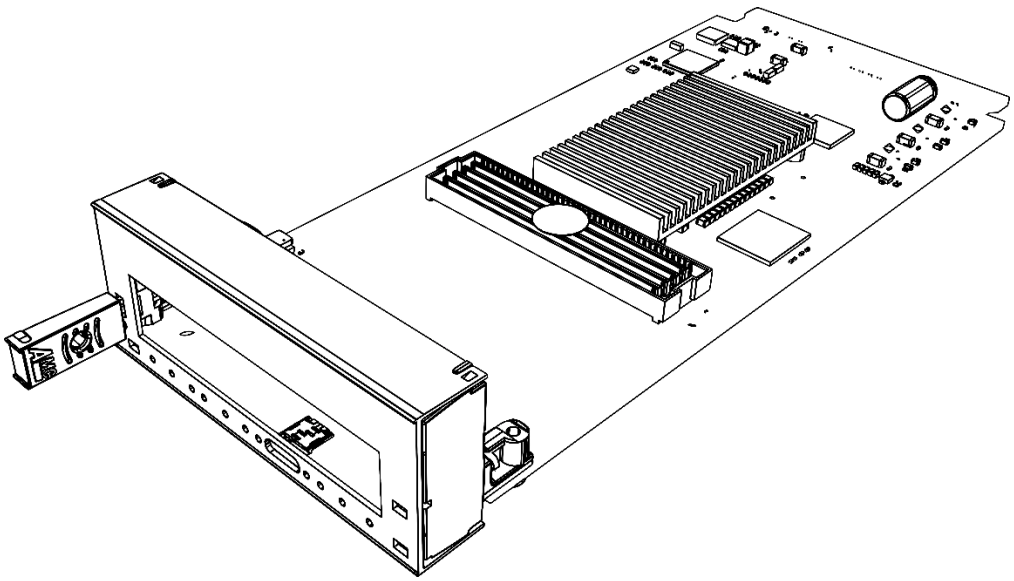
NAT-AMC-ZYNQUP-ECO

FMC CARRIER BOARD

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.3

HW REVISION 1.X

N.A.T. Gesellschaft für Netzwerk- und Automatisierungs-Technologie mbH
Konrad-Zuse-Platz 9 | 53227 Bonn, Germany | Phone: +49 228 965 864 - 0
sales@nateurope.com | www.nateurope.com

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. PREFACE

1.1. Disclaimer

The following documentation, compiled by N.A.T. GmbH (henceforth called N.A.T.), represents the current status of the product´s development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. N.A.T. is under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

We must caution you, that this publication could include technical inaccuracies or typographical errors.

N.A.T. offers no warranty, either expressed or implied, for the contents of this documentation or for the product described therein, including but not limited to the warranties of merchantability or the fitness of the product for any specific purpose.

In no event will N.A.T. be liable for any loss of data or for errors in data utilization or processing resulting from the use of this product or the documentation. In particular, N.A.T. will not be responsible for any direct or indirect damages (including lost profits, lost savings, delays or interruptions in the flow of business activities, including but not limited to, special, incidental, consequential, or other similar damages) arising out of the use of or inability to use this product or the associated documentation, even if N.A.T. or any authorized N.A.T. representative has been advised of the possibility of such damages.

All registered names, trademarks etc. are property of their respective holders. The use of registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations (patent laws, trade mark laws, etc.) and therefore free for general use. In no case does N.A.T. guarantee that the information given in this documentation is free of such third-party rights.

Neither this documentation nor any part thereof may be copied, translated, or reduced to any electronic medium or machine form without the prior written consent from N.A.T. GmbH.

This product (and the associated documentation) is governed by the N.A.T. General Conditions and Terms of Delivery and Payment.

Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-AMC-ZYNQUP-ECO's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-AMC-ZYNQUP-ECO's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-AMC-ZYNQUP-ECO** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-AMC-ZYNQUP-ECO's** main features

Hardware

Description of the connectors, switches, and LEDs located on the **NAT-AMC-ZYNQUP-ECO**

FMC Operation

Special information on mounting and operating a FMC module on the **NAT-AMC-ZYNQUP-ECO**

Known Issues

List of known issues of the current PCB version

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document and standards, the **NAT-AMC-ZYNQUP-ECO** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-AMC-ZYNQUP-ECO** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-AMC-ZYNQUP-ECO** is a FMC carrier for a wide field of applications. Depending on the number of installed mezzanines, the board comes in mid-size (one FMC) or single full-size (two FMCs) AMC form factor.

Heart of the **NAT-AMC-ZYNQUP-ECO** is a Xilinx Zynq UltraScale+ (for better readability: ZynqUP) FPGA. This so-called MPSoC combines the best of two worlds: an FPGA portion for time-critical, massive parallel processing, and ARM CPU cores for higher-level software tasks. The board is available in various FPGA configurations.

2.1. Basic Functionality

The PS (Processing System - CPU part) is accompanied by 4GB DDR4 RAM; the PL (Programmable Logic - FPGA part) comes with 2GB DDR4 RAM. Flexible I/Os including high speed SerDes interconnects make it ready for operation in many domains. A versatile on-board PLL (programmable by the MPSoC) provides a basis for timing and clock synchronization.

The FMC carrier supports Low Pin Count connectors (LPC) as defined by VITA 57.1. This allows the use of standard-off-the-shelf FMCs i.e., for industrial busses, industrial serial I/O etc.

The **NAT-AMC-ZYNQUP-ECO** features an MicroSD-Card slot. So, it allows an easy change of software configurations during development or maintenance, or extra security features.

2.2. Applications

As the board's functionality is determined mainly by the installed FMC card, it offers many options to meet the customer's specific demands: An important field of application is **NATvision**. In combination with the **NAT-FMC-PoE**, the **NAT-AMC-ZYNQUP-ECO** targets on applications like aggregation and processing of video streams.

Detailed information can be found on our website, please refer to (chapter 7.1 Internal Reference Documentation) for links.

2.3. Main Features

Table 1 – Technical Data

Form Factor	
	• Single-width, mid- or full-size AMC, expandable with one or two FMC(s) • Width: 73.5 mm, Depth: 180.6 mm
Processing Resources	

MPSoC	• Xilinx Zynq Ultrascale+ FPGA MPSoC
	  • ZU2CG/EG
	  • ZU4CG/EG/EV
	  • ZU5CG/EG/EV
	• Dual-or quad-core ARM Cortex-A53 processor (application processing unit)
	• Dual-core ARM Cortex-R5 (real-time processing unit)

Memory	• 4 GB DDR4 SDRAM (x64) for PS • 2 GB DDR4 SDRAM (x64) for PL • QSPI FLASH • eMMC • MicroSD card slot
Microcontroller	• Atmel ATxmega128 as MMC
Software / Firmware	• IPMI 1.5 compliant • Linux boot – Linux drivers • API for all external/internal interfaces
FPGA Programming Interface	
	• Front panel USB/JTAG connector • JTAG over backplane connections • Onboard Xilinx header connector
FMC Slot	
	• Single HPC FMC slot • VITA 57.1 compliant
Backplane Interconnect	
	• Ports 0/1: Dual 1G-KX • Ports 4/5: PCIe x1/x2 or 10G-KR (depending on FPGA type) • AMC TCLKA-D and FCLKA connectivity • IPMI for module management • JTAG
Front Panel	
	• USB/JTAG-Connector • SD card slot • AMC front panel elements and application LEDs
Compliance	
	• AMC.0 R2.0, CE, RoHS, REACH
Environmental	
Operating Environment	• 0 to +55 degrees Celsius (extended temperature range on request) • Humidity: 5% to 95% (non-condensing)
Storage Environment	• -40 to +100 degrees Celsius • Humidity: 5% to 95% (non-condensing)

*Order Codes: NAT-AMC-ZYNQUP-ECO- <Options>	
<FPGA>-<speed grade + version + temperature range >-<Front-Panel>	
<FPGA>	• 04: ZU4
<Speed Grade>	• A: speed grade 1 • C: speed grade 2
<Version>	• 2: EG
<Temp>	• S: standard
<Front Panel>	• 0: no front panel • 1: single full-size • 2: single mid-size

Info: For other assembly options, please contact NAT.

3. QUICK START

To ensure proper functioning of the **NAT-AMC-ZYNQUP-ECO** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the AMC-Edge-Connector to ensure proper contact when inserting the **NAT-AMC-ZYNQUP-ECO** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAT-AMC-ZYNQUP-ECO** is designed to meet the requirements of µTCA systems but can be plugged onto any ATCA carrier board supporting AMC standards as well. So, the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAT-AMC-ZYNQUP-ECO**, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-AMC-ZYNQUP-ECO**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-swap-capable, if you do not switch off the power.

Ensure that the **NAT-AMC-ZYNQUP-ECO** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-AMC-ZYNQUP-ECO** must meet the following specifications:

+12V / 4A max.

+ 3,3V / 0.15A max.

3.3.2. Hot-Swap

The **NAT-AMC-ZYNQUP-ECO** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-AMC-ZYNQUP-ECO** or the system it is plugged into from damage!

Insertion of a hot-swap-capable Module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-AMC-ZYNQUP-ECO** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAT-AMC-ZYNQUP-ECO** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable Module

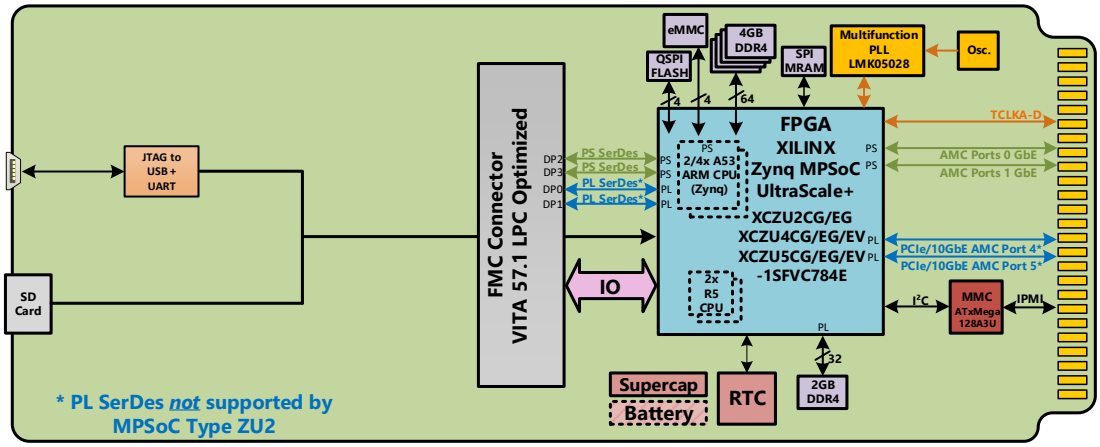
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAT-AMC-ZYNQUP-ECO** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

The **NAT-AMC-ZYNQUP-ECO** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 1 – Block Diagram



Please note: This diagram shows the standard assembly. An alternative assembly with a different SerDes assignment is available as an option. For more information, please refer to chapter 4.6 SerDes Connectivity – Alternative Assembly.

4.1. MPSoC

The central component on the **NAT-AMC-ZYNQUP-ECO** is a Xilinx Zynq MPSoC Ultrascale+ FPGA device (ZynqUP). This SoC provides a powerful general-purpose ARM-CPU, field-programmable hardware accelerators (FPGA, DSP, and GPU), and flexible I/O.

Several different types of MPSoCs are available: ZU2CG/EG, ZU4CG/EG/EV, or ZU5CG/EG/EV.

4.1.1. Processing System (CPU)

The CPU core of the ZynqUP features a dual- or quad-core ARM Cortex-A53 processor as application processing unit and a dual-core ARM Cortex-R5 for real-time processing. The exact number of ARM cores depends on the chosen FPGA type.

4.1.1.1. Memory

The Processing System is accompanied by 4GB DDR4 RAM (x64, 1600-2400Mb/s) with fixed assignment between PS pins and RAM.

On board NAND and NOR flashes can be used for booting and configuring the ZynqUP. The additional MicroSD-Card slot at the front panel can also be used for that purpose, but offers quicker physical access, which is useful during the development. The memory to PS assignment is shown in the table below.

Table 2 – Memory to PS Pin Assignment

QSPI Signal Name	MPSoC Bank 500 Pin#	MPSoC Pin Name
QSPI_IO_0	AG16	PS_MIO4
QSPI_IO_1	V1	PS_MIO1
QSPI_IO_2	U4	PS_MIO2
QSPI_IO_3	Y1	PS_MIO3
QSPI_CS	W4	PS_MIO5
QSPI_SCL	W3	PS_MIO0
MRAM Signal Name	**MPSoC Bank 500 Pin#**	**MPSoC Pin Name**
MRAM_CLK	AC17	PS_MIO12
MRAM_SS	AE18	PS_MIO15
MRAM_MISO	AF18	PS_MIO16
MRAM_MOSI	AC18	PS_MIO17
MicroSD Card Signal Name	**MPSoC Bank 501 Pin#**	**MPSoC Pin Name**
SDIO_1_D0	L20	PS_MIO46
SDIO_1_D1	H21	PS_MIO47
SDIO_1_D2	J21	PS_MIO48
SDIO_1_D3	M18	PS_MIO49
SDIO_1_CMD	M19	PS_MIO50
SDIO_1_CLK	L21	PS_MIO51
eMMC Signal Name	**MPSoC Bank 502 Pin#**	**MPSoC Pin Name**
SDIO_0_D0	B18	PS_MIO67
SDIO_0_D1	C18	PS_MIO68
SDIO_0_D2	D19	PS_MIO69
SDIO_0_D3	C19	PS_MIO70
SDIO_0_D4	B19	PS_MIO71
SDIO_0_D5	G20	PS_MIO72
SDIO_0_D6	G21	PS_MIO73
SDIO_0_D7	D20	PS_MIO74
SDIO_1_CMD	G19	PS_MIO66
SDIO_1_CLK	E19	PS_MIO64

Please note: the assembled memory may vary in size and type due to availability und customer preferences

4.1.2. Programmable Logic (FPGA)

4.1.2.1. Programming

The Programmable Logic of the ZynqUP can be accessed via an onboard Xilinx Programming Module (JTAG-SMT3). It allows to program and debug the FPGA using a Micro-USB Cable, while it serves the same functionality as the Xilinx Platform Cable II programmer. Moreover, it features a side UART channel that is connected to the PS UART0.

For more information, please refer to chapter 7.2 External Reference Documentation.

4.1.2.2. Memory

The Programmable Logic is accompanied by 2GB DDR4 RAM (x32, 1600-2400Mb/s). The memory to FPGA pin assignment is shown in the tables below.

Table 3 – DDR4-Memory to FPGA Pin Assignment – Address CMD, REFCLK, RESET

DDR4 Pin#	FPGA Bank 65 Pin#	DDR4 Pin#	FPGA Bank 65 Pin#
DDRB_A00	W8	DDRB_MCK_p	R8
DDRB_A01	Y8	DDRB_MCK_n	T8
DDRB_A02	U9	DDRB_BA0	H3
DDRB_A03	V9	DDRB_BA1	K4
DDRB_A04	U8	DDRB_ODT	K3
DDRB_A05	V8	DDRB_CKE	L3
DDRB_A06	R7	DDRB_CSn	L2
DDRB_A07	T7	DDRB_BG0	L7
DDRB_A08	R6	DDRB_BG1	L6
DDRB_A09	T6	CLK_DDR4_T_PL_p	M6
DDRB_A10	L1	CLK_DDR4_T_PL_n	L5
DDRB_A11	K1	RSTn_DDRB	N7
DDRB_A12	J1	DDRB_ALERTn	N6
DDRB_A13	H1	DDRB_PAR	P7
DDRB_A14	K2	DDRB_ACTn	P6
DDRB_A15	J2		
DDRB_A16	H4		

Table 4 – DDR4-Memory to FPGA Pin Assignment – DATA and Strobe

DDR4 Pin#	FPGA Bank 64 Pin#	DDR4 Pin#	FPGA Bank 64 Pin#
DDRB_DQ00	AB7	DDRB_DM0	AC9
DDRB_DQ01	AE8	DDRB_DM1	AG9
DDRB_DQ02	AC8	DDRB_DM2	AD5
DDRB_DQ03	AC7	DDRB_DM3	AG4
DDRB_DQ04	AB8	DDRB_DQSO_p	AD7
DDRB_DQ05	AE9	DDRB_DQS0_n	AE7
DDRB_DQ06	AB6	DDRB_DQS1_p	AG6
DDRB_DQ07	AC6	DDRB_DQS1_n	AG5
DDRB_DQ08	AE5	DDRB_DQS2_p	AB2
DDRB_DQ09	AF8	DDRB_DQS2_n	AC2
DDRB_DQ10	AF5	DDRB_DQS3_p	AE2
DDRB_DQ11	AH7	DDRB_DQS3_n	AF2
DDRB_DQ12	AF6		
DDRB_DQ13	AH8		
DDRB_DQ14	AF7		
DDRB_DQ15	AG8		
DDRB_DQ16	AC1		
DDRB_DQ17	AC3		
DDRB_DQ18	AD1		
DDRB_DQ19	AB3		
DDRB_DQ20	AB1		
DDRB_DQ21	AD4		
DDRB_DQ22	AD2		
DDRB_DQ23	AB4		
DDRB_DQ24	AH1		
DDRB_DQ25	AG3		
DDRB_DQ26	AH2		
DDRB_DQ27	AH3		
DDRB_DQ28	AG1		
DDRB_DQ29	AE3		
DDRB_DQ30	AF1		
DDRB_DQ31	AF3		

4.2. PLL and Clocking

The **NAT-AMC-ZYNQUP-ECO** features a multifunctional LMK05028 PLL, which is user-configurable by the FPGA via I²C.

The following figure shows the CLK connections between PLL, FPGA, Backplane, and FMC-Connector. Reference Clock Frequencies are listed in the table below.

Figure 2 – PLL and Clocking

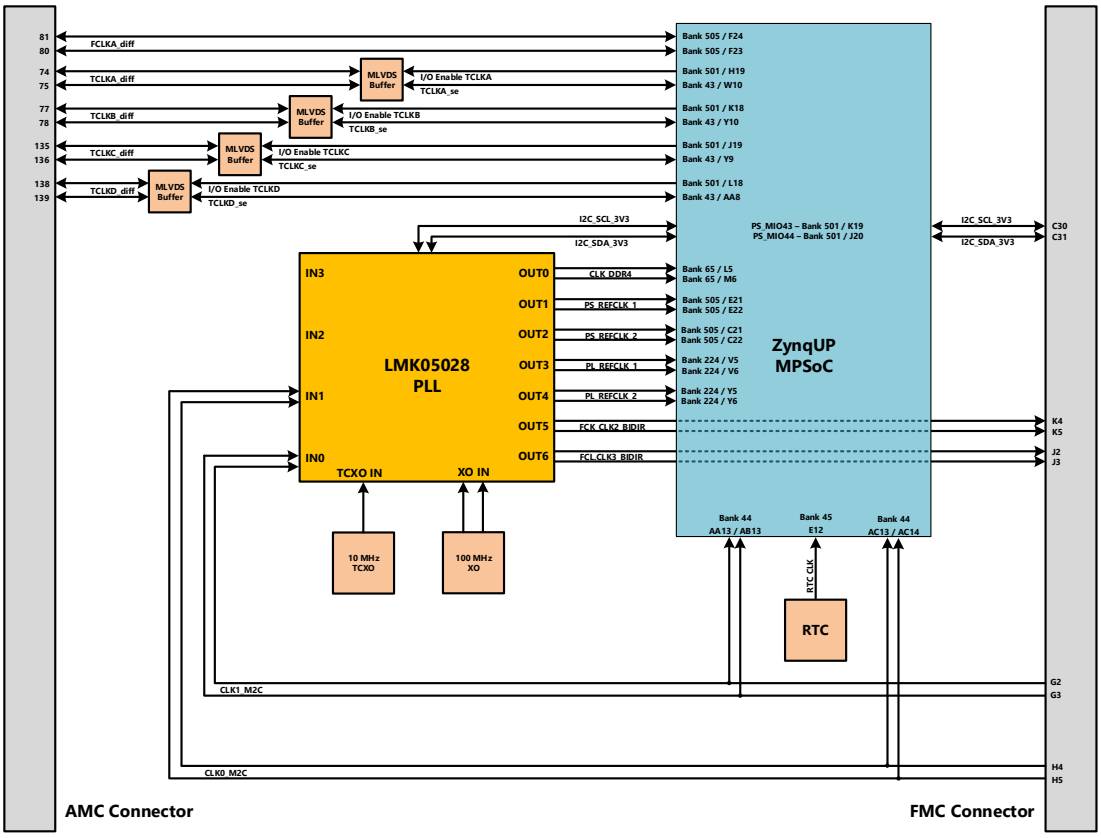


Table 5 – Reference Clock Frequencies

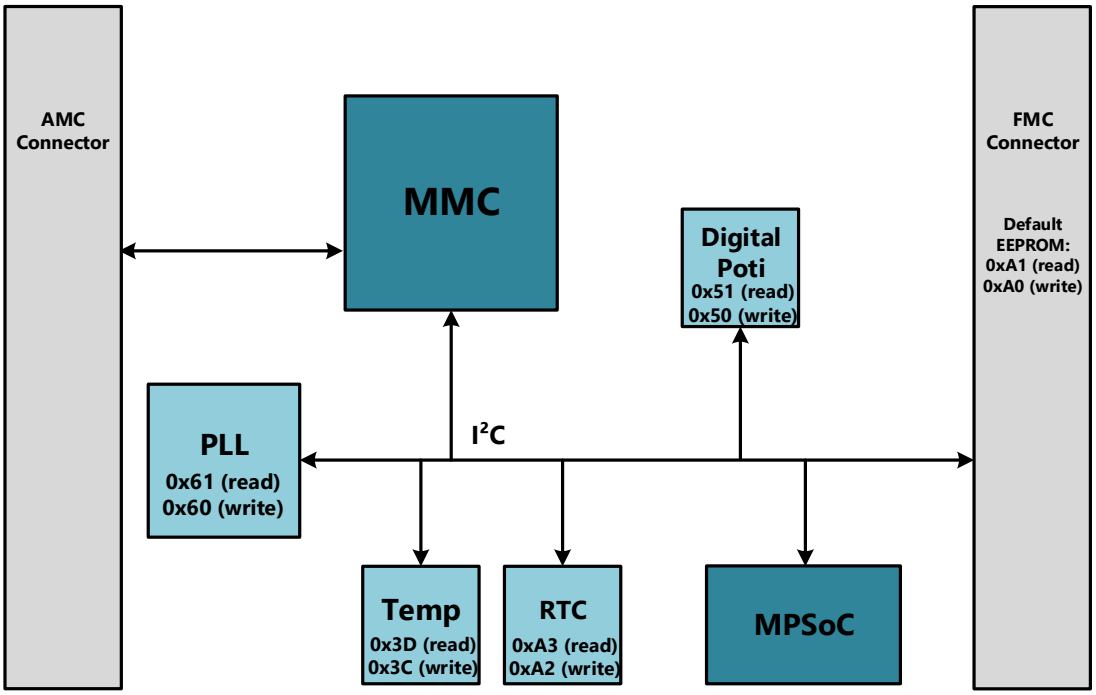
PLL Output	Signal Name	Frequency	Destination
OUT0	CLK_DDR4	125MHz	MPSoC
OUT1	PS_REFCLK_1	125MHz	MPSoC
OUT2	PS_REFCLK_2	125MHz	MPSoC
OUT3	PL_REFCLK_1	156.25MHz	MPSoC
OUT4	PL_REFCLK_2	125MHz	MPSoC
OUT5	FCK_CLK2_BIDIR	125MHz	FMC
OUT6	FCK_CLK3_BIDIR	125MHz	FMC

4.3. IPMB-Interface and I²C-Devices

The **NAT-AMC-ZYNQUP-ECO** implements an IPMB interface consisting of an IPMI-µC (ATXMega128) and a couple of I²C devices connected via I²C.

The following figure shows the architecture in detail.

Figure 3 – IPMB-Interface



The external channel of the temperature sensor monitors the FPGA temperature, the internal channel measures the local PCB temperature.

The IPMI controller also manages the geographical address as requested by the AMC specification.

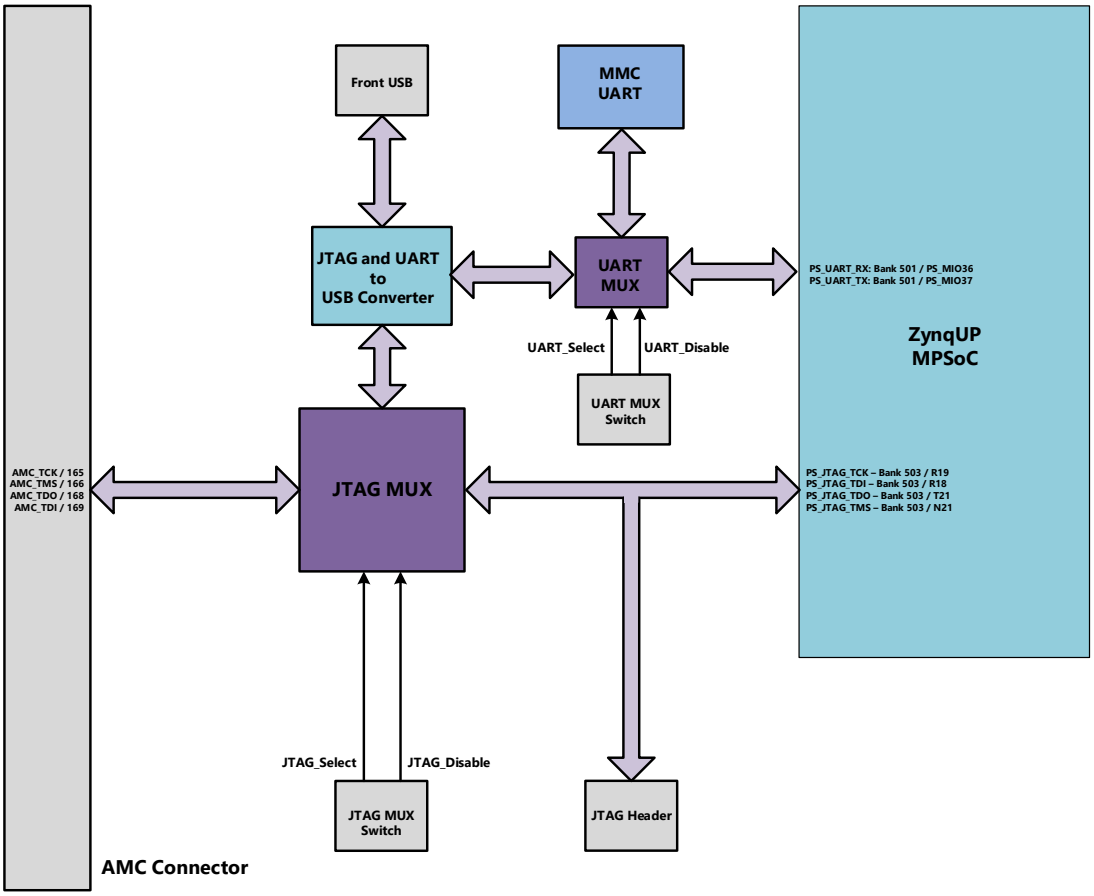
4.4. JTAG and UART

The **NAT-AMC-ZYNQUP-ECO** supports JTAG and serial UART via the front panel USB connector or the on-board JTAG programming header. Both interfaces can be used simultaneously and can be configured using on-board DIP switches.

Configuration of the JTAG Master is possible via the JTAG MUX Switch; for detailed information on this switch, please refer to chapter 5.3.9 SW3: JTAG MUX.

Configuration of the UART Master is possible via the UART MUX Switch; for detailed information on this switch, please refer to chapter 5.3.10 SW4: UART MUX.

Figure 4 – JTAG Architecture



4.5. SerDes Connectivity

The ZynqUP MPSoC interfaces directly to the FMC slot via a VITA 57.1 compliant High Pin Count (HPC) connector, and to the µTCA backplane via its SerDes lanes on AMC Port 0/1 and 4/5.

Please note: The PL SerDes connections are supported by the MPSoC types ZU4 / ZU5 only and are ***not*** available with the ZynqUP type ZU2!

The figures below give an overview of the signal assignment, more details are described in the following tables.

Figure 5 – SerDes Connectivity – Standard Assembly

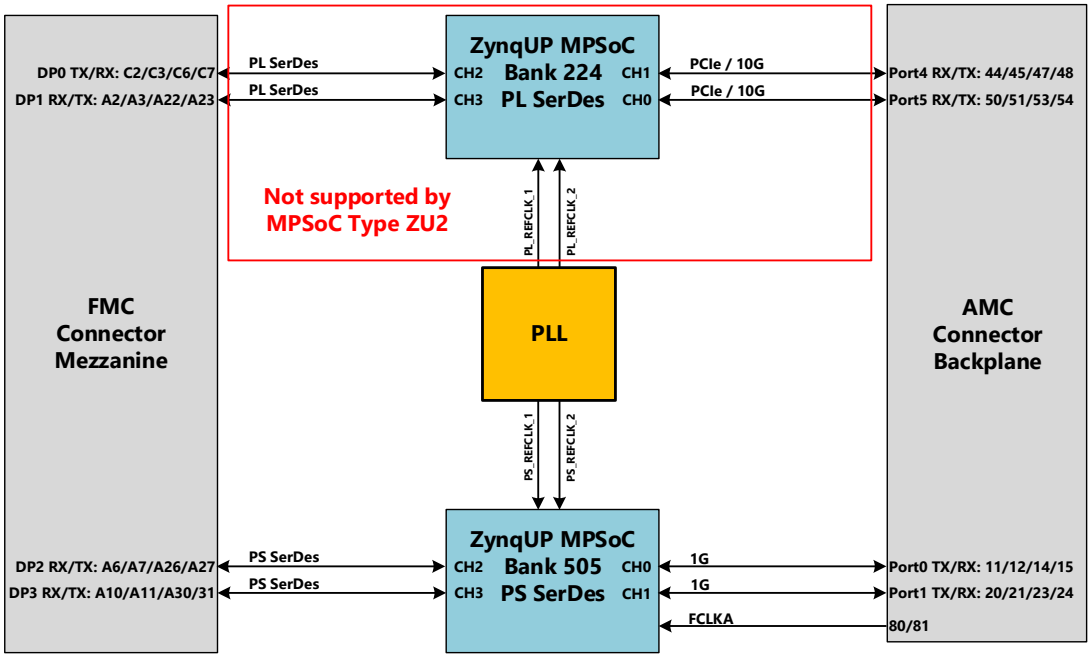


Table 6 – SerDes Connectivity – PL SerDes Bank 224 – Pin Assignment

FMC Connector Pin#	Signal Name	MPSoC Pin#	MPSoC Pin Name
C6	SerDes_PL-RX_0_P	V2	MGTRRXP_2_224
C7	SerDes_PL-RX_0_N	V1	MGTRRXN_2_224
C2	SerDes_PL-TX_0_P	U4	MGTRTXP_2_224
C3	SerDes_PL-TX_0_N	U3	MGTRTXN_2_224
A2	SerDes_PL-RX_1_P	Y2	MGTRRXP_3_224
A3	SerDes_PL-RX_1_N	Y1	MGTRRXN_3_224
A22	SerDes_PL-TX_1_P	W4	MGTRTXP_3_224
A23	SerDes_PL-TX_1_N	W3	MGTRTXN_3_224
AMC Connector Pin#	**Signal Name**	**MPSoC Pin#**	**MPSoC Pin Name**
47	PORT4_RX_P	T2	MGTRRXP1_224
48	PORT4_RX_N	T1	MGTRRXN_1_224
44	PORT4_TX_P	R4	MGTRTXP_1_224
45	PORT4_TX_N	R3	MGTRTXN_1_224
53	PORT5_RX_P	P2	MGTRRXP0_224
54	PORT5_RX_N	P1	MGTRRXN_0_224
50	PORT5_TX_P	N4	MGTRTXP_0_224
51	PORT5_TX_N	N3	MGTRTXN_0_224
PLL Pin#	**Signal Name**	**MPSoC Pin#**	**MPSoC Pin Name**
34	PL_REFCLK_1_P	V6	MGTREFCLK0P_224
33	PL_REFCLK_1_N	V5	MGTREFCLK0N_224
51	PL_REFCLK_2_P	Y6	MGTREFCLK1P_224
52	PL_REFCLK_2_N	Y5	MGTREFCLK1N_224

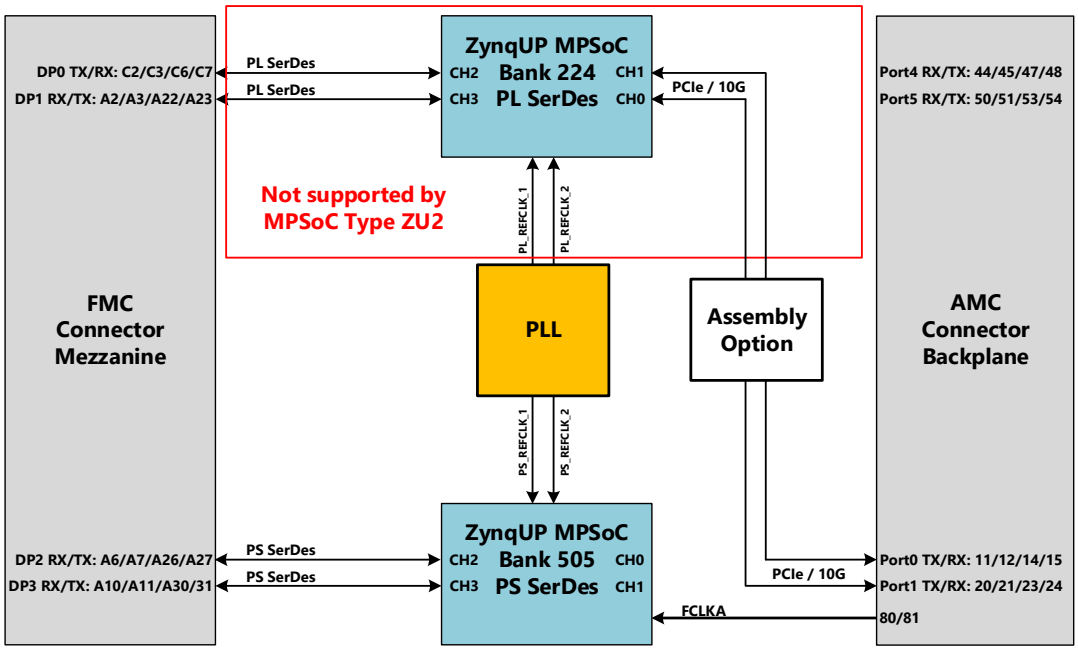
Table 7 – SerDes Connectivity – PS SerDes Bank 505 – Pin Assignment

FMC Connector Pin#	Signal Name	MPSoC Pin#	MPSoC Pin Name
A6	SerDes_PS-RX_2_P	B27	PS_MGTRRXP_2_505
A7	SerDes_PS-RX_2_N	B28	PS_MGTRRXN_2_505
A26	SerDes_PS-TX_2_P	C25	PS_MGTRTXP_2_505
A27	SerDes_PS-TX_2_N	C26	PS_MGTRTXN_2_505
A10	SerDes_PS-RX_3_P	A25	PS_MGTRRXP_3_505
A11	SerDes_PS-RX_3_N	A26	PS_MGTRRXN_3_505
A30	SerDes_PS-TX_3_P	B23	PS_MGTRTXP_3_505
A31	SerDes_PS-TX_3_N	B24	PS_MGTRTXN_3_505
AMC Connector Pin#	**Signal Name**	**MPSoC Pin#**	**MPSoC Pin Name**
14	PORT0_RX_P	F27	PS_MGTRRXP_0_505
15	PORT0_RX_N	F28	PS_MGTRRXN_0_505
11	PORT0_TX_P	E25	PS_MGTRTXP_0_505
12	PORT0_TX_N	E26	PS_MGTRTXN_0_505
23	PORT1_RX_P	D27	PS_MGTRRXP_1_505
24	PORT1_RX_N	D28	PS_MGTRRXN_1_505
20	PORT1_TX_P	D23	PS_MGTRTXP_1_505
21	PORT1_TX_N	D24	PS_MGTRTXN_1_505
80	AMC_FCLKA_P	F23	PS_MGTREFCLK0P_505
81	AMC_FCLKA_P	F24	PS_MGTREFCLK0N_505
PLL Pin#	**Signal Name**	**MPSoC Pin#**	**MPSoC Pin Name**
27	PS_REFCLK_1_P	E21	PS_MGTREFCLK1P_505
26	PS_REFCLK_1_N	E22	PS_MGTREFCLK1N_505
31	PS_REFCLK_2_P	C21	PS_MGTREFCLK2P_505
32	PS_REFCLK_2_N	C22	PS_MGTREFCLK2N_505

4.6. SerDes Connectivity – Alternative Assembly

For some use cases it is preferrable to connect the MPSoC' SerDes interfaces to AMC Ports 0/1. This variant is available as an alternative assembly option.

Figure 6 – SerDes Connectivity – Alternative Assembly



4.7. Port 17-20 MLVDS Bus Lines (Trigger Signals)

MLVDS signals between AMC backplane and MPSoC are implemented by a level shifter. The assignment can be found in the following table.

Table 8 – Port 17-20 MLVDS Connectivity

AMC Pin#	AMC Signal Name	MPSoC Signal Name	MPSoC Bank 65 Data Pin#	MPSoC Bank 64/65 Direction Pin#
141	TRIG_17_RX_n	Port17-Rx-IO	N8	H6
142	TRIG_17_RX_p			
144	TRIG_17_TX_n	Port17-Tx-IO	N9	J6
145	TRIG_17_TX_p			
147	TRIG_18_RX_n	Port18-Rx-IO	L8	H7
148	TRIG_18_RX_p			
150	TRIG_18_TX_n	Port18-Tx-IO	M8	J7
151	TRIG_18_TX_p			
153	TRIG_19_RX_n	Port19-Rx-IO	K5	K7
154	TRIG_19_RX_p			
156	TRIG_19_TX_n	Port19-Tx-IO	P9	K8
157	TRIG_19_TX_p			
159	TRIG_20_RX_n	Port20-Rx-IO	J4	AE4
160	TRIG_20_RX_p			
162	TRIG_20_TX_n	Port20-Tx-IO	J5	AB5
163	TRIG_20_TX_p			

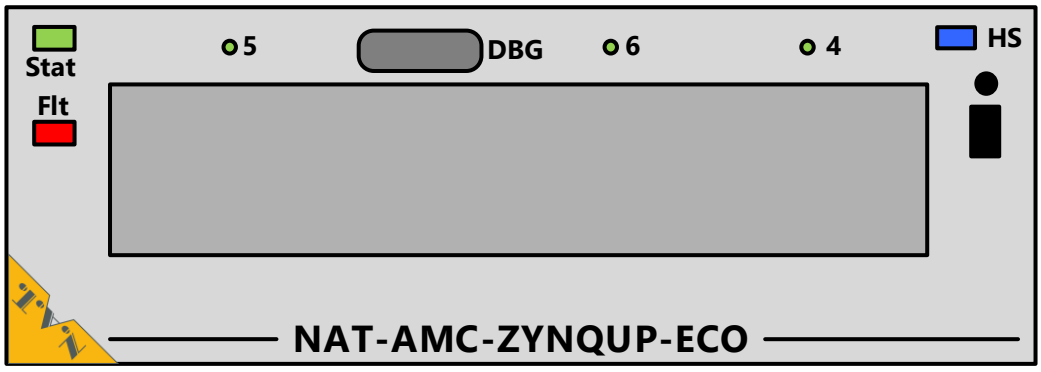
The level shifting is performed in two steps: the conversion from differential to single-ended signal standard is executed by a TI DS91M040 MLVDS transceiver. A TI SN74AVC2T245 bus transceiver translates from 3.3V to 1.2V voltage level.

5. HARDWARE

5.1. Front Panel and LEDs

The front plate appearance and the labelling vary depending on the number and variant(s) of installed FMCs. The figure below shows the full-size version of the **NAT-AMC-ZYNQUP-ECO** carrier board.

Figure 7 – Front Panel – Full Size - preliminary



Colour, behaviour, and function of the front panel LEDs are described in the table below.

Table 9 – LED Functionality

LED	Color	Signal Level / Pins	Function
4 (User)	Green	Bank 501 – J16	User defined – PS_MIO_32
5 (User)	Green	Bank 501 – L16	User defined – PS_MIO_33
6 (User)	Green	Bank 503 – M21	PS_done
HS (Hot Swap)	Blue ON	n/a	AMC Management power (3V3) present Ready for hot-swap
	Blue Blinking	n/a	IPMI-Controller disables payload power
	OFF	n/a	Payload Power (12V) present
Stat (User)	Green	MMC	AMC status information
	Yellow		
Flt (Fault Indication)	Red ON	MMC	Board over temperature or error during board initialization
	OFF		Normal operation

5.2. AMC Port Definition

Table 10 – AMC Port Definition – Standard Assembly

Connector Region		AMC Port #	Signal
Basic Side	Clocks	CLK1/TCLKA	Telecom Clock
		CLK2/TCLKB	Telecom Clock
		CLK3/TCLKC	Telecom Clock
		CLK4/TCLKD	Telecom Clock
		CLK5/FCLKA	Fabric Clock
	Common Options	0	GbE
		1	
		2	nc
		3	
	Fat Pipe	4	PCIe / Ethernet
		5	
		6	nc
		7	
Extended Side	Extended Fat Pipe	8	nc
		9	
		10	
		11	
	Extended Options	12	nc
		13	
		14	
		15	
		16	
		17	
		18	
		19	
		20	

Table 11 – AMC Port Definition – Alternative Assembly

Connector Region		AMC Port #	Signal
Basic Side	Clocks	CLK1/TCLKA	Telecom Clock
		CLK2/TCLKB	Telecom Clock
		CLK3/TCLKC	Telecom Clock
		CLK4/TCLKD	Telecom Clock
		CLK5/FCLKA	Fabric Clock
	Common Options	0	PCIe / Ethernet
		1	
		2	nc
		3	
	Fat Pipe	4	nc
		5	
		6	nc
		7	
Extended Side	Extended Fat Pipe	8	nc
		9	
		10	
		11	
	Extended Options	12	nc
		13	
		14	
		15	
		16	
		17	
		18	
		19	
		20	

5.3. Component-, Connector-, and Switch-Location

Figure 8 – Location Diagram – Top

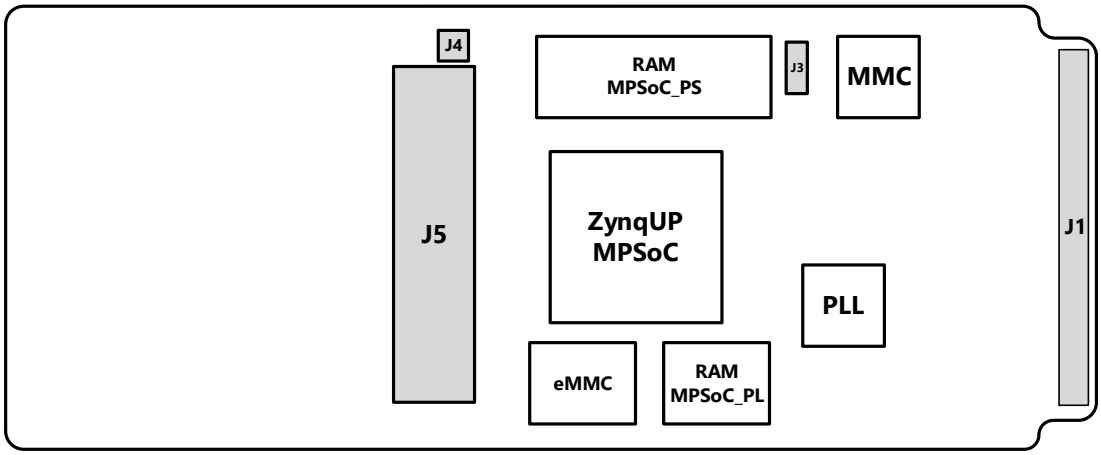
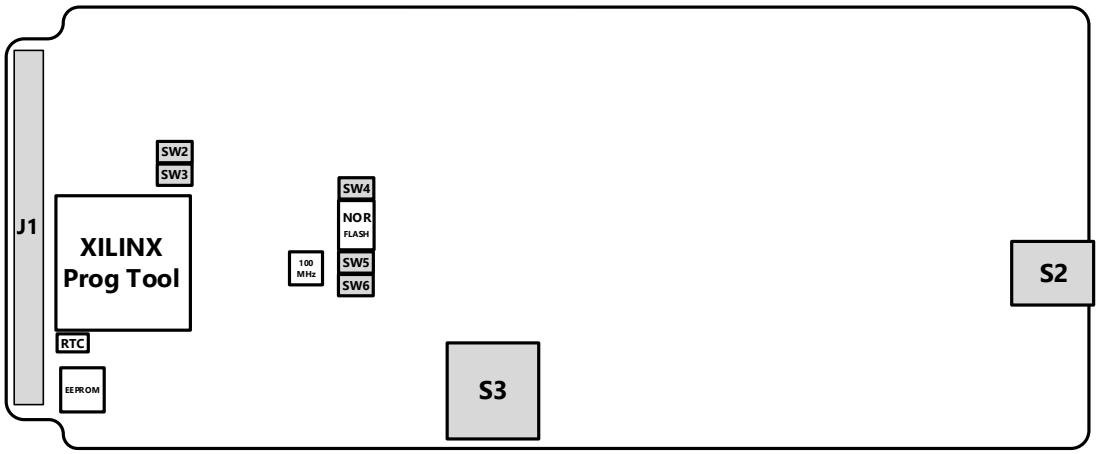


Figure 9 – Location Diagram – Bottom



Connectors on top side: drawings imply the board is orientated with the AMC Edge Connector to the right side

Connectors on bottom side: drawings imply the board is orientated with the AMC Edge Connector to the left side

Please refer to the following tables to look up the connector pin assignment of the **NAT-AMC-ZYNQUP-ECO**.

5.3.1. J1: AMC Connector

Figure 10 – J1: AMC-Connector (top view)

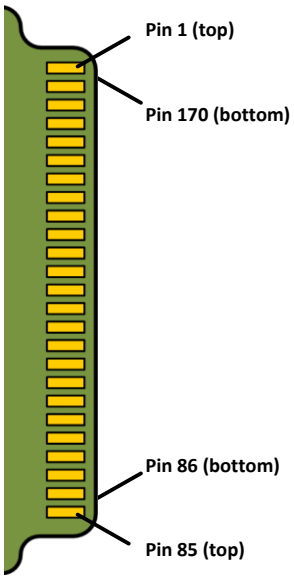


Table 12 – J1A: AMC-Connector Top – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	12V_PP_AMC	AMC_TDI	169
3	/AMC_PS1	AMC_TDO	168
4	3.3V_MP	nc	167
5	AMC_GA0	AMC_TMS	166
6	nc	AMC_TCK	165
7	GND	GND	164
8	nc	TRIG_20_TX_p	163
9	12V_PP_AMC	TRIG_20_TX_n	162
10	GND	GND	161
11	PORT0-Tx_p	TRIG_20_RX_p	160
12	PORT0-Tx_n	TRIG_20_RX_n	159
13	GND	GND	158
14	PORT0-Rx_p	TRIG_19_TX_p	157
15	PORT0-Rx_n	TRIG_19_TX_n	156
16	GND	GND	155
17	AMC_GA1	TRIG_19_RX_p	154
18	12V_PP_AMC	TRIG_19_RX_n	153
19	GND	GND	152
20	PORT1-Tx_p	TRIG_18_TX_p	151
21	PORT1-Tx_n	TRIG_18_TX_n	150
22	GND	GND	149
23	PORT1-Rx_p	TRIG_18_RX_p	148

Pin #	Signal	Signal	Pin #
24	PORT1-Rx_n	TRIG_18_RX_n	147
25	GND	GND	146
26	AMC_GA2	TRIG_17_TX_p	145
27	12V_PP_AMC	TRIG_17_TX_n	144
28	GND	GND	143
29	nc	TRIG_17_RX_p	142
30	nc	TRIG_17_RX_n	141
31	GND	GND	140
32	nc	AMC_TCLKD_p	139
33	nc	AMC_TCKLD_n	138
34	GND	GND	137
35	nc	AMC_TCLKC_p	136
36	nc	AMC_TCKLC_n	135
37	GND	GND	134
38	nc	nc	133
39	nc	nc	132
40	GND	GND	131
41	AMC_ENABLEn	nc	130
42	12V_PP_AMC	nc	129
43	GND	GND	128
44	PORT4-Tx_p	nc	127
45	PORT4-Tx_n	nc	126
46	GND	GND	125
47	PORT4-Rx_p	nc	124
48	PORT4-Rx_n	nc	123
49	GND	GND	122
50	PORT5-Tx_p	nc	121
51	PORT5-Tx_n	nc	120
52	GND	GND	119
53	PORT5-Rx_p	nc	118
54	PORT5-Rx_n	nc	117
55	GND	GND	116
56	AMC_SCL	nc	115
57	12V_PP_AMC	nc	114
58	GND	GND	113
59	nc	nc	112
60	nc	nc	111
61	GND	GND	110
62	nc	nc	109
63	nc	nc	108
64	GND	GND	107
65	nc	nc	106
66	nc	nc	105
67	GND	GND	104
68	nc	nc	103
69	nc	nc	102
70	GND	GND	101
71	AMC_SDA	nc	100
72	12V_PP_AMC	nc	99

Pin #	Signal	Signal	Pin #
73	GND	GND	98
74	AMC_TCLKA_p	nc	97
75	AMC_TCKLA_n	nc	96
76	GND	GND	95
77	AMC_TCLKB_p	nc	94
78	AMC_TCKLB_n	nc	93
79	GND	GND	92
80	AMC_FCLKA_p	nc	91
81	AMC_FCKLA_n	nc	90
82	GND	GND	89
83	/AMC_PS0	nc	88
84	12V_PP_AMC	nc	87
85	GND	GND	86

5.3.2. J2: Microcontroller Programming Header

Connector J2 features a programming interface for the Atmel microcontroller.

Figure 11 – J2: Microcontroller Programming Interface

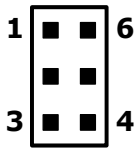


Table 13 – J2: Microcontroller Programming Header

Pin #	Signal	Signal	Pin #
1	PDI_CLK	GND	6
2	nc	nc	5
3	PDI_DATA	+3.3V_MP	4

5.3.3. J3: JTAG Programming Header

Connector J3 offers a JTAG programming interface.

Figure 12 – J3: JTAG Programming Header

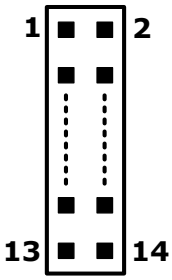


Table 14 – J3: JTGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	JTAG_DISABLE	V_PROG	2
3	GND	PS_JTAG_TMS	4
5	GND	PS_JTAG_TCK	6
7	GND	PS_JTAG_TDI	8
9	GND	PS_JTAG_TDO	10
11	GND	nc	12
13	GND	PS_SRST_B	14

5.3.4. J5: FMC Connector

Connector J5 connects to the FMC mezzanine board

Table 15 – J5: FMC Connector – Overview

	A	B	C	D	E	F	G	H	J	K
1	GND	nc	GND	FSIG.PG_C2M	GND	FSIG.PG_M2C	GND	FVREF.VREF_A_M2C	GND	FVREF.VREF_B_M2C
2	SerDes_PL-RX_1_p	GND	SerDes_PL-TX_0_p	GND	HA.HA01_CC_p	GND	FCK.CLK1_M2C_p	FSIG.PRSNT_M2C_L	FCK.CLK3_BIDIR_p	GND
3	SerDes_PL-RX_1_n	GND	SerDes_PL-TX_0_n	GND	HA.HA01_CC_n	GND	FCK.CLK1_M2C_n	GND	FCK.CLK3_BIDIR_n	GND
4	GND	nc	GND	FGC.CLK0_M2C_p	GND	HA.HA00_CC_p	GND	FCK.CLK0_M2C_p	GND	FCL.CLK2_BIDIR_p
5	GND	nc	GND	FGC.CLK0_M2C_n	GND	HA.HA00_CC_n	GND	FCK.CLK0_M2C_n	GND	FCL.CLK2_BIDIR_n
6	SerDes_PS-RX_2_p	GND	SerDes_PL-RX_0_p	GND	HA.HA05_p	GND	LA.LA00_CC_p	GND	HA.HA03_p	GND
7	SerDes_PS-RX_2_n	GND	SerDes_PL-RX_0_n	GND	HA.HA05_n	HA.HA04_p	LA.LA00_CC_n	LA.LA02_p	HA.HA03_n	HA.HA02_p
8	GND	nc	GND	LA.LA01_CC_p	GND	HA.HA04_n	GND	LA.LA02_n	GND	HA.HA02_n
9	GND	nc	GND	LA.LA01_CC_n	HA.HA09_p	GND	LA.LA03_p	GND	HA.HA07_p	GND
10	SerDes_PS-RX_3_p	GND	LA.LA06_p	GND	HA.HA09_n	HA.HA08_p	LA.LA03_n	LA.LA04_p	HA.HA07_n	HA.HA06_p
11	SerDes_PS-RX_3_n	GND	LA.LA06_n	LA.LA05_p	GND	HA.HA08_n	GND	LA.LA04_n	GND	HA.HA06_n

	A	B	C	D	E	F	G	H	J	K
12	GND	nc	GND	LA.LA05_n	HA.HA13_p	GND	LA.LA08_p	GND	HA.HA11_p	GND
13	GND	nc	GND	GND	HA.HA13_n	HA.HA12_p	LA.LA08_n	LA.LA07_p	HA.HA11_n	HA.HA10_p
14	nc	GND	LA.LA10_p	LA.LA09_p	GND	HA.HA12_n	GND	LA.LA07_n	GND	HA.HA10_n
15	nc	GND	LA.LA10_n	LA.LA09_n	HA.HA16_p	GND	LA.LA12_p	GND	HA.HA14_p	GND
16	GND	nc	GND	GND	HA.HA16_n	HA.HA15_p	LA.LA12_n	LA.LA11_p	HA.HA14_n	HA.HA17_CC_p
17	GND	nc	GND	LA.LA13_p	GND	HA.HA15_n	GND	LA.LA11_n	GND	HA.HA17_CC_n
18	nc	GND	LA.LA14_p	LA.LA13_n	HA.HA20_p	GND	LA.LA16_p	GND	HA.HA18_p	GND
19	nc	GND	LA.LA14_n	GND	HA.HA20_n	HA.HA19_p	LA.LA16_n	LA.LA15_p	HA.HA18_n	HA.HA21_p
20	GND	FGC.CLK1_M2C_p	GND	LA.LA17_CC_p	GND	HA.HA19_n	GND	LA.LA15_n	GND	HA.HA21_n
21	GND	FGC.CLK1_M2C_n	GND	LA.LA17_CC_n	nc	GND	LA.LA20_p	GND	HA.HA22_p	GND
22	SerDes_PL-TX_1_p	GND	LA.LA18_CC_p	GND	nc	nc	LA.LA20_n	LA.LA19_p	HA.HA22_n	HA.HA23_p
23	SerDes_PL-TX_1_n	GND	LA.LA18_CC_n	LA.LA23_p	GND	nc	GND	LA.LA19_n	GND	HA.HA23_n
24	GND	nc	GND	LA.LA23_n	nc	GND	LA.LA22_p	GND	nc	GND
25	GND	nc	GND	GND	nc	nc	LA.LA22_n	LA.LA21_p	nc	nc
26	SerDes_PS-TX_2_p	GND	LA.LA27_p	LA.LA26_p	GND	nc	GND	LA.LA21_n	GND	nc
27	SerDes_PS-TX_2_n	GND	LA.LA27_n	LA.LA26_n	nc	GND	LA.LA25_p	GND	nc	GND
28	GND	nc	GND	GND	nc	nc	LA.LA25_n	LA.LA24_p	nc	nc
29	GND	nc	GND	FPGA_TCK	GND	nc	GND	LA.LA24_n	GND	nc
30	SerDes_PS-TX_3_p	GND	FSIG.SCL	FPGA_TDI	nc	GND	LA.LA29_p	GND	nc	GND

	A	B	C	D	E	F	G	H	J	K
31	SerDes_PS-TX_3_n	GND	FSIG_SDA	FPGA_TDO	nc	nc	LA.LA29_n	LA.LA28_p	nc	nc
32	GND	nc	GND	3P3VAUX	GND	nc	GND	LA.LA28_n	GND	nc
33	GND	nc	GND	FPGA_TMS	nc	GND	LA.LA31_p	GND	nc	GND
34	nc	GND	FSIG.GA0	PS SRST_B	nc	nc	LA.LA31_n	LA.LA30_p	nc	nc
35	nc	GND	12POV	FSIG.GA1	GND	nc	GND	LA.LA30_n	GND	nc
36	GND	nc	GND	3P3V	nc	GND	LA.LA33_p	GND	nc	GND
37	GND	nc	12POV	GND	nc	nc	LA.LA33_n	LA.LA32_p	nc	nc
38	nc	GND	GND	3P3V	GND	nc	GND	LA.LA32_n	GND	nc
39	nc	GND	3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C	GND
40	GND	nc	GND	3P3V	GND	FMC_VADJ	GND	FMC_VADJ	GND	VIO_B_M2C

Details about the pin assignment are given in the following tables. Generally, the designation of 'Pin Name' and 'Pin#' refers to an FPGA pin. In case the signal contacts to another part (PLL or microcontroller), this is labelled separately.

Note: The polarity of several FMC signals to FPGA interface pins is swapped intentionally! This is indicated by **bold lettering**!

Table 16 – J5A: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
A1	GND	GND				
A2	DP1_M2C_P	SerDes_PL-RX_1_p	224	n/a	MGTRRXP_3_224	Y2
A3	DP1_M2C_N	SerDes_PL-RX_1_n			MGTRRXN_3_224	Y1
A4	GND	GND				
A5	GND	GND				
A6	DP2_M2C_P	SerDes_PS-RX_2_p	505	n/a	PS_MGTRRXP_2_505	B27
A7	DP2_M2C_N	SerDes_PS-RX_2_n			PS_MGTRRXN_2_505	B28
A8	GND	GND				
A9	GND	GND				
A10	DP3_M2C_P	SerDes_PS-RX_3_p	505	n/a	PS_MGTRRXP_3_505	A25
A11	DP3_M2C_N	SerDes_PS-RX_3_n			PS_MGTRRXN_3_505	A26
A12	GND	GND				
A13	GND	GND				
A14	DP4_M2C_P	nc				
A15	DP4_M2C_N	nc				
A16	GND	GND				
A17	GND	GND				
A18	DP5_M2C_P	nc				
A19	DP5_M2C_N	nc				
A20	GND	GND				
A21	GND	GND				
A22	DP1_C2M_P	SerDes_PL-TX_1_p	224	n/a	MGTRTXP_3_224	W4
A23	DP1_C2M_N	SerDes_PL-TX_1_n			MGTRTXN_3_224	W3
A24	GND	GND				
A25	GND	GND				
A26	DP2_C2M_P	SerDes_PS-TX_2_p	505	n/a	PS_MGTRTXP_2_505	C25
A27	DP2_C2M_N	SerDes_PS-TX_2_n			PS_MGTRTXN_2_505	C26

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
A28	GND	GND				
A29	GND	GND				
A30	DP3_C2M_P	SerDes_PS-TX_3_p	505	n/a	PS_MGTRTXP_3_505	B23
A31	DP3_C2M_N	SerDes_PS-TX_3_n			PS_MGTRTXN_3_505	B24
A32	GND	GND				
A33	GND	GND				
A34	DP4_C2M_P	nc				
A35	DP4_C2M_N	nc				
A36	GND	GND				
A37	GND	GND				
A38	DP5_C2M_P	nc				
A39	DP5_C2M_N	nc				
A40	GND	GND				

Table 17 – J5B: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
B1	CLK_DIR	nc				
B2	GND	GND				
B3	GND	GND				
B4	DP9_M2C_P	nc				
B5	DP9_M2C_N	nc				
B6	GND	GND				
B7	GND	GND				
B8	DP8_M2C_P	nc				
B9	DP8_M2C_N	nc				
B10	GND	GND				
B11	GND	GND				
B12	DP7_M2C_P	nc				
B13	DP7_M2C_N	nc				
B14	GND	GND				
B15	GND	GND				
B16	DP6_M2C_P	nc				
B17	DP6_M2C_N	nc				
B18	GND	GND				
B19	GND	GND				
B20	**GBTCLK1_M2C_P**	**FGC.CLK1_M2C_P**	**46**	**FMC_VADJ**	**IO_L8N_HDGC_AD4N_46**	**E15**
B21	**GBTCLK1_M2C_N**	**FGC.CLK1_M2C_N**			**IO_L8P_HDGC_AD4N_46**	**F15**
B22	GND	GND				
B23	GND	GND				
B24	DP9_C2M_P	nc				
B25	DP9_C2M_N	nc				
B26	GND	GND				
B27	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
B28	DP8_C2M_P	nc				
B29	DP8_C2M_N	nc				
B30	GND	GND				
B31	GND	GND				
B32	DP7_C2M_P	nc				
B33	DP7_C2M_N	nc				
B34	GND	GND				
B35	GND	GND				
B36	DP6_C2M_P	nc				
B37	DP6_C2M_N	nc				
B38	GND	GND				
B39	GND	GND				
B40	RES0	nc				

Table 18 – J5C: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
C1	GND	GND				
C2	DP0_C2M_P	SerDes_PL-TX_0_p	224	n/a	MGTRTXP_2_224	U4
C3	DP0_C2M_N	SerDes_PL-TX_0_n			MGTRTXN_2_224	U3
C4	GND	GND				
C5	GND	GND				
C6	DP0_M2C_P	SerDes_PL-RX_0_p	224	n/a	MGTRRXP_2_224	V2
C7	DP0_M2C_N	SerDes_PL-RX_0_n			MGTRRXN_2_224	V1
C8	GND	GND				
C9	GND	GND				
C10	**LA06_P**	**LA.LA06_p**	**46**	**FMC_VADJ**	**IO_L11N_AD1N_46**	**J14**
C11	**LA06_N**	**LA.LA06_n**			**IO_L11P_AD1P_46**	**K14**
C12	GND	GND				
C13	GND	GND				
C14	LA10_P	LA.LA10_p	66	FMC_VADJ	IO_L1P_T0L_N0_DBC _66	G1
C15	LA10_N	LA.LA10_n			IO_L1N_T0L_N1_DBC _66	F1
C16	GND	GND				
C17	GND	GND				
C18	**LA14_P**	**LA.LA14_p**	**66**	**FMC_VADJ**	**IO_L5N_T0U_N9_AD14N_66**	**E3**
C19	**LA14_N**	**LA.LA14_n**			**IO_L5P_T0U_N8_AD14P_66**	**E4**
C20	GND	GND				
C21	GND	GND				
C22	**LA18_P_CC**	**LA.LA18_CC_p**	**66**	**FMC_VADJ**	**IO_L14N_T2L_N3_GC _66**	**D5**
C23	**LA18_N_CC**	**LA.LA18_CC_n**			**IO_L14P_T2L_N2_GC _66**	**E5**
C24	GND	GND				
C25	GND	GND				
C26	LA27_P	LA.LA27_p	66	FMC_VADJ	IO_T3U_N12_66	C7
C27	LA27_N	LA.LA27_n			IO_T2U_N12_66	E7

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
C28	GND	GND				
C29	GND	GND				
C30	SCL	FSIG.SCL	500	3V3	PS_MIO43	K19
C31	SDA	FSIG_SDA			PS_MIO44	J20
C32	GND	GND				
C33	GND	GND				
C34	GA0	FSIG.GA0				
C35	12POV	12POV				
C36	GND	GND				
C37	12POV	12POV				
C38	GND	GND				
C39	3P3V	3P3V				
C40	GND	GND				

Table 19 – J5D: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
D1	PG_C2M	FSIG.PG_C2M			PC3 (µC)	18
D2	GND	GND				
D3	GND	GND				
D4	GBTCLK0_M2C_P	FGC.CLK0_M2C_p	46	FMC_VADJ	IO_L7P_HDGC_AD5P_46	G13
D5	GBTCLK0_M2C_N	FGC.CLK0_M2C_n			IO_L7N_HDGC_AD5N_46	F13
D6	GND	GND				
D7	GND	GND				
D8	LA01_P_CC	LA.LA01_CC_p	66	FMC_VADJ	IO_L12P_T1U_N10_GC_66	C3
D9	LA01_N_CC	LA.LA01_CC_n			IO_L12N_T1U_N11_GC_66	C2
D10	GND	GND				
D11	LA05_P	LA.LA05_p	46	FMC_VADJ	IO_L12P_AD0P_46	L14
D12	LA05_N	LA.LA05_n			IO_L12N_AD0N_46	L13
D13	GND	GND				
D14	LA09_P	LA.LA09_p	46	FMC_VADJ	IO_L4P_AD8P_46	C14
D15	LA09_N	LA.LA09_n			IO_L4N_AD8N_46	C13
D16	GND	GND				
D17	LA13_P	LA.LA13_p	66	FMC_VADJ	IO_L4P_T0U_N6_DBC_AD7P_66	G3
D18	LA13_N	LA.LA13_n			IO_L4N_T0U_N7_DBC_AD7N_66	F3
D19	GND	GND				
D20	**LA17_P_CC**	**LA.LA17_CC_p**	**66**	**FMC_VADJ**	**IO_L13N_T2L_N1_GC_QBC_66**	**D6**
D21	**LA17_N_CC**	**LA.LA17_CC_n**			**IO_L13P_T2L_N0_GC_QBC_66**	**D7**
D22	GND	GND				
D23	**LA23_P**	**LA.LA23_p**	**66**	**FMC_VADJ**	**IO_L15N_T2L_N5_AD11N_66**	**F6**
D24	**LA23_N**	**LA.LA23_n**			**IO_L15P_T2L_N4_AD11P_66**	**G6**
D25	GND	GND				
D26	**LA26_P**	**LA.LA26_p**	**66**	**FMC_VADJ**	**IO_L18N_T2U_N11_AD2N_66**	**D9**
D27	**LA26_N**	**LA.LA26_n**			**IO_L18P_T2U_N10_AD2P_66**	**E9**

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
D28	GND	GND				
D29	TCK	FPGA_TCK				
D30	TDI	FPGA_TDI				
D31	TDO	FPGA_TDO				
D32	3P3VAUX	3P3VAUX				
D33	TMS	FPGA_TMS				
D34	TRST_L	PS SRST_B	503	3V3	PS_SRST_B	N19
D35	GA1	FSIG.GA1				
D36	3P3V	3P3V				
D37	GND	GND				
D38	3P3V	3P3V				
D39	GND	GND				
D40	3P3V	3P3V				

Table 20 – J5E: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
E1	GND	GND				
E2	HA01_P_CC	HA.HA01_CC_p	44	VIO_B_M2C	IO_L6P_HDGC_44	AC14
E3	HA01_N_CC	HA.HA01_CC_n			IO_L6N_HDGC_44	AC13
E4	GND	GND				
E5	GND	GND				
E6	HA05_P	HA.HA05_p	44	VIO_B_M2C	IO_L4P_AD12P_44	AE13
E7	HA05_N	HA.HA05_n			IO_L4N_AD12N_44	AF13
E8	GND	GND				
E9	**HA09_P**	**HA.HA09_p**	**44**	**VIO_B_M2C**	**IO_L11N_AD9N_44**	**W11**
E10	**HA09_N**	**HA.HA09_n**			**IO_L11P_AD9P_44**	**W12**
E11	GND	GND				
E12	HA13_P	HA.HA13_p	45	VIO_B_M2C	IO_L3P_AD13P_45	H11
E13	HA13_N	HA.HA13_n			IO_L3N_AD13N_45	G10
E14	GND	GND				
E15	HA16_P	HA.HA16_p	45	VIO_B_M2C	IO_L6P_HDGC_45	F12
E16	HA16_N	HA.HA16_n			IO_L6N_HDGC_45	F11
E17	GND	GND				
E18	HA20_P	HA.HA20_p	45	VIO_B_M2C	IO_L9P_AD11P_45	C11
E19	HA20_N	HA.HA20_n			IO_L9N_AD11N_45	B10
E20	GND	GND				
E21	HB03_P	nc				
E22	HB03_N	nc				
E23	GND	GND				
E24	HB05_P	nc				
E25	HB05_N	nc				
E26	GND	GND				
E27	HB09_P	nc				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
E28	HB09_N	nc				
E29	GND	GND				
E30	HB13_P	nc				
E31	HB13_N	nc				
E32	GND	GND				
E33	HB19_P	nc				
E34	HB19_N	nc				
E35	GND	GND				
E36	HB21_P	nc				
E37	HB21_N	nc				
E38	GND	GND				
E39	VADJ	FMC_VADJ				
E40	GND	GND				

Table 21 – J5F: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
F1	PG_M2C	FSIG.PG_M2C			PD7 (µC)	32
F2	GND	GND				
F3	GND	GND				
F4	HA00_P_CC	HA.HA00_CC_p	44	VIO_B_M2C	IO_L5P_HDGC_44	AD15
F5	HA00_N_CC	HA.HA00_CC_n			IO_L5N_HDGC_44	AD14
F6	GND	GND				
F7	HA04_P	HA.HA04_p	44	VIO_B_M2C	IO_L3P_AD13P_44	AG13
F8	HA04_N	HA.HA04_n			IO_L3N_AD13N_44	AH13
F9	GND	GND				
F10	**HA08_P**	**HA.HA08_p**	**44**	**VIO_B_M2C**	**IO_L10N_AD10N_44**	**Y13**
F11	**HA08_N**	**HA.HA08_n**			**IO_L10P_AD10P_44**	**Y14**
F12	GND	GND				
F13	HA12_P	HA.HA12_p	45	VIO_B_M2C	IO_L2P_AD14P_45	K13
F14	HA12_N	HA.HA12_n			IO_L2N_AD14N_45	K12
F15	GND	GND				
F16	HA15_P	HA.HA15_p	45	VIO_B_M2C	IO_L5P_HDGC_45	G11
F17	HA15_N	HA.HA15_n			IO_L5N_HDGC_45	F10
F18	GND	GND				
F19	HA19_P	HA.HA19_p	45	VIO_B_M2C	IO_L8P_HDGC_45	E12
F20	HA19_N	HA.HA19_n			IO_L8N_HDGC_45	E11
F21	GND	GND				
F22	HB02_P	nc				
F23	HB02_N	nc				
F24	GND	GND				
F25	HB04_P	nc				
F26	HB04_N	nc				
F27	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
F28	HB08_P	nc				
F29	HB08_N	nc				
F30	GND	GND				
F31	HB12_P	nc				
F32	HB12_N	nc				
F33	GND	GND				
F34	HB16_P	nc				
F35	HB16_N	nc				
F36	GND	GND				
F37	HB20_P	nc				
F38	HB20_N	nc				
F39	GND	GND				
F40	VADJ	FMC_VADJ				

Table 22 – J5G: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
G1	GND	GND				
G2	CLK1_M2C_P	FCK.CLK1_M2C_p			IN0_P (PLL)	1
G3	CLK1_M2C_N	FCK.CLK1_M2C_n			IN0_N (PLL)	2
G4	GND	GND				
G5	GND	GND				
G6	LA00_P_CC	LA.LA00_CC_p	66	FMC_VADJ	IO_L11P_T1U_N8_GC_66	D4
G7	LA00_N_CC	LA.LA00_CC_n			IO_L11N_T1U_N9_GC_66	C4
G8	GND	GND				
G9	LA03_P	LA.LA03_p	46	FMC_VADJ	IO_L2P_AD10P_46	B14
G10	LA03_N	LA.LA03_n			IO_L2N_AD10N_46	A14
G11	GND	GND				
G12	**LA08_P**	**LA.LA08_p**	**46**	**FMC_VADJ**	**IO_L9N_AD3N_46**	**G14**
G13	**LA08_N**	**LA.LA08_n**			**IO_L9P_AD3P_46**	**G15**
G14	GND	GND				
G15	LA12_P	LA.LA12_p	66	FMC_VADJ	IO_L3P_T0L_N4_AD15P_66	F2
G16	LA12_N	LA.LA12_n			IO_L3N_T0L_N5_AD15N_66	E2
G17	GND	GND				
G18	LA16_P	LA.LA16_p	66	FMC_VADJ	IO_T1U_N12_66	D2
G19	LA16_N	LA.LA16_n			IO_T0U_N12_VRP_66	G4
G20	GND	GND				
G21	**LA20_P**	**LA.LA20_p**	**66**	**FMC_VADJ**	**IO_L8N_T1L_N3_AD5N_66**	**A1**
G22	**LA20_N**	**LA.LA20_n**			**IO_L8P_T1L_N2_AD5P_66**	**A2**
G23	GND	GND				
G24	**LA22_P**	**LA.LA22_p**	**66**	**FMC_VADJ**	**IO_L10N_T1U_N7_QBC_AD4N_66**	**A4**
G25	**LA22_N**	**LA.LA22_n**			**IO_L10P_T1U_N6_QBC_AD4P_66**	**B4**
G26	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
G27	**LA25_P**	**LA.LA25_p**	**66**	**FMC_VADJ**	**IO_L17N_T2U_N9_AD10N_66**	**E8**
G28	**LA25_N**	**LA.LA25_n**			**IO_L17P_T2U_N8_AD10P_66**	**F8**
G29	GND	GND				
G30	**LA29_P**	**LA.LA29_p**	**66**	**FMC_VADJ**	**IO_L20N_T3L_N3_AD1N_66**	**B6**
G31	**LA29_N**	**LA.LA29_n**			**IO_L20P_T3L_N2_AD1P_66**	**C6**
G32	GND	GND				
G33	**LA31_P**	**LA.LA31_p**	**66**	**FMC_VADJ**	**IO_22N_T3U_N7_DBC_AD0N_66**	**B8**
G34	**LA31_N**	**LA.LA31_n**			**IO_22P_T3U_N6_DBC_AD0P_66**	**C8**
G35	GND	GND				
G36	**LA33_P**	**LA.LA33_p**	**66**	**FMC_VADJ**	**IO_L24N_T3U_N11_66**	**B9**
G37	**LA33_N**	**LA.LA33_n**			**IO_L24P_T3U_N10_66**	**C9**
G38	GND	GND				
G39	VADJ	FMC_VADJ				
G40	GND	GND				

Table 23 – J5H: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
H1	VREF_A_M2C	FVREF.VREF_A_M2C				T13
H2	PRSNT_M2C_L	FSIG.PRSNT_M2C_L			PD4 (µC)	29
H3	GND	GND				
H4	CLK0_M2C_P	FCK.CLK0_M2C_p			IN1_P (PLL)	14
H5	CLK0_M2C_N	FCK.CLK0_M2C_n			IN1_N (PLL)	15
H6	GND	GND				
H7	LA02_P	LA.LA02_p	46	FMC_VADJ	IO_L1P_AD11P_46	B15
H8	LA02_N	LA.LA02_n			IO_L1N_AD11N_46	A15
H9	GND	GND				
H10	LA04_P	LA.LA04_p	46	FMC_VADJ	IO_L3P_AD9P_46	B13
H11	LA04_N	LA.LA04_n			IO_L3N_AD9N_46	A13
H12	GND	GND				
H13	**LA07_P**	**LA.LA07_p**	**46**	**FMC_VADJ**	**IO_L10N_AD2N_46**	**H13**
H14	**LA07_N**	**LA.LA07_n**			**IO_L10P_AD2P_46**	**H14**
H15	GND	GND				
H16	LA11_P	LA.LA11_p	66	FMC_VADJ	IO_L2P_T0L_N2_66	E1
H17	LA11_N	LA.LA11_n			IO_L2N_T0L_N3_66	D1
H18	GND	GND				
H19	**LA15_P**	**LA.LA15_p**	**66**	**FMC_VADJ**	**IO_L6N_T0U_N11_AD6N_66**	**F5**
H20	**LA15_N**	**LA.LA15_n**			**IO_L6P_T0U_N10_AD6P_66**	**G5**
H21	GND	GND				
H22	**LA19_P**	**LA.LA19_p**	**66**	**FMC_VADJ**	**IO_L7N_T1L_N1_QBC_AD13N_66**	**B1**
H23	**LA19_N**	**LA.LA19_n**			**IO_L7P_T1L_N0_QBC_AD13P_66**	**C1**
H24	GND	GND				
H25	**LA21_P**	**LA.LA21_p**	**66**	**FMC_VADJ**	**IO_L9N_T1L_N5_AD12N_66**	**A3**
H26	**LA21_N**	**LA.LA21_n**			**IO_L9P_T1L_N4_AD12P_66**	**B3**
H27	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
H28	**LA24_P**	**LA.LA24_p**	**66**	**FMC_VADJ**	**IO_L16N_T2U_N7_QBC_AD3N_66**	**F7**
H29	**LA24_N**	**LA.LA24_n**			**IO_L16P_T2U_N6_QBC_AD3P_66**	**G8**
H30	GND	GND				
H31	**LA28_P**	**LA.LA28_p**	**66**	**FMC_VADJ**	**IO_L19N_T3L_N1_DBC_AD9N_66**	**A5**
H32	**LA28_N**	**LA.LA28_n**			**IO_L19P_T3L_N0_DBC_AD9P_66**	**B5**
H33	GND	GND				
H34	**LA30_P**	**LA.LA30_p**	**66**	**FMC_VADJ**	**IO_L21N_T3L_N5_AD8N_66**	**A6**
H35	**LA30_N**	**LA.LA30_n**			**IO_L21P_T3L_N4_AD8P_66**	**A7**
H36	GND	GND				
H37	**LA32_P**	**LA.LA32_p**	**66**	**FMC_VADJ**	**IO_L24N_T3U_N11_66**	**B9**
H38	**LA32_N**	**LA.LA32_n**			**IO_L24P_T3U_N10_66**	**C9**
H39	GND	GND				
H40	VADJ	FMC_VADJ				

Table 24 – J5J: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
J1	GND	GND				
J2	CLK3_BIDIR_P	FCK.CLK3_BIDIR_p			OUT6_P (PLL)	57
J3	CLK3_BIDIR_N	FCK.CLK3_BIDIR_n			OUT6_N (PLL)	58
J4	GND	GND				
J5	GND	GND				
J6	HA03_P	HA.HA03_p	44	VIO_B_M2C	IO_L2P_AD14P_44	AG14
J7	HA03_N	HA.HA03_n			IO_L2N_AD14N_44	AH14
J8	GND	GND				
J9	HA07_P	HA.HA07_p	44	VIO_B_M2C	IO_L9P_AD11P_44	W14
J10	HA07_N	HA.HA07_n			IO_L9N_AD11N_44	W13
J11	GND	GND				
J12	**HA11_P**	**HA.HA11_p**	**45**	**VIO_B_M2C**	**IO_L1N_AD15N_45**	**J10**
J13	**HA11_N**	**HA.HA11_n**			**IO_L1P_AD15P_45**	**J11**
J14	GND	GND				
J15	HA14_P	HA.HA14_p	45	VIO_B_M2C	IO_L4P_AD12P_45	J12
J16	HA14_N	HA.HA14_n			IO_L4N_AD12N_45	H12
J17	GND	GND				
J18	HA18_P	HA.HA18_p	45	VIO_B_M2C	IO_L7P_HDGC_45	E10
J19	HA18_N	HA.HA18_n			IO_L7N_HDGC_45	D10
J20	GND	GND				
J21	HA22_P	HA.HA22_p	45	VIO_B_M2C	IO_L11P_AD9P_45	A12
J22	HA22_N	HA.HA22_n			IO_L11N_AD9N_45	A11
J23	GND	GND				
J24	HB01_P	nc				
J25	HB01_N	nc				
J26	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
J27	HB07_P	nc				
J28	HB07_N	nc				
J29	GND	GND				
J30	HB11_P	nc				
J31	HB11_N	nc				
J32	GND	GND				
J33	HB15_P	nc				
J34	HB15_N	nc				
J35	GND	GND				
J36	HB18_P	nc				
J37	HB18_N	nc				
J38	GND	GND				
J39	VIO_B_M2C	VIO_B_M2C				
J40	GND	GND				

Table 25 – J5K: FMC Connector

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
K1	VREF_B_M2C	FVREF.VREF_B_M2C				R12
K2	GND	GND				
K3	GND	GND				
K4	CLK2_BIDIR_P	FCL.CLK2_BIDIR_p			OUT5_P (PLL)	54
K5	CLK2_BIDIR_N	FCL.CLK2_BIDIR_n			OUT5_N (PLL)	53
K6	GND	GND				
K7	HA02_P	HA.HA02_p	44	VIO_B_M2C	IO_L1P_AD15P_44	AE15
K8	HA02_N	HA.HA02_n			IO_L1N_AD15N_44	AE14
K9	GND	GND				
K10	HA06_P	HA.HA06_p	44	VIO_B_M2C	IO_L8P_HDGC_44	AB15
K11	HA06_N	HA.HA06_n			IO_L8N_HDGC_44	AB14
K12	GND	GND				
K13	**HA10_P**	**HA.HA10_p**	**44**	**VIO_B_M2C**	**IO_L12N_AD8N_44**	**AA12**
K14	**HA10_N**	**HA.HA10_n**			**IO_L12P_AD8P_44**	**Y12**
K15	GND	GND				
K16	HA17_P_CC	HA.HA17_CC_p	44	VIO_B_M2C	IO_L7P_HDGC_44	AA13
K17	HA17_N_CC	HA.HA17_CC_n			IO_L7N_HDGC_44	AB13
K18	GND	GND				
K19	HA21_P	HA.HA21_p	45	VIO_B_M2C	IO_L10P_AD10P_45	B11
K20	HA21_N	HA.HA21_n			IO_L10N_AD10N_45	A10
K21	GND	GND				
K22	HA23_P	HA.HA23_p	45	VIO_B_M2C	IO_L12P_AD8P_45	D12
K23	HA23_N	HA.HA23_n			IO_L12N_AD8N_45	C12
K24	GND	GND				
K25	HB00_P_CC	nc				
K26	HB00_N_CC	nc				
K27	GND	GND				

FMC Pin#	FMC Label	Signal Name	FPGA Bank	FPGA VCCO	Pin Name	Pin#
K28	HB06_P_CC	nc				
K29	HB06_N_CC	nc				
K30	GND	GND				
K31	HB10_P	nc				
K32	HB10_N	nc				
K33	GND	GND				
K34	HB14_P	nc				
K35	HB14_N	nc				
K36	GND	GND				
K37	HB17_P_CC	nc				
K38	HB17_N_CC	nc				
K39	GND	GND				
K40	VIO_B_M2C	VIO_B_M2C				

5.3.5. S2: USB-/ UART Connector

The **NAT-AMC-ZYNQUP-ECO** features an USB-/ UART interface via a Micro-USB connector at the front panel. It is necessary to use a cable with a long micro-USB connector (7mm+).

Figure 13 – S3: USB-/ UART Connector

Table 26 – S3: USB-/ UART Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	V_USB	USB_N	2
3	USB_P	GND	4
5	GND		

5.3.6. S3: MicroSD-Card Slot

The **NAT-AMC-ZYNQUP-ECO** includes a secure digital input/output (SDIO) interface to provide user-logic access to general-purpose nonvolatile MicroSD-Cards. To boot from a MicroSD-Card, insert a card with a bootable image and set the boot mode switches (see chapter 5.3.11 SW5 / SW6: Boot Mode Select Switches for details) to MicroSD-Card position.

Figure 14 – S2: MicroSD-Card Slot

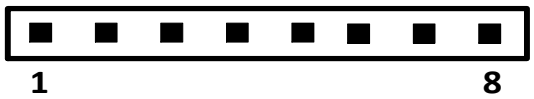


Table 27 – S2: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SDIO_1_D2	SDIO_1_D3	2
3	SDIO_1_CMD	3V3	4
5	SDIO_1_CLK	GND	6
7	SDIO_1_D0	SDIO_1_D1	8

5.3.7. SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

5.3.8. SW2: Dip Switch

DIP SW2 is tbd.

Figure 15 – SW2: FMC Configuration Switch

Table 28 – SW2 – Operating Parameters

Switch #	Function
SW2-1	tbd
SW2-2	tbd

Table 29 – SW2 – Configuration

Switch #	ON	OFF
SW2-1	tbd	***tbd***
SW2-2	Tbd	***tbd***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3.9. SW3: JTAG MUX Switch

The tables below provide information on the operating parameters and configuration options of SW3.

Figure 16 – SW3: JTAG MUX Switch

Table 30 – SW3 – Operating Parameters

Switch #	Function
SW3-1	JTAG Select – FPGA or JTAG-SMT3 module as Master
SW3-2	JTAG Disable

Table 31 – SW3 – Configuration

Switch #	ON	OFF
SW3-1	Use Backplane as FPGA JTAG Master	***Use JTAG-SMT2 as FPGA JTAG Master***
SW3-2	JTAG Circuits are disabled	***JTAG Circuits are enabled***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3.10. SW4: UART MUX

The tables below provide information on the operating parameters and configuration options of SW4.

Figure 17 – SW4: UART MUX

Table 32 – SW4 – Operating Parameters

Switch #	Function
SW4-1	UART Select
SW4-2	UART Disable

Table 33 – SW4 – Configuration

Switch #	ON	OFF
SW4-1	Use MMC UART	***Use FPGA UART***
SW4-2	UART disabled	***UART enabled***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3.11. SW5 / SW6: Boot Mode Select Switches

The **NAT-AMC-ZYNQUP-ECO** supports several boot options:

- Boot from SD card
- Boot from on-board QSPI FLASH
- Boot from JTAG

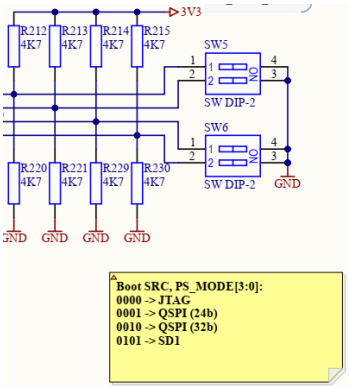
Figure 18 – SW5 / SW6: Boot Mode Select Switch

Table 34 – SW5 / SW6: Boot Mode Select Switch

Boot Mode	SW5-1	SW5-2	SW6-1	SW6-2
JTAG	ON	ON	ON	ON
QSPI(24b)	***OFF***	***ON***	***ON***	***ON***
QSPI(32b)	ON	OFF	ON	ON
SD Card	OFF	ON	OFF	ON

Note:

Default configuration is labelled with ***bold, italic letters***.



6. FMC OPERATION

6.1. Front panel

Depending on the used FMC, the front panel metalwork may not fit and needs to be reworked. This is needed in case FMCs with 8.5 mm stacking height are used that do not fit into the standard front panel cut out which is made for 100 mm stacking height FMCs. Please contact N.A.T. in case specialized front panel needs to be made.

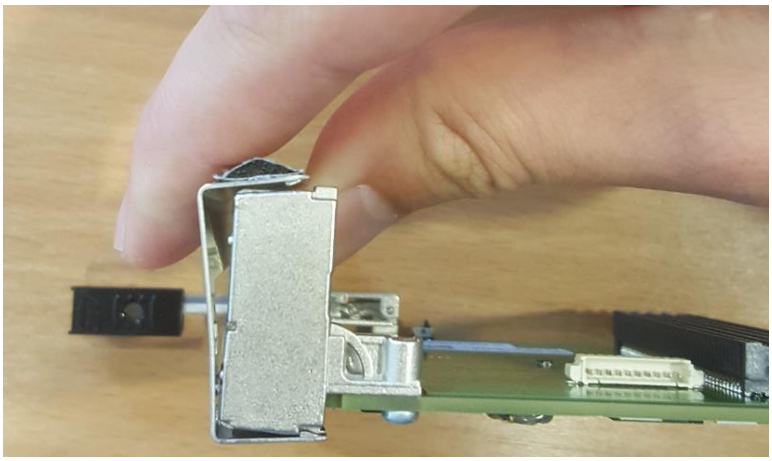
6.2. Supported FMC's

All FMCs compliant to VITA 57.1 are supported, including region 1, 2, and 3 FMC modules. VADJ and VIO_B_M2C are limited to 1.8V. Please check I/O 5.3.1 table for constraints to make sure your FMC is supported.

6.3. Installing a FMC Module

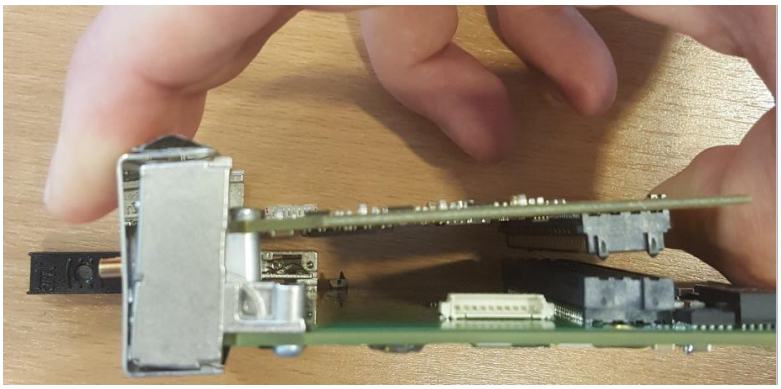
When applying a FMC module it could be necessary to remove or to untighten the front metal in order for the FMC front to fit into the cut-out.

Figure 19 – Installing FMC Module Part 1



After fitting the FMC module to the carrier, the front panel needs to be restored.

Figure 20 – Installing FMC Module Part 2



6.4. FMC EEPROM Wizard

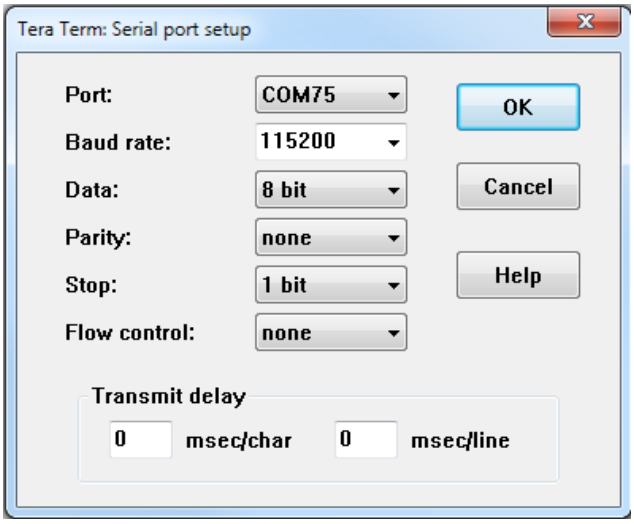
Per default, the carrier will try to parse the FMC FRU records from the modules EEPROM contents to set the carrier's power supply and clock direction. In case there is an FMC without records, there are two options:

1) Generate and program the records with the carrier. Set SW2-3 2 to "ON".

2) Ignore the FRU EEPROM. This is automatically done when no valid FRU content is detected. ***Warning:*** In this case, a default VADJ voltage of 1.8V is applied to the FMC module. Please check the capabilities of your FMC in this case.

In case the records for the FMC should be generated with the carrier, the Micro USB cable has to be connected to the front plate's USB port. The host should detect a USB-Hub and two COM ports. The first enumerated COM port is the serial console of the MMC. Open it with a tool (e.g. TeraTerm) and set the COM settings according to the following figure.

Figure 21 – Serial Console COM Port Settings



The MMC has to be rebooted with triggering the HS-Handle. The console output should output the following line:

```
Press any key to generate FMC FRU file ... 5.0
```

Within five seconds time press any key to enter the FMC programming mode. This mode is guided and will lead through the steps to program the FMC records. At the end of the wizard, it will ask to program the EEPROM file of the FMC.

7. SPECIFICATIONS AND COMPLIANCES

7.1. Internal Reference Documentation

- **NAT-AMC-ZYNQUP-ECO**
- **NAT-FMC-PoE**
- **NAT-AMC-ZYNQUP-ADV**
- https://nateurope.com/solution/natvision/

7.2. External Reference Documentation

- Atmel ATxmega128 µC Product Datasheet, Rev A, 08/2018
- Micron MT40A512M16LY-062 DDR4 SDRAM Datasheet, Rev. P, 04/2019
- Texas Instruments DS91M040 MLVDS Transceiver Datasheet, Rev. M, 04/2013
- Texas Instruments SN74AVC2T245 Bus Transceiver Datasheet, Rev. E, 09/2024
- Xilinx Zynq UltraScale+ MPSoC DS891, V1.10, 11/2022
- Xilinx Programming Module: https://reference.digilentinc.com/reference/programmers/jtag-smt3/reference-manual

7.3. Standards Compliance

- AMC.0 R2.0
- AMC.1
- AMC.2
- AMC.3
- AMC.4
- IMPI V1.5
- HPM.1

7.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.7. Product Safety

The board complies with EN60950 and UL1950.

7.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7.9. Abbreviation List

Table 35 – Abbreviation List

Abbreviation	Description
ADC	Analog-Digital-Converter
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
CPU	Central Processing Unit
DAC	Digital-Analog-Converter
DDR4 SDRAM	Double Data Rate Synchronous DRAM
(D)RAM	(Dynamic) Random Access Memory
eMMC	Embedded Multimedia Card
FCLK	Fabric Clock
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FRU	Field-Replaceable Unit
GbE	Gigabit Ethernet
GPU	Graphics Processing Unit
HPC	High Pin-Count
HPM	Hardware Platform Management
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
MicroSD-Card	Micro Secure Digital Memory Card
MIMO	Multiple-Input and Multiple-Output
MUX	Multiplexer
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
QDR4 RAM	Quad Data Rate RAM
(Q)SPI (FLASH)	(Quad) Serial Peripheral Interface (FLASH)
RF	Radio Frequency
RL DRAM	Reduced Latency DRAM
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SDR	Software Defined Radio
SoC	System on a Chip
SRIO	Serial Rapid I/O
TCKL	Telecom Clock
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

8. DOCUMENT'S HISTORY

Table 36 – Document's History

Rev	Date	Description	Author
1.0	19.04.2024	• initial release	se
1.1	1.08.2024	• Updated Figure 3 – IPMB-Interface	Se
	17.09.2024	• Updated chapter 4.2 PLL and Clocking • Updated chapter 4.1.1.1 Memory	se
	13.11.2024	• Updated chapter 4.5 SerDes Connectivity • Added chapter 4.6 SerDes Connectivity – Alternative Assembly • Added chapter 4.7 Port 17-20 MLVDS Bus Lines (Trigger Signals) • Added chapter Table 11 – AMC Port Definition – Alternative Assembly	Se
1.2	20.11.2024	• Minor changes • Added Order Codes	Se
	13.03.2025	• Updated FMC-FPGA Assignment • Updated Figure 4 – JTAG Architecture	Se
1.3	24.03.2025	• Updated Table 1 – Technical Data • Updated Figure 2 – PLL and Clocking • Corrected Labelling of FMC Assignment Tables	se