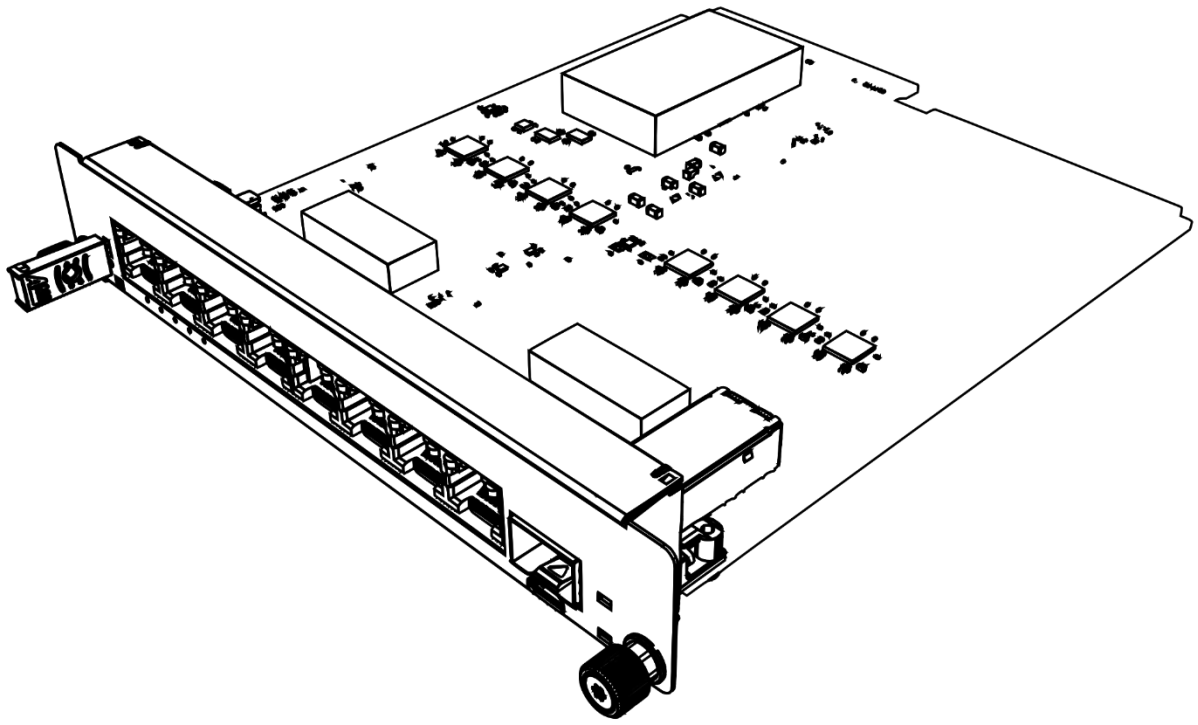
NAT-AMC-ZYNQUP-ECAT

ETHERCAT SLAVE NODE AMC

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.1

HW REVISION 1.X

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. PREFACE

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1.2. About This Document

This document is intended to give an overview on the **NAT-AMC-ZYNQUP-ECAT's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-AMC-ZYNQUP-ECAT's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-AMC-ZYNQUP-ECAT** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-AMC-ZYNQUP-ECAT's** main features

Hardware

Information about LEDs, connectors, and port definitions

FPGA Pin-Out

Detailed tables showing mapping of the FPGA pins to the rest of the module's components

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-AMC-ZYNQUP-ECAT** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-AMC-ZYNQUP-ECAT** is handled by qualified personnel only!

2. INTRODUCTION

With the **NAT-AMC-ZYNQUP-ECAT**, any embedded system based on the MTCA standard can be integrated as a slave node in an existing high performance, real time field bus system based on EtherCAT.

The core of the double-wide, mid-sized AMC is a XILINX Zynq Ultrascale+ MPSoC with 4 GB DDR4 RAM and QSPI FLASH. The SoC is linked to the backplane by two GbE interfaces on Ports 0/1, two PCIe-connections on AMC Ports 4/8, and (M)LVDS connections on Ports 12-15 as well as on Ports 17-20.

Moreover, the **NAT-AMC-ZYNQUP-ECAT** features an SFP-Connector at the front plate as general purpose I/O, a Micro-USB jack as serial- and JTAG-Interface, and 4 pairs of RJ45 connectors (100 Mbit) as interfaces to the EtherCAT network.

2.1. Basic Functionality – What is EtherCAT?

The goal of EtherCAT (***Ether***net for ***C***ontrol ***A***utomation ***T***echnology) is to have a low price, high speed real-time field bus system with very short cycle times and exact synchronization, which is important in industrial automation applications. EtherCAT can be used in a broad range of applications and is completely compliant to the current Ethernet standard, but does not have the latency and overhead issues of Ethernet.

An EtherCAT network has an EtherCAT Master, which controls the network of EtherCAT slave devices. Up to 65535 EtherCAT slaves can be integrated with a distance of up to 100m to each other, totaling n x 100m for the whole network. The topology of the field bus network can be line, star, and branch.

2.1.1. EtherCAT Master

To use a MTCA system as the EtherCAT master, only a standard CPU AMC module running the Master EtherCAT software and standard Ethernet are needed.

2.1.2. EtherCAT Slave

To use a MTCA system as an EtherCAT slave, a special AMC module is needed, which adds and drops information on the fly in real time into the EtherCAT bit stream.

Due to its 4 pairs of RJ45 connectors, the **NAT-AMC-ZYNQUP-ECAT** can be embedded into four different EtherCAT networks as Slave Node; the assignment is user-defined and handled by the MPSoC.

2.2. Applications

MTCA systems as slave devices of an EtherCAT network can be used for image and sensor preprocessing, or for complex control applications such as robotics. In addition, EtherCAT also allows the transfer of standard Ethernet packets. Therefore, all the new features of remote control and management functions of MTCA systems can be used over the same cable.

2.3. Main Features

Table 1 – Technical Data

NAT-AMC-ZYNQUP-ECAT	
Form Factor	• Double-wide, mid-size AMC (option: full-size) • Width: 149 mm, Height: 19 mm (29 mm), Depth: 182 mm
SoC	• XILINX Zynq Ultrascale+ MPSoC
MMC	• Atmel ATxmega128
Memory	• DDR4 RAM: 4GB, 64 bit-wide • QSPI FLASH: 1Gbit NOR-FLASH • MicroSD-Card
Ethernet PHY	• 8x Microchip KSZ8061MNG
PLL	• SI5338 Differential Clock Generator
Backplane Interfaces	• AMC Ports 0/1: GbE • AMC Ports 4/8: PCIe • AMC Ports 12-15: LVDS P2P • AMC Ports 17-20: MLVDS Bus • TCLKA-D • IPMI
Front Panel Interfaces	• 8x 100Mbit Ethernet via RJ45 • SFP as GPIO of FPGA (LVDS or single-ended I/O) • JTAG to USB and UART
Indicator LEDs	• 3 standard AMC LEDs • 5 status LEDs (red/green)
Standards Compliance	• AMC.0 R2.0, AMC.1, AMC.2, IMPI V1.5, HPM.1
Operating Environment	• Default: 0°C to +55°C (with forced cooling) • Humidity: 10% to 90% at +55°C (non-condensing)
Storage Environment	• Default: -40°C to +85°C • Humidity: 10% to 90% (non-condensing)

3. QUICK START

To ensure proper functioning of the **NAT-AMC-ZYNQUP-ECAT** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the AMC-Edge-Connector to ensure proper contact when inserting the **NAT-AMC-ZYNQUP-ECAT** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAT-AMC-ZYNQUP-ECAT** is designed to meet the requirements of µTCA systems, but can be plugged onto any ATCA carrier board supporting AMC standards as well. So the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAT-AMC-ZYNQUP-ECAT**, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-AMC-ZYNQUP-ECAT**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-swap-capable, if you do not switch off the power.

Ensure that the **NAT-AMC-ZYNQUP-ECAT** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-AMC-ZYNQUP-ECAT** must meet the following specifications:

+12V / 2A max.

+ 3,3V / 0.15A max.

3.3.2. Hot-Swap

The **NAT-AMC-ZYNQUP-ECAT** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-AMC-ZYNQUP-ECAT** or the system it is plugged into from damage!

Insertion of a hot-swap-capable Module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-AMC-ZYNQUP-ECAT** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAT-AMC-ZYNQUP-ECAT** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable Module

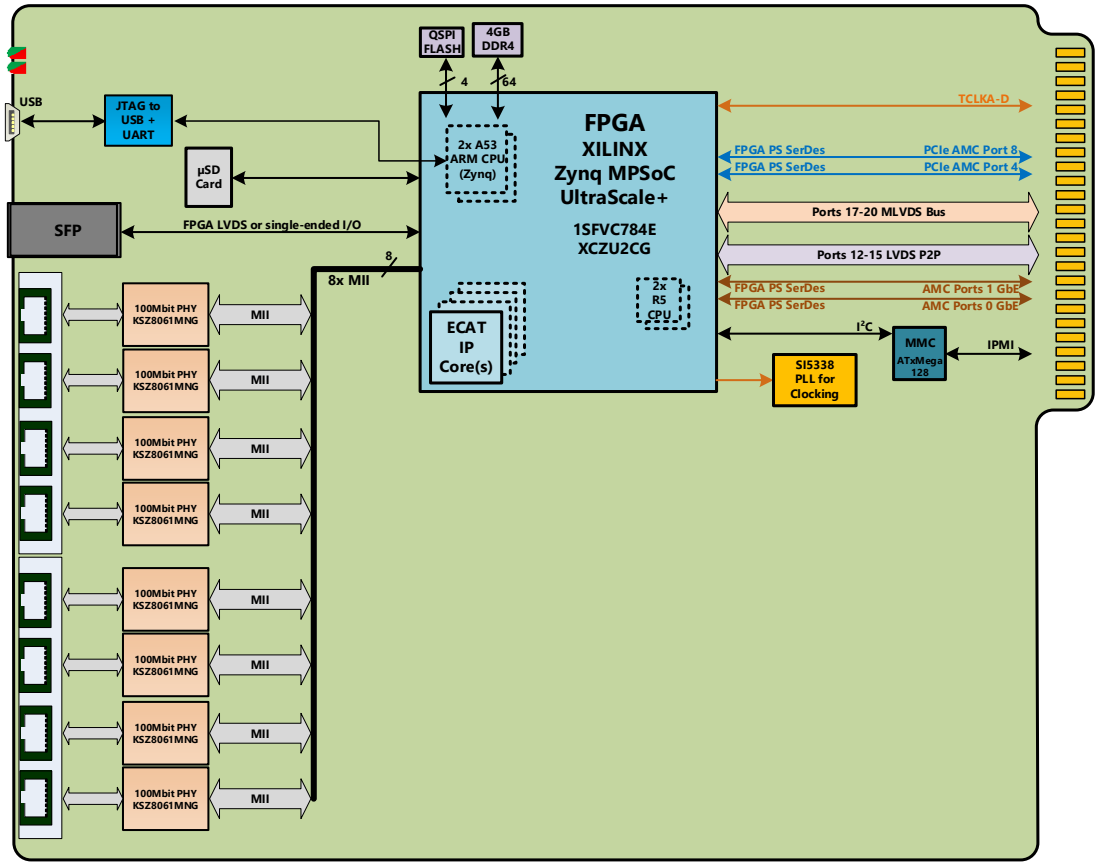
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAT-AMC-ZYNQUP-ECAT** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

The **NAT-AMC-ZYNQUP-ECAT** can be divided into several functional blocks, which are described in the following paragraphs.

The following figures give an overview on the functional blocks.

Figure 1 – Block Diagram NAT-AMC-ZYNQUP-ECAT



4.1. SoC

The **NAT-AMC-ZYNQUP-ECAT** is equipped with a XILINX Zynq Ultrascale+ MPSoC, which features a processing unit combined with programmable logic.

4.1.1. Processing Unit

The processing unit of the XILINX Ultrascale+ MPSoC made up of a dual-core ARM Cortex-A53 as application processing unit, and a dual-core ARM Cortex-R5 as real time processing unit.

4.1.1.1. Memory

Four 64bit-wide DDR4 Chips (Nanya NT5AD512M16A4-HRI) are connected to the Processing System of the MPSoC.

Moreover, a Micro-SD-Card and a QSPI FLASH are connected to the A53 application processing unit.

4.2. Programmable Logic

The ECAT FPGA cores are implemented in the programmable logic.

4.3. Front Panel Interfaces

4.3.1. Ethernet PHYs

Due to 4 pairs of RJ45 connectors (100 Mbit), the **NAT-AMC-ZYNQUP-ECAT** can be embedded into four different EtherCAT networks as slave node; the assignment is user-defined and handled by the MPSoC.

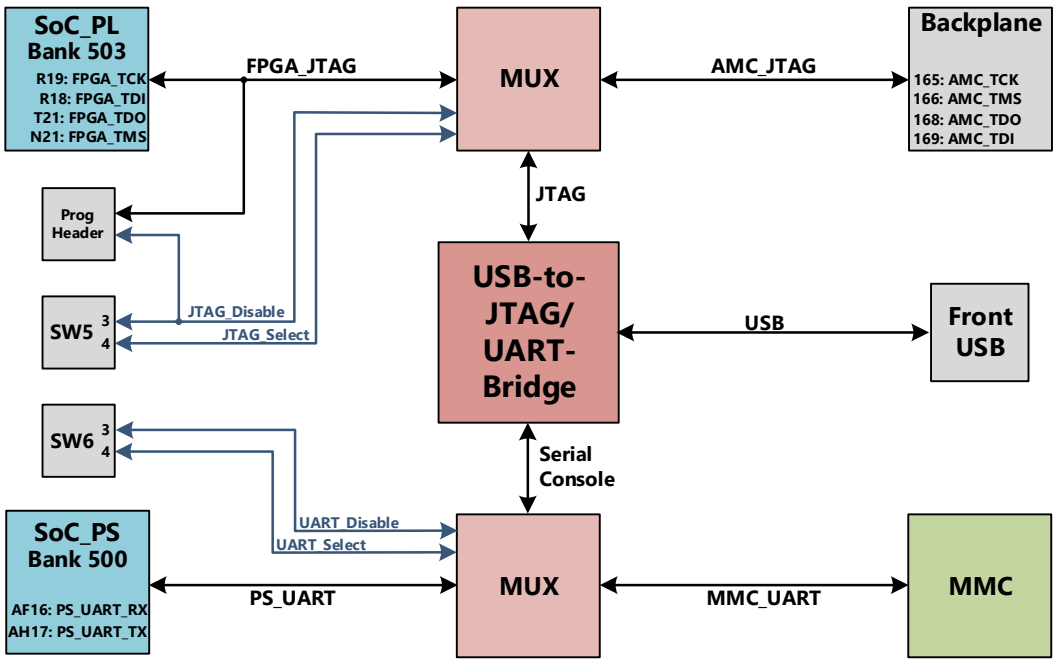
4.3.2. GPIO

The **NAT-AMC-ZYNQUP-ECAT** features an SFP-Connector at the front plate as general purpose I/O.

4.3.3. JTAG-/UART-Interface

Moreover, the **NAT-AMC-ECAT-ZYNQUP** features a Micro-USB jack as serial- and JTAG-Interface. A USB-to-JTAG/UART-Bridge splits the signal; the connectivity is illustrated in the following figure.

Figure 2 – JTAG-/UART-Connectivity



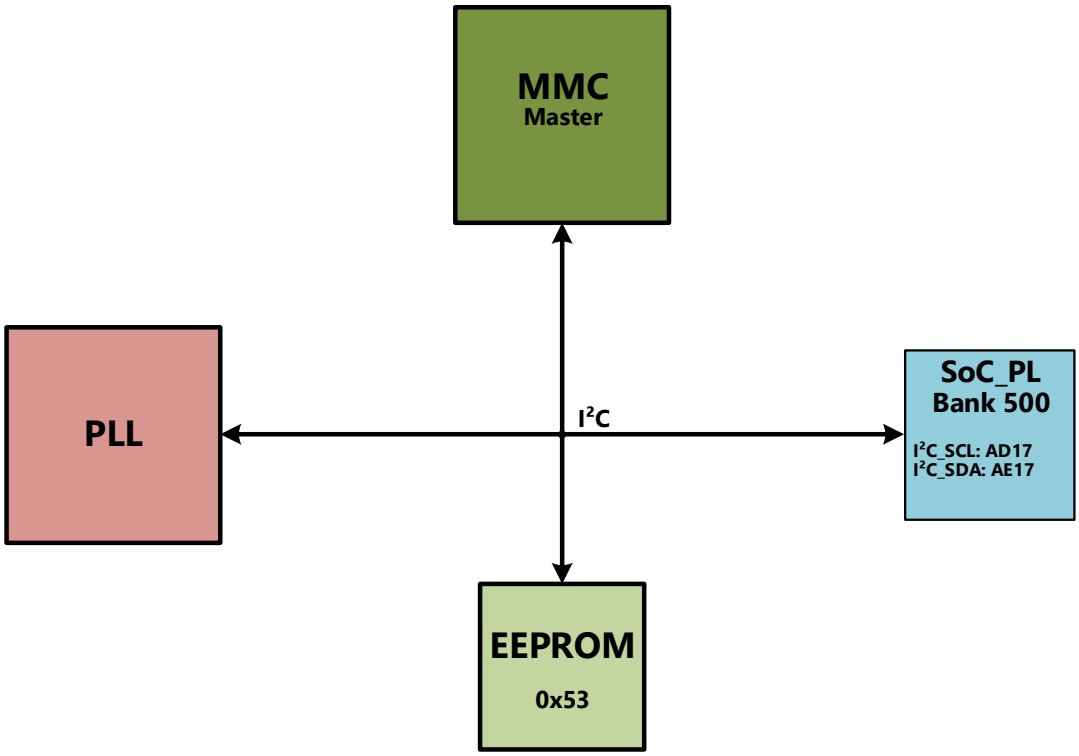
4.4. Backplane Interconnect

The MPSoC is linked to the backplane by two GbE interfaces on Ports 0/1, two PCIe-connections on AMC Ports 4/8, and (M)LVDS connections on Ports 12-15 as well as on Ports 17-20.

4.5. Microcontroller

An Atmel ATxmega128 microcontroller works as IPMI controller. I²C-Connectivity of the **NAT-AMC-ECAT-ZYNQUP** is illustrated below:

Figure 3 – I²C-Connectivity



5. HARDWARE

5.1. Front Panel and LEDs

The **NAT-AMC-ZYNQUP-ECAT** is equipped with various LEDs described in the following sections.

Figure 4 – Front Panel (Mid-Size)

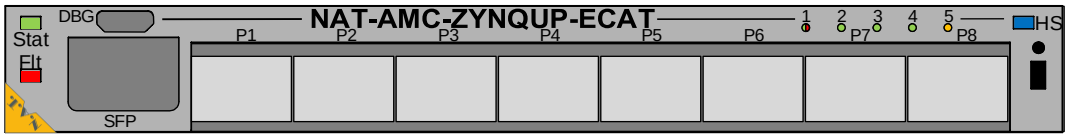


Table 2 – LED Functionality

LED	Color	Function	Description
AMC GP LED	Green	tbd	tbd
	Yellow	tbd	tbd
AMC Fault LED	Red	ON	Temperature exceeding / underrunning threshold level
		OFF	Temperature OK
AMC HS LED	Blue	ON	please refer to chapter 3.3.2 Hot-Swap
		blink	
		OFF	
LED 1	Red	custom	controlled by FPGA; please refer to **Table 25 – LED to FPGA Pin-Out** for details
	Green		
LED 2	Green		
LED 3	Green		
LED 4	Green		
LED 5	Yellow		
LED 6 (on PCB)	Green		

Note: Although appearing as one LED optically, the AMC GP LED consists of two LEDs (green and yellow) physically, sharing the same hole in the front plate.

5.2. AMC Port Definition

Table 3 – AMC Port Definition

Connector Region		AMC Port #	Signal	Non-Redundant MCH / Fabric #	Redundant MCH / Fabric #
Basic Side	Clocks	TCLKA	Reference TCLKA	CLK1	
		TCLKB	Reference TCLKB	CLK2	
		FCLKA	Fabric Clock	CLK3	
	Common Options	0	GbE Channel 0	A	1 / A
		1	GbE Channel 1		2 / A
		2	unassigned	(B)	(1 / B)
		3	unassigned	(C)	(2 / B)
	Fat Pipe	4	PCIe	D	1 / D
		5	unassigned	E	1 / E
		6	unassigned	F	1 / F
		7	unassigned	G	1 / G
Extended Side	Extended Fat Pipe	8	PCIe		2 / D
		9	unassigned		2 / E
		10	unassigned		2 / F
		11	unassigned		2 / G
	Extended Options	12	LVDS P2P		
		13			
		14			
		15			
		16	Reference TCLKC/D		CLK1 / CLK2
		17	MLVDS-Bus		
		18			
		19			
		20			

Note: The mapping of the MCH's fabrics can vary depending on which backplane the **NAT-AMC-ZYNQUP-ECAT** is operated. This table shows the standard assignment.

5.3. Component-, Connector-, and Switch-Location

Figure 5 – Location Diagram – Top

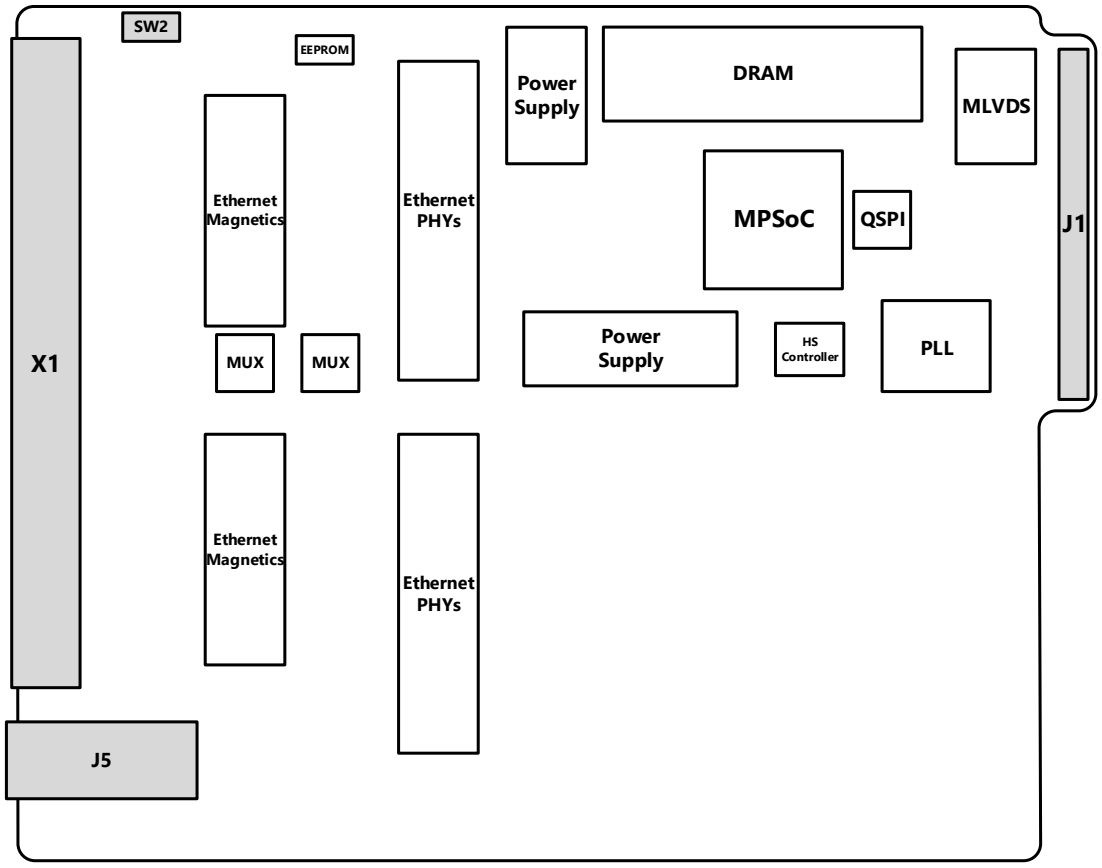
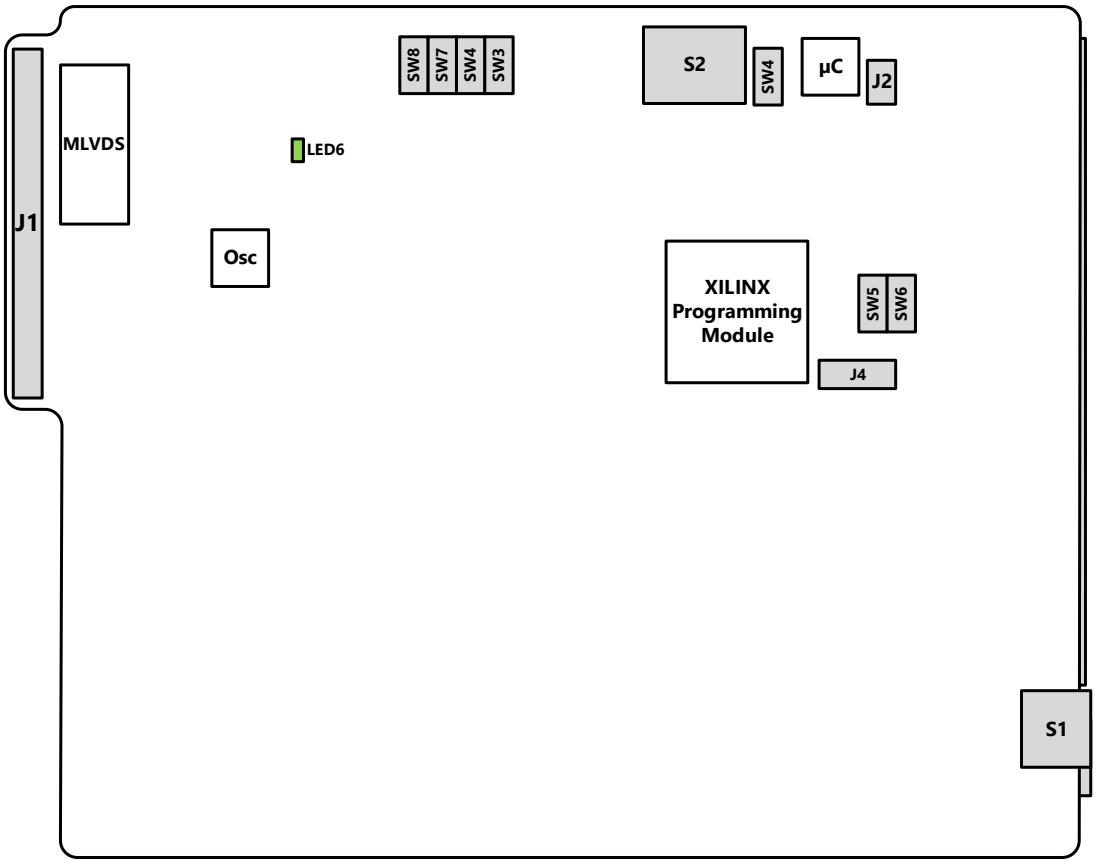


Figure 6 – Location Diagram – Bottom



Please refer to the following tables to look up the connector pin assignment of the **NAT-AMC-ZYNQUP-ECAT**.

5.3.1. J1: AMC Edge Connector

The **NAT-AMC-ZYNQUP-ECAT** connects to the backplane via J1.

Figure 7 – J1: AMC Edge Connector

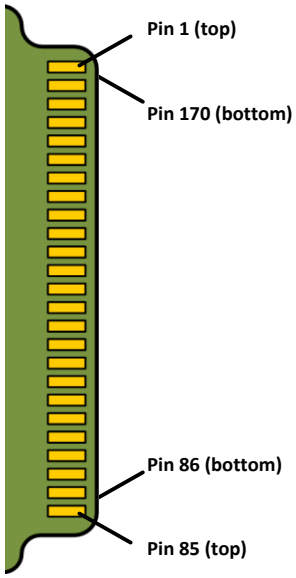


Table 4 – J1: AMC Edge Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	PWR_IN	AMC_TDI	169
3	/AMC_PS1	AMC_TDO	168
4	+3.3V_MP	nc	167
5	AMC.GA0	AMC_TMS	166
6	nc	AMC_TCK	165
7	GND	GND	164
8	nc	PORT20-Tx_P	163
9	PWR_IN	PORT20-Tx_N	162
10	GND	GND	161
11	PORT0-Tx_P	PORT20-Rx_P	160
12	PORT0-Tx_N	PORT20-Rx_N	159
13	GND	GND	158
14	PORT0-Rx_P	PORT19-Tx_P	157
15	PORT0-Rx_N	PORT19-Tx_N	156
16	GND	GND	155
17	AMC.GA1	PORT19-Rx_P	154
18	PWR_IN	PORT19-Rx_N	153
19	GND	GND	152
20	PORT1-Tx_P	PORT18-Tx_P	151
21	PORT1-Tx_N	PORT18-Tx_N	150

Pin #	Signal	Signal	Pin #
22	GND	GND	149
23	PORT1-Rx_P	PORT18-Rx_P	148
24	PORT1-Rx_N	PORT18-Rx_N	147
25	GND	GND	146
26	AMC.GA2	PORT17-Tx_P	145
27	PWR_IN	PORT17-Tx_N	144
28	GND	GND	143
29	nc	PORT17-Rx_P	142
30	nc	PORT17-Rx_N	141
31	GND	GND	140
32	nc	AMC_TCLKD_P	139
33	nc	AMC_TCKLD_N	138
34	GND	GND	137
35	nc	AMC_TCLKC_P	136
36	nc	AMC_TCKLC_N	135
37	GND	GND	134
38	nc	PORT15-Tx_P	133
39	nc	PORT15-Tx_N	132
40	GND	GND	131
41	AMC_ENABLEn	PORT15-Rx_P	130
42	PWR_IN	PORT15-Rx_N	129
43	GND	GND	128
44	PORT4-Tx_P	PORT14-Tx_P	127
45	PORT4-Tx_N	PORT14-Tx_N	126
46	GND	GND	125
47	PORT4-Rx_P	PORT14-Rx_P	124
48	PORT4-Rx_N	PORT14-Rx_N	123
49	GND	GND	122
50	nc	PORT13-Tx_P	121
51	nc	PORT13-Tx_N	120
52	GND	GND	119
53	nc	PORT13-Rx_P	118
54	nc	PORT13-Rx_N	117
55	GND	GND	116
56	I2C_SCL_MP	PORT12-Tx_P	115
57	PWR_IN	PORT12-Tx_N	114
58	GND	GND	113
59	nc	PORT12-Rx_P	112
60	nc	PORT12-Rx_N	111
61	GND	GND	110
62	nc	nc	109
63	nc	nc	108
64	GND	GND	107
65	nc	nc	106
66	nc	nc	105
67	GND	GND	104
68	nc	nc	103
69	nc	nc	102

Pin #	Signal	Signal	Pin #
70	GND	GND	101
71	I2C_SDA_MP	nc	100
72	PWR_IN	nc	99
73	GND	GND	98
74	AMC_TCLKA_P	nc	97
75	AMC_TCKLA_N	nc	96
76	GND	GND	95
77	AMC_TCLKB_P	nc	94
78	AMC_TCKLB_N	nc	93
79	GND	GND	92
80	AMC_FCLKA_P	PORT8_Tx_P	91
81	AMC_FCKLA_N	PORT8_Tx_N	90
82	GND	GND	89
83	/AMC_PS0	PORT8_Rx_P	88
84	PWR_IN	PORT8-Rx_N	87
85	GND	GND	86

5.3.2. J2: Microcontroller Programming Header

J2 is a programming header for the Atmel ATxmega µC.

Figure 8 – J2: PDI Connector

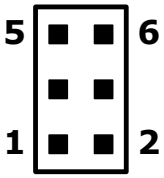


Table 5 – J2: Microcontroller Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI-DATA	+3.3V_MP	2
3	nc	nc	4
5	PDI_CLK	GND	6

5.3.3. J4: FPGA Programming Header

J4 offers a JTAG interface for a FPGA programming connection.

Figure 9 – J4: FPGA Programming Header

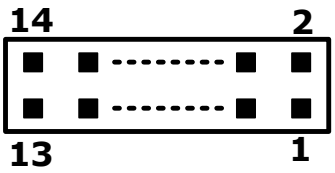


Table 6 – J4: FPGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	V_PROG	JTAG_SEL	2
3	FPGA_TMS	GND	4
5	FPGA_TCK	GND	6
7	FPGA_TDO	GND	8
9	FPGA_TDI	GND	10
11	nc	GND	12
13	PS_ARM_SRTS	GND	14

5.3.4. S1: USB Connector

S1 offers a USB/UART interface to the **NAT-AMC-ZYNQUP-ECAT**.

Figure 10 – S1: USB Connector

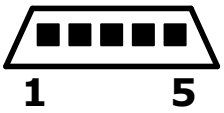


Table 7 – S1: USB Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC	U_N	2
3	U_P	nc	4
5	GND		

5.3.5. S2: MicroSD-Card Slot

S2 is a MicroSD-Card slot on the **NAT-AMC-ZYNQUP-ECAT**.

Figure 11 – S2: MicroSD-Card Slot

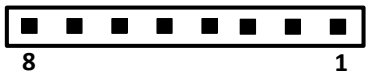


Table 8 – S2: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SDIO_1_D2	SDIO1_D3	2
3	SDIO_1_CMD	3V3	4
5	SDIO_1_CLK	GND	6
7	SDIO_1_D0	SDIO_1_D1	8

5.3.6. SW1: tbd

DIP SW1 is populated for future use

Figure 12 – SW1: tbd

Table 9 – SW1 – Operating Parameters

Switch #	Function
SW1-1	***tbd***
SW1-2	***tbd***

Note: Default configuration is labelled with ***bold, italic letters***.

5.3.7. SW2: Hot Swap Switch

Switch SW2 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

5.3.8. SW3 / SW4: Boot Mode Select Switches

SW3 and SW4 are boot mode select switches.

Figure 13 – SW3/SW4: Boot Mode Select Switches

Table 10 – SW3 – Operating Parameters

Switch #	Function
SW3-1	***OFF: Signal 'PS_MODE[2]' high*** ON: Signal 'PS_MODE[2]' low
SW3-2	***OFF: Signal 'PS_MODE[3]' high*** ON: Signal 'PS_MODE[3]' low

Table 11 – SW4 – Operating Parameters

Switch #	Function
SW4-1	***OFF: Signal 'PS_MODE[0]' high*** ON: Signal 'PS_MODE[0]' low
SW4-2	***OFF: Signal 'PS_MODE[1]' high*** ON: Signal 'PS_MODE[1]' low

Note: Default configuration is labelled with ***bold, italic letters***.

More information on SW3/SW4 can be found in **Table 26 – DIP-Switch to FPGA Pin-Out**.

5.3.9. SW5 / SW6: JTAG MUX Switches

SW5 and SW6 are JTAG MUX switches.

Figure 14 – SW5/SW6: JTAG MUX Switches

Table 12 – SW5 – Operating Parameters

Switch #	Function
SW5-1	***OFF: Use SMT2 as FPGA JTAG Master*** ON: Use Backplane as FPGA JTAG Master
SW5-2	***OFF: JTAG circuits are enabled*** ON: JTAG circuits are disabled

Table 13 – SW6 – Operating Parameters

Switch #	Function
SW6-1	***OFF: Use FPGA UART*** ON: Use MMC UART
SW6-2	***OFF: UART enabled*** ON: UART disabled

Note: Default configuration is labelled with ***bold, italic letters***.

5.3.10. SW7 / SW8: Custom Switches

SW7 and SW8 are connected to the FPGA directly and can be customized by the user.

Figure 15 – SW7/SW8: Custom Switches

Table 14 – SW7 – Operating Parameters

Switch #	Function
SW7-1	***custom***
SW7-2	***custom***

Table 15 – SW8 – Operating Parameters

Switch #	Function
SW8-1	***custom***
SW8-2	***custom***

Note: Default configuration is labelled with ***bold, italic letters***.

More information on SW7/SW8 can be found in **Table 26 – DIP-Switch to FPGA Pin-Out**.

5.3.11. X1 – Ethernet Connector

Connector X1 with its ports P1-P8 features eight RJ45 interfaces for connecting the **NAT-AMC-ZYNQUP-ECAT** to an EtherCAT network.

Each RJ45 connector owns two green LEDs, which are configurable via the Ethernet PHY.

Figure 16 – X1: Ethernet Connector

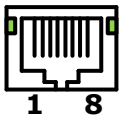


Table 16 – X1: Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	TDx_P	TDx_N	2
3	RDx_P	not used	4
5	not used	RDx_N	6
7	not used	not used	8

Note: 'x' refers to the according signal [0..7]

6. FPGA PIN-OUT

Table 17 – PHYs to FPGA Pin-Out

PHY Pin#	PHY Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
PHY 0						
16	MDIO	MDIO	26	VCCO_26	IO_L5P_HDGC_AD7P_26	D15
17	MCLK	MCLK			IO_L5N_HDGC_AD7N_26	D14
18	RXERR	RX_ERR			IO_L3P_AD9P_26	B13
19	RXDV	RX_DV			IO_L10N_AD2N_26	H13
20	RXD3	RX_DATA3			IO_L2N_AD10N_26	A14
23	RXD2	RX_DATA2			IO_L9N_AD3N_26	G14
24	RXD1	RX_DATA1			IO_L2P_AD10P_26	B14
25	RXD0	RX_DATA0			IO_L10P_AD2P_26	H14
26	RXC	RX_CLK			IO_L8N_HDGC_AD4N_26	E15
29	TXC	TX_CLK			IO_L8P_HDGC_AD4P_26	F15
30	TXEN	TX_ENA			IO_L11N_AD1N_26	J14
31	TXD0	TX_DATA0			IO_L1N_AD11N_26	A15
32	TXD1	TX_DATA1			IO_L1P_AD11P_26	B15
35	TXD2	TX_DATA2			IO_L9P_AD3P_26	G15
37	TXD3	TX_DATA3			IO_L12N_AD0N_26	L13
39	LED0	LED_LINK_ACT_0_0			IO_L11P_AD1P_26	K14
42	RESET#	NPHY_RESET_OUT0_0			IO_L12P_AD0P_26	L14
PHY1						
16	MDIO	MDIO	26	VCCO_26	IO_L5P_HDGC_AD7P_26	D15
17	MCLK	MCLK			IO_L5N_HDGC_AD7N_26	D14
18	RXERR	RX_ERR	25	VCCO_25	IO_L9N_AD11N_25	B10
19	RXDV	RX_DV			IO_L10P_AD10P_25	B11
20	RXD3	RX_DATA3			IO_L10N_AD10N_25	A10
23	RXD2	RX_DATA2			IO_L11N_AD9N_25	A11
24	RXD1	RX_DATA1			IO_L3N_AD13N_25	G10
25	RXD0	RX_DATA0			IO_L11P_AD9P_25	A12
26	RXC	RX_CLK			IO_L8N_HDGC_25	D11
29	TXC	TX_CLK			IO_L8P_HDGC_25	E12
30	TXEN	TX_ENA			IO_L9P_AD11P_25	C11
31	TXD0	TX_DATA0			IO_L12N_AD8N_25	C12
32	TXD1	TX_DATA1			IO_L12P_AD8P_25	D12
35	TXD2	TX_DATA2			IO_L3P_AD13P_25	H11
37	TXD3	TX_DATA3			IO_L4P_AD12P_25	J12
39	LED0	LED_LINK_ACT_0_1			IO_L2N_AD14N_25	K12
42	RESET#	NPHY_RESET_OUT1_0			IO_L4N_AD12N_25	H12

PHY Pin#	PHY Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
PHY2						
16	MDIO	MDIO	24	VCCO_24	IO_L5P_HDGC_24	AD15
17	MCLK	MCLK			IO_L5N_HDGC_24	AD14
18	RXERR	RX_ERR			IO_L12N_AD8N_24	AA12
19	RXDV	RX_DV			IO_L9N_AD11N_24	W13
20	RXD3	RX_DATA3			IO_L11N_AD9N_24	W11
23	RXD2	RX_DATA2			IO_L12P_AD8P_24	Y12
24	RXD1	RX_DATA1			IO_L11P_AD9P_24	W12
25	RXD0	RX_DATA0			IO_L9P_AD11P_24	W14
26	RXC	RX_CLK			IO_L8N_HDGC_24	AB14
29	TXC	TX_CLK			IO_L8P_HDGC_24	AB15
30	TXEN	TX_ENA			IO_L10N_AD10N_24	Y13
31	TXD0	TX_DATA0			IO_L10P_AD10P_24	Y14
32	TXD1	TX_DATA1			IO_L1N_AD15N_24	AE14
35	TXD2	TX_DATA2			IO_L1P_AD15P_24	AE15
37	TXD3	TX_DATA3			IO_L2P_AD14P_24	AG14
39	LED0	LED_LINK_ACT_1_0			IO_L2N_AD14N_24	AH14
42	RESET#	NPHY_RESET_OUT0_1			IO_L3P_AD13P_24	AG13
PHY3						
16	MDIO	MDIO	24	VCCO_24	IO_L5P_HDGC_24	AD15
17	MCLK	MCLK			IO_L5N_HDGC_24	AD14
18	RXERR	RX_ERR	44	VCCO_44	IO_L1N_AD11N_44	AH10
19	RXDV	RX_DV			IO_L2P_AD10P_44	AG11
20	RXD3	RX_DATA3			IO_L1P_AD11P_44	AG10
23	RXD2	RX_DATA2			IO_L2N_AD10N_44	AG11
24	RXD1	RX_DATA1			IO_L3P_AD9P_44	AH12
25	RXD0	RX_DATA0			IO_L11N_AD1N_44	AA8
26	RXC	RX_CLK			IO_L8N_HDGC_AD4N_44	AC11
29	TXC	TX_CLK			IO_L8P_HDGC_AD4P_44	AB11
30	TXEN	TX_ENA			IO_L12N_AD0N_44	AB9
31	TXD0	TX_DATA0			IO_L12P_AD0P_44	AB10
32	TXD1	TX_DATA1			IO_L11P_AD1P_44	Y9
35	TXD2	TX_DATA2			IO_L10N_AD2N_44	Y10
37	TXD3	TX_DATA3			IO_L10P_AD2P_44	W10
39	LED0	LED_LINK_ACT_1_1			IO_L9N_AD3N_44	AA10
42	RESET#	NPHY_RESET_OUT1_1			IO_L9P_AD3P_44	AA11

PHY Pin#	PHY Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
PHY4						
16	MDIO	MDIO	66	VCCO_66 VREF_66	IO_L20P_T3L_N2_AD1P_66	C6
17	MCLK	MCLK			IO_L20N_T3L_N3_AD1N_66	B6
18	RXERR	RX_ERR			IO_L17P_T2U_N8_AD10P_66	F8
19	RXDV	RX_DV			IO_L18N_T2U_N11_AD2N_66	D9
20	RXD3	RX_DATA3			IO_T2U_N12_66	E7
23	RXD2	RX_DATA2			IO_L18P_T2U_N10_AD2P_66	E9
24	RXD1	RX_DATA1			IO_L17N_T2U_N9_AD10N_66	E8
25	RXD0	RX_DATA0			IO_L21N_T3L_N5_AD8N_66	A6
26	RXC	RX_CLK			IO_L14N_T2L_N3_GC_66	D5
29	TXC	TX_CLK			IO_L14P_T2L_N2_GC_66	E5
30	TXEN	TX_ENA			IO_L22P_T3U_N6_DBC_AD0P_66	C8
31	TXD0	TX_DATA0			IO_L21P_T3L_N4_AD8P_66	A7
32	TXD1	TX_DATA1			IO_L22N_T3U_N7_DBC_AD0N_6	B8
35	TXD2	TX_DATA2			IO_L23N_T3U_N9_66	A8
37	TXD3	TX_DATA3			IO_L23P_T3U_N8_66	A9
39	LED0	LED_LINK_ACT_2_0			IO_L24N_T3U_N11_66	B9
42	RESET#	NPHY_RESET_OUT0_2			IO_L24P_T3U_N10_66	C9
PHY5						
16	MDIO	MDIO	66	VCCO_66 VREF_66	IO_L20P_T3L_N2_AD1P_66	C6
17	MCLK	MCLK			IO_L20N_T3L_N3_AD1N_66	B6
18	RXERR	RX_ERR			IO_T0U_N12_VRP_66	G4
19	RXDV	RX_DV			IO_L6P_T0U_N10_AD6P_66	G5
20	RXD3	RX_DATA3			IO_L5N_T0U_N9_AD14N_66	E3
23	RXD2	RX_DATA2			IO_L7P_T1L_N0_QBC_AD13P_66	C1
24	RXD1	RX_DATA1			IO_T1U_N12_66	D2
25	RXD0	RX_DATA0			IO_L7N_T1L_N1_QBC_AD13N_66	B1
26	RXC	RX_CLK			IO_L13P_T2L_N0_GC_QBC_66	D7
29	TXC	TX_CLK			IO_L12N_T1U_N11_GC_66	C2
30	TXEN	TX_ENA			IO_L6N_T0U_N11_AD6N_66	F5
31	TXD0	TX_DATA0			IO_L8N_T1L_N3_AD5N_66	A1
32	TXD1	TX_DATA1			IO_L9P_T1L_N4_AD12P_66	B3
35	TXD2	TX_DATA2			IO_L8P_T1L_N2_AD5P_66	A2
37	TXD3	TX_DATA3			IO_L10P_T1U_N6_QBC_AD4P_66	B4
39	LED0	LED_LINK_ACT_2_1			IO_L10N_T1U_N7_QBC_AD4N_66	A4
42	RESET#	NPHY_RESET_OUT1_2			IO_L9N_T1L_N5_AD12N_66	A3

PHY Pin#	PHY Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
PHY6						
16	MDIO	MDIO	65	VCCO_65 VREF_65	IO_L20P_T3L_N2_AD1P_65	J6
17	MCLK	MCLK			IO_L20N_T3L_N3_AD1N_65	H6
18	RXERR	RX_ERR			IO_T2U_N12_65	P9
19	RXDV	RX_DV			IO_L18N_T2U_N11_AD2N_65	L8
20	RXD3	RX_DATA3			IO_L17P_T2U_N8_AD10P_65	N9
23	RXD2	RX_DATA2			IO_L18P_T2U_N10_AD2P_65	M8
24	RXD1	RX_DATA1			IO_L17N_T2U_N9_AD10N_65	N8
25	RXD0	RX_DATA0			IO_L22N_T3U_N7_DBC_AD0N_65	K7
26	RXC	RX_CLK			IO_L14N_T2L_N3_GC_65	L5
29	TXC	TX_CLK			IO_L14P_T2L_N2_GC_65	M6
30	TXEN	TX_ENA			IO_L22P_T3U_N6_DBC_AD0P_65	K8
31	TXD0	TX_DATA0			IO_L21P_T3L_N4_AD8P_65	J7
32	TXD1	TX_DATA1			IO_L21N_T3L_N5_AD8N_65	H7
35	TXD2	TX_DATA2			IO_L24N_T3U_N11_PERSTN0_65	H8
37	TXD3	TX_DATA3			IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	H9
39	LED0	LED_LINK_ACT_3_0			IO_L23P_T3U_N8_I2C_SCLK_65	K9
42	RESET#	NPHY_RESET_OUT0_3			IO_L23N_T3U_N9_65	J9
PHY7						
16	MDIO	MDIO	65	VCCO_65 VREF_65	IO_L20P_T3L_N2_AD1P_65	J6
17	MCLK	MCLK			IO_L20N_T3L_N3_AD1N_65	H6
18	RXERR	RX_ERR			IO_T0U_N12_VRP_65	W9
19	RXDV	RX_DV			IO_L7P_T1L_N0_QBC_AD13P_65	L1
20	RXD3	RX_DATA3			IO_L6N_T0U_N11_AD6N_65	T6
23	RXD2	RX_DATA2			IO_L6P_T0U_N10_AD6P_65	R6
24	RXD1	RX_DATA1			IO_L5N_T0U_N9_AD14N_65	T7
25	RXD0	RX_DATA0			IO_L9P_T1L_N4_AD12P_65	K2
26	RXC	RX_CLK			IO_L13P_T2L_N0_GC_QBC_65	L7
29	TXC	TX_CLK			IO_L13N_T2L_N1_GC_QBC_65	L6
30	TXEN	TX_ENA			IO_L7N_T1L_N1_QBC_AD13N_65	K1
31	TXD0	TX_DATA0			IO_L9N_T1L_N5_AD12N_65	J2
32	TXD1	TX_DATA1			IO_L8P_T1L_N2_AD5P_65	J1
35	TXD2	TX_DATA2			IO_T1U_N12_65	H2
37	TXD3	TX_DATA3			IO_L10N_T1U_N7_QBC_AD4N_65	H3
39	LED0	LED_LINK_ACT_3_1			IO_L10P_T1U_N6_QBC_AD4P_65	H4
42	RESET#	NPHY_RESET_OUT1_3			IO_L8N_T1L_N3_AD5N_65	H1

Table 18 – Memory to FPGA Pin-Out

Memory Pin#	Memory Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
Micro-SD						
1	DAT2/RSV	SDIO_1_D2	501	VCCO_PSIO1_501	PS_MIO48	J21
2	CD/DAT3/$\overline{CS}$	SDIO_1_D3			PS_MIO49	M18
3	CMD/DI	SDIO_1_CMD			PS_MIO50	M19
5	CLK/SCLK	SDIO_1_CLK			PS_MIO51	L21
7	DAT0/DO	SDIO_1_D0			PS_MIO46	L20
8	DAT1/RSV	SDIO_1_D1			PS_MIO47	H21
QSPI						
B2	C	QSPI_SCL	500	VCCO_PSIO0_500	PS_MIO0	AG15
C2	S#	QSPI_CS			PS_MIO5	AD16
C4	W#/DQ2	QSPI_IO_2			PS_MIO2	AF15
D2	DQ1	QSPI_IO_1			PS_MIO1	AG16
D3	DQ0	QSPI_IO_0			PS_MIO4	AH16
D4	DQ3	QSPI_IO_3			PS_MIO3	AH15

Table 19 – Backplane Connector J1A to FPGA Pin-Out

J1 Pin#	J1 Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
11	TX0+	PORT0-TX_P	505	VCCO_PSDDR_505	PS_MGTRTXP0_505	E25
12	TX0-	PORT0-TX_N			PS_MGTRTXN0_505	E26
14	RX0+	PORT0-RX_P			PS_MGTRRXP0_505	F27
15	RX0-	PORT0-RX_N			PS_MGTRRXN0_505	F28
20	TX1+	PORT1-TX_P			PS_MGTRTXP1_505	D23
21	TX1-	PORT1-TX_N			PS_MGTRTXN1_505	D24
23	RX1+	PORT1-RX_P			PS_MGTRRXP1_505	D27
24	RX1-	PORT1-RX_N			PS_MGTRRXN1_505	D28
44	TX4+	PORT4-TX_P			PS_MGTRTXP3_505	B23
45	TX4-	PORT4-TX_N			PS_MGTRTXN3_505	B24
47	RX4+	PORT4-RX_P			PS_MGTRRXP3_505	A25
48	RX4-	PORT4-RX_N			PS_MGTRRXN3_505	A26
74	TCLKA+	TCLKA_P	64	VCCO_64VREF_64	IO_L23P_T3U_N8_64	AH2
75	TCLKA-	TCLKA_N			IO_L23N_T3U_N9_64	AH1
77	TCLKB+	TCLKB_P			IO_L24P_T3U_N10_64	AF1
78	TCLKB-	TCLKB_N			IO_L24N_T3U_N11_6	AG1
80	FCLKA+	FCLKA_P	505	VCCO_PSDDR_505	PS_MGTREFCLK0P_505	F23
81	FCLKA-	FCLKA_N			PS_MGTREFCLK0N_505	F24

Table 20 - Backplane Connector J1B to FPGA Pin-Out

J1 Pin#	J1 Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
87	RX8-	PORT8-RX_N	505	VCCO_ PSDDR_505	PS_MGTRRXN2_505	B28
88	RX8+	PORT8-RX_P			PS_MGTRRXP2_505	B27
90	TX8-	PORT8-TX_N			PS_MGTRTXN2_505	C26
91	TX8+	PORT8-TX_P			PS_MGTRTXP2_505	C25
111	RX12-	PORT12-RX_N	64	VCCO_64 VREF_64	IO_L1N_T0L_N1_DBC_64	AD9
112	RX12+	PORT12-RX_P			IO_L1P_T0L_N0_DBC_64	AC9
114	TX12-	PORT12-TX_N			IO_L4N_T0U_N7_DBC_AD7N_64	AE7
115	TX12+	PORT12-TX_P			IO_L4P_T0U_N6_DBC_AD7P_64	AD7
117	RX13-	PORT13-RX_N			IO_L2N_T0L_N3_64	AE8
118	RX13+	PORT13-RX_P			IO_L2P_T0L_N2_64	AE9
120	TX13-	PORT13-TX_N			IO_L5N_T0U_N9_AD14N_64	AC7
121	TX13+	PORT13-TX_P			IO_L5P_T0U_N8_AD14P_64	AB7
123	RX14-	PORT14-RX_N			IO_L3N_T0L_N5_AD15N_64	AC8
124	RX14+	PORT14-RX_P			IO_L3P_T0L_N4_AD15P_64	AB8
126	TX14-	PORT14-TX_N			IO_L6N_T0U_N11_AD6N_64	AC6
127	TX14+	PORT14-TX_P			IO_L6P_T0U_N10_AD6P_64	AB6
129	RX15-	PORT15-RX_N			IO_L7N_T1L_N1_QBC_AD13N_64	AH9
130	RX15+	PORT15-RX_P			IO_L7P_T1L_N0_QBC_AD13P_64	AG9
132	TX15-	PORT15-TX_N			IO_L10N_T1U_N7_QBC_AD4N_64	AG5
133	TX15+	PORT15-TX_P			IO_L10P_T1U_N6_QBC_AD4P_64	AG6
135	TCLKC-	TCLKC_N			IO_L14N_T2L_N3_GC_64	AC3
136	TCLKC+	TCLKC_P			IO_L14P_T2L_N2_GC_64	AC4
138	TCLKD-	TCLKD_N			IO_L13N_T2L_N1_GC_QBC_64	AD4
139	TCLKD+	TCLKD_P			IO_L13P_T2L_N0_GC_QBC_64	AD5

J1 Pin#	J1 Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
141	RX17-	PORT17-RX_N	64	VCCO_64 VREF_64	I/O: IO_L17N_T2U_N9_AD10N_64	AC2
142	RX17+	PORT17-RX_P			R̄/W: IO_L18N_T2U_N11_AD2N_64	AC1
144	TX17-	PORT17-TX_N			I/O: IO_L17P_T2U_N8_AD10P_64	AB2
145	TX17+	PORT17-TX_P			R̄/W: IO_L18P_T2U_N10_AD2P_64	AB1
147	RX18-	PORT18-RX_N			I/O: IO_L15N_T2L_N5_AD11N_64	AB3
148	RX18+	PORT18-RX_P			R̄/W: IO_L16N_T2U_N7_QBC_AD3N_64	AD1
150	TX18-	PORT18-TX_N			I/O: IO_L15P_T2L_N4_AD11P_64	AB4
151	TX18+	PORT18-TX_P			R̄/W: IO_L16P_T2U_N6_QBC_AD3P_64	AD2
153	RX19-	PORT19-RX_N			I/O: IO_L20N_T3L_N3_AD1N_64	AH3
154	RX19+	PORT19-RX_P			R̄/W: IO_L21N_T3L_N5_AD8N_64	AF3
156	TX19-	PORT19-TX_N			I/O: IO_L20P_T3L_N2_AD1P_64	AG3
157	TX19+	PORT19-TX_P			R̄/W: IO_L21P_T3L_N4_AD8P_64	AE3
159	RX20-	PORT20-RX_N			I/O: IO_T3U_N12_64	AE4
160	RX20+	PORT20-RX_P			R̄/W: IO_L19N_T3L_N1_DBC_AD9N_64	AH4
162	TX20-	PORT20-TX_N			I/O: IO_T2U_N12_64	AB5
163	TX20+	PORT20-TX_P			R̄/W: IO_L19P_T3L_N0_DBC_AD9P_64	AG4

Note: Differential signals from AMC Port 17..20 (LVDS) are converted to single ended signals. The I/O signal contains the payload information, the R̄/W part sets the direction of the signal.

Table 21 – PLL to FPGA Pin-Out

PLL Pin#	PLL Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
9	CLK3B	REFCLK_2_N	505	VCCO_ PSDDR_505	PS_MGTREFCLK2N_505	C22
10	CLK3A	REFCLK_2_P			PS_MGTREFCLK2P_505	C21
13	CLK2B	REFCLK_1_N			PS_MGTREFCLK1N_505	E22
14	CLK2A	REFCLK_1_P			PS_MGTREFCLK1P_505	E21
18	CLK1A	ECAT_CLK1	26	VCCO_26	IO_L7P_HDGC_AD5P_26	G13
			24	VCCO_24	IO_L7P_HDGC_24	AA13
17	CLK1B	ECAT_CLK2	66	VCCO_66 VREF_66	IO_L12P_T1U_N10_GC_66	C3
			65	VCCO_65 VREF_65	IO_L12P_T1U_N10_GC_65	L3

Table 22 – FPGA Management Pin-Out

Pin#	Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
JTAG-MUX						
3	COM2	TCK	503	VCCO_PSIO3 _503	PS_JTAG_TCK	R19
4	COM3	TDI			PS_JTAG_TDI	R18
6	COM4	TDO			PS_JTAG_TDO	T21
1	COM1	TMS			PS_JTAG_TMS	N21
Serial-MUX						
* via Bus-Transceiver *		PS_UART_TX	500	VCCO_PSIO0 _500	PS_MIO7	AH17
		PS_UART_RX			PS_MIO6	AF16
I²C						
* via bus *		I²C_SCL_3V3	500	VCCO_PSIO0 _500	PS_MIO10	AD17
		I²C_SDA_3V3			PS_MIO11	AE17

Table 23 – MMC to FPGA Pin-Out

MMC Pin#	MMC Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
26	PD0	PS_DONE	503	VCCO_PSIO3 _503	PS_DONE	M21
27	PD1	PS_INIT_B			PS_INIT_B	P21
28	PD2	PS_POR_B			PS_POR_B	P16
41	PE5	PS_SRST_B			PS_SRST_B	N19

Table 24 – SFP to FPGA Pin-Out

SFP Pin#	SFP Label	Signal	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
3	TX_DISABLE	OSFP0TX0 DISAB	500	VCCO_PSIO0_500	PS_MIO9	AC16
7	RATE SELECT	SFP_RATES ELECT			PS_MIO12	AC17
12	RD-	SFP_RX_N	64	VCCO_64 VREF_64	IO_L11N_T1U_N9_GC_64	AF6
13	RD+	SFP_RX_P			IO_L11P_T1U_N8_GC_64	AF7
18	TD+	SFP_TX_P			IO_L8P_T1L_N2_AD5P_64	AF8
19	TD-	SFP_TX_N			IO_L8N_T1L_N3_AD5N_64	AG8

Table 25 – LED to FPGA Pin-Out

LED#	Color	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
FPGA_LED_0	Yellow	44	VCCO_44	IO_L4P_AD8P_44	AE10
FPGA_LED_1	Green			IO_L4N_AD8N_44	AF10
FPGA_LED_2	Green	501	VCCO_PSIO1_501	PS_MIO27	J15
FPGA_LED_3	Green			PS_MIO26	L15
FPGA_LED_4	Red	44	VCCO_44	IO_L6P_HDGC_AD6P_44	AC12
FPGA_LED_5	Green			IO_L6N_HDGC_AD6N_44	AD12

Table 26 – DIP-Switch to FPGA Pin-Out

Switch#	FPGA Bank	VCCO	FPGA Pin Name	FPGA Pin#
SW3-1	503	VCCO_PSIO3_503	PS_MODE0	P19
SW3-2			PS_MODE1	P20
SW4-1			PS_MODE2	R20
SW4-2			PS_MODE3	T20
SW7-3	65	VCCO_65 VREF_65	IO_L1N_T0L_N1_DBC_65	Y8
SW7-4			IO_L1P_T0L_N0_DBC_65	W8
SW8-3			IO_L2N_T0L_N3_65	V9
SW8-4			IO_L2P_T0L_N2_65	U9

7. SPECIFICATIONS AND COMPLIANCES

7.1. Internal Reference Documentation

- none

7.2. External Reference Documentation

- Atmel ATxmega128 Microcontroller Data Sheet, Rev. 8386E, 09/2014
- Microchip KSZ8061MNG PHY Data Sheet, DS00002038D, 01/2019
- Nanya NT5AD512M16A4-HRI DDR4 RAM Datasheet, V1.8, 12/2018
- XILINX Zynq Ultrascale+ MPSoC Data Sheet, DS925 (v1.18), 08/2020

7.3. Standards Compliance

- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- PICMG AMC.2 Rev. 1.0
- IPMI Specification v1.5 Rev. 1.0
- PICMG HPM.1

7.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle,

so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.7. Product Safety

The board complies with EN60950 and UL1950.

7.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally

being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7.9. Abbreviation List

Table 27 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
ARM	Processor Architecture with reduced instruction set
CPU	Central Processing Unit
DDR4 DRAM	Double Data Rate Dynamic RAM
EtherCAT	***Ether***net for ***C***ontrol ***A***utomation ***T***echnology
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GPIO	General Purpose I/O
HS	Hot Swap
I/O	Input / Output
I^2C	Inter-Integrated Circuit
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LVDS	Low Voltage Differential Signaling
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
MicroSD Card	Micro Secure Digital Memory Card
MLVDS	Multipoint LVDS
MPSoC	Multiprocessor SoC
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
QSPI	Quad SPI
RAM	Random Access Memory
SerDes	Serializer/Deserializer
SFP	Small Form-Factor Pluggable
SoC	System on a Chip
SPI (FLASH)	Serial Peripheral Interface (FLASH)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

8. DOCUMENT'S HISTORY

Table 28 – Document's History

Rev	Date	Description	Author
1.0	10.11.2020	• initial release	Se
	18.02.2021	• Updated chapters 4.3 Front Panel Interfaces and 4.5 Microcontroller • Added chapter 6 FPGA Pin-Out • Minor changes	se
	29.04.2021	• Added preliminary title photo • Minor changes	se
1.1	30.04.2024	• Updated cover page • Updated chapter 5.1 Front Panel and LEDs • Updated Figure 6 – Location Diagram – Bottom • Updated chapter 5.3.11 X1 – Ethernet Connector	se