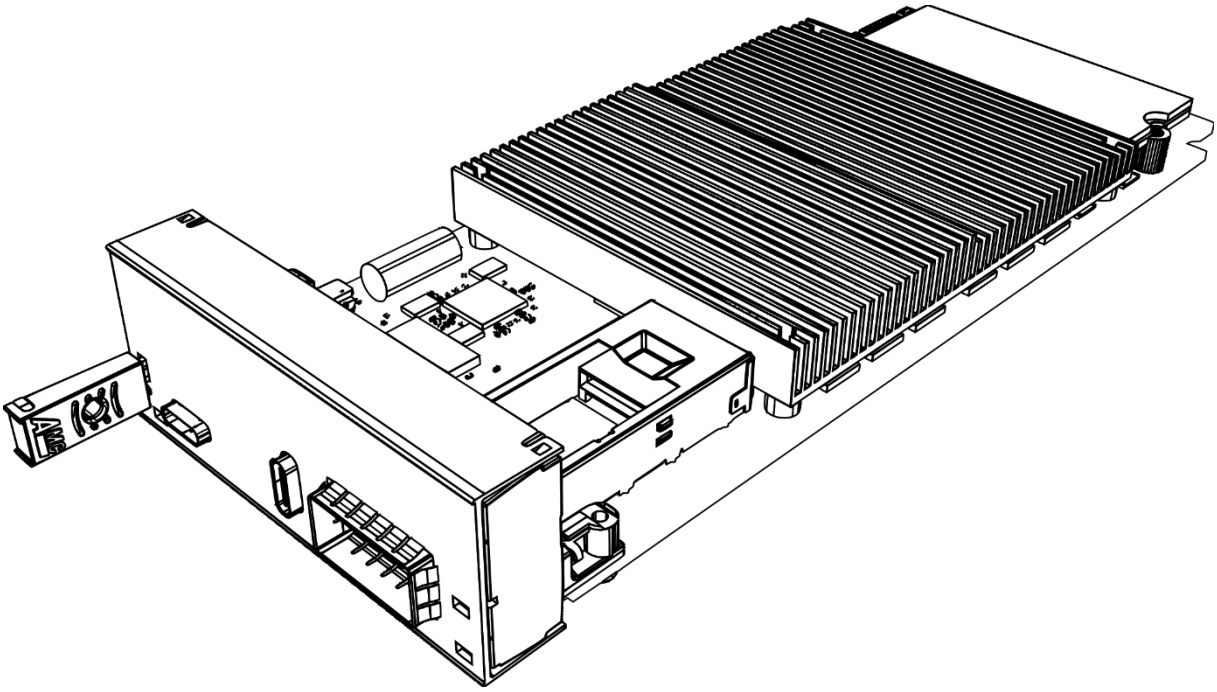
NAT-AMC-LX2

AMC PROCESSOR BOARD

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.2

HW REVISION 1.X

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. PREFACE

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-AMC-LX2's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-AMC-LX2's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-AMC-LX2** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-AMC-LX2's** main features

Hardware

Information about LEDs and connectors

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-AMC-LX2** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-AMC-LX2** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-AMC-LX2** is a versatile Processing AMC (PrAMC), covering a wide field of network-related applications.

It supports any voice or data application with requirements such as deep packet inspection, encryption, protocol conversion, or Layer 2-7 routing. Moreover, it can serve as, e.g. multi-service switch, edge router, radio network controller (RNC), VoIP/VoP gateway and router, or mobile network equipment.

As successor of the **NAMC-QorIQ-P2/P3/P4** series, the **NAT-AMC-LX2** strikes with the latest generation of NXP ARM CPUs. With up to 16 Cortex-A72 cores, PCIe- and SerDes-Interfaces as well as an Ethernet switch on-chip, the Layerscape LX2160A CPU is ideally suited for networking-related usage.

Apart from its 16 cores, multiple PCIe- and 40/100GbE interfaces, special hardware for Ethernet frame processing, and a security hardware engine, the LX2160A processor stands out by its superior power efficiency.

By its onboard M.2 socket, a PCIe-x4- or SATA-coupled SSD can be realized. The M.2 socket can also be used to provide a USB3 or PCIe-x4 extension for any custom application.

The QSFP28-Transceiver slot offers various front panel interface options:

- 1x 40G / 100G Ethernet (SR4)
- 4x 10G / 25G Ethernet (SR)
- 2x 50G Ethernet (SR2)

2.1. Main Features

Table 1 – Main Features

Form Factor		
	• Single-width, full- or mid-sized AMC • Width: 73.5 mm, Depth: 180.6 mm	
Processing Resources		
	LX2160	**LX2080**
CPU	• 16x ARM Cortex-A72 cores @ up to 2.2 GHz • 2x 72b DDR4 Controller @ up to 3200 MHz • 32KB/48KB L1 Cache • 8MB L2 Cache • 24 SerDes • Embedded Ethernet Switch • Encryption • TDP 26.9W	• 8x ARM Cortex-A72 cores @ up to 1.8 GHz • 2x 72b DDR4 Controller @ up to 2600 MHz • 32KB/48KB L1 Cache • 8MB L2 Cache • 24 SerDes • Embedded Ethernet Switch • TDP 11W
Memory	• 2x 16GB x8DDRAM4 ECC (72bit): up to 32GB total • 256MB QSPI • SPI MRAM • Up to 2x 16Gb eMMC • MicroSD-Card	
MMC	• Atmel ATxMega 128	
Software	• Linux	
Front Panel Connectivity		

	• QSFP28-Transceiver
	  • 1x 40G / 100G Ethernet (SR4)
	  • 4x 10G / 25G Ethernet (SR)
	  • 2x 50G Ethernet (SR2)
	• USB3 Type C to LX2 CPU
	• USB2 Type C to UART converter for control / debug
	• Status / Fault / Hot-Swap LEDs
	• MicroSD-Card Slot	

Backplane Connectivity		
Backplane	• TCLKA-D • 1-10GbE at AMC Ports 0/1 • SATA at AMC Ports 2/3 • PCIe x4 at AMC Ports 4-7 • PCIe x4 / 40-100GbE (depending on backplane) at AMC Ports 8-11	
Compliance		
	• MTCA.0, AMC.0, AMC.1, AMC.2 • IMPI V1.5 • HMP.1 • CE, RoHS, REACH	
Environmental		
Operating Environment	• 0 to +55 degrees Celsius • Humidity: 5% to 95% (non-condensing)	
Storage Environment	• -40 to +185 degrees Celsius • Humidity: 5% to 95% (non-condensing)	

Order Codes	
-2080	• LX2080SN71826B processor (8x A72 cores), 8GB DDR4
-2160	• LX2160SE72232B processor (16x A72 cores), 32GB DDR4

3. QUICK START

To ensure proper functioning of the **NAT-AMC-LX2** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the connectors to ensure proper contact when connecting the **NAT-AMC-LX2** to the MTCA-System.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The installation requires a MicroTCA backplane, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-AMC-LX2**, read the Installation Guide and the User's Manual of the **NAT-AMC-LX2** and the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is Hot-Swap capable, if you don't switch off the power.

Ensure that the **NAT-AMC-LX2** is connected with the connector(s) completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the rear panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-AMC-LX2** must meet the following specifications:

- +12V / 4A max.
- + 3,3V / 0.15A max.

3.3.2. Hot-Swap

The **NAT-AMC-LX2** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-AMC-LX2** or the system it is plugged into from damage!

Insertion of a hot-swap-capable module

- Ensure the module and the backplane support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-AMC-LX2** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane detects the board
- If the information provided by the **NAT-AMC-LX2** is valid, the backplane enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable module

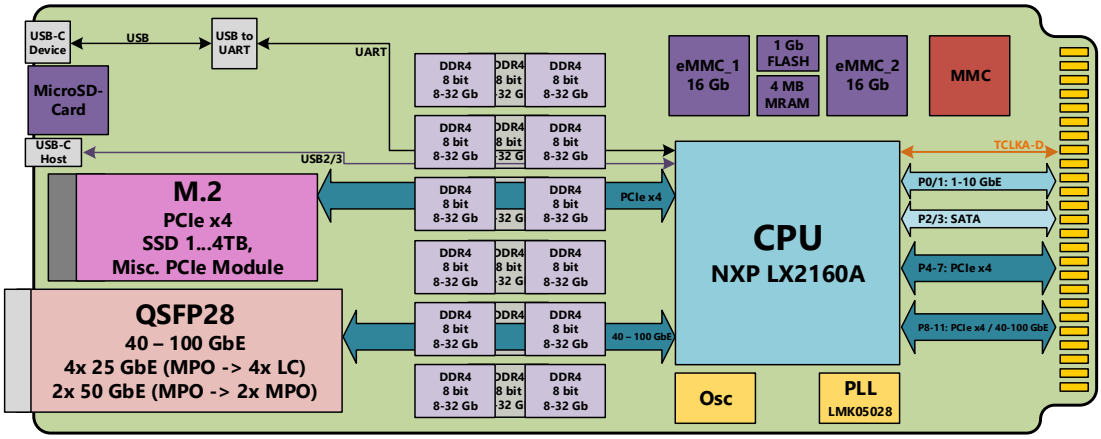
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane disables payload power
- The HS-LED turns solid on
- Pull the **NAT-AMC-LX2** carefully out of the backplane

4. FUNCTIONAL DESCRIPTION

The **NAT-AMC-LX2** can be divided into several functional blocks, which are described in the following paragraphs.

The following figures give an overview of the functional blocks.

Figure 1 – Block Diagram NAT-AMC-LX2



4.1. CPU

The **NAT-AMC-LX2** is available with two CPU variants. Main differences between both types are shown in the table below, for detailed information, please refer to chapter 6.2 External Reference Documentation.

Table 2 – CPU Type Comparison

Feature	LX2160	LX2080
# ARM Cortex-A72 CPU cores	16	8
Max. operating frequency	2200 MHz	1800 MHz
Max. DRAM frequency	3200 MHz	2600 MHz
TDP	26.9 W	11 W
Encryption	Yes	No

4.2. DRAM

All variants of the **NAT-AMC-LX2** provide two 72bit DRAM controllers with ECC. Eighteen x8 DDR4 SDRAM bricks result in a storage capacity of 32 GB.

4.3. M.2 Interface

The M.2 interface is a mass storage interface intended to be used with an SSD or FLASH memory. Via PCIe x4, SATA, or USB3, it supports SSDs with a capacity from 1 – 4 TB.

Important note:

Polarity of several signals and dedicated M.2 interface pins is swapped intentionally! This is indicated by **bold lettering**!

Table 3 – M.2 Interface: Pin Assignment

Pin #	Signal	Pin Label	Pin Label	Signal	Pin #
1	CONFIG_3	CONFIG_3	3.3V	3.3V	2
3	GND	GND	3.3V	3.3V	4
5	M.2_PCIE4_RX_N	PERn3	NC	nc	6
7	M.2_PCIE4_RX_P	PERp3	NC	nc	8
9	GND	GND	DAS/DSS#	LED4	10
11	**M.2_PCIE4_TX_P**	**PETn3**	3.3V	3.3V	12
13	**M.2_PCIE4_TX_N**	**PETp3**	3.3V	3.3V	14
15	GND	GND	3.3V	3.3V	16
17	**M.2_PCIE3_RX_P**	**PERn2**	3.3V	3.3V	18
19	**M.2_PCIE3_RX_N**	**PERp2**	NC	nc	20
21	CONFIG_0	CONFIG_0	NC	nc	22
23	**M.2_PCIE3_TX_P**	**PETn2**	NC	nc	24
25	**M.2_PCIE3_TX_N**	**PETp2**	NC	nc	26
27	GND	GND	NC	nc	28
29	M.2_PCIE2_RX_N	PERn1	NC	nc	30
31	M.2_PCIE2_RX_P	PERp1	NC	nc	32
33	GND	GND	NC	nc	34
35	**M.2_PCIE2_TX_P**	**PETn1**	NC	nc	36
37	**M.2_PCIE2_TX_N**	**PETn2**	DEVSLP	SLEEP	38
39	GND	GND	SMB_CLK	3V3_LX2_I2C1_SCL	40
41	M.2_PCIE1_RX_N	PERn0	SMB_DATA	3V3_LX2_I2C1_SDA	42
43	M.2_PCIE1_RX_P	PETp0	ALERT#	SMB_ALERTn_3V3	44
45	GND	GND	NC	nc	46
47	**M.2_PCIE1_TX_P**	**PETn0**	NC	nc	48
49	**M.2_PCIE1_TX_N**	**PETp0**	PERST#	CE_CB_RESET#_3V3	50
51	GND	GND	CLKREQ#	CLKREQ_M2#_3V3	52
53	PCIE_CLK_N	REFCLKn	PEWAKE#	CE_WAKE0#_3V3	54
55	PCIE_CLK_P	REFCLKp	NC	nc	56
57	GND	GND	NC	nc	58
59					60
61					62
63					64
65					66
67	nc	NC	SUSCLK	SUSCLK	68
69	CONFIG_1	CONFIG_1	3.3V	3V3	70
71	GND	GND	3.3V	3V3	72
73	GND	GND	3.3V	3V3	74
75	CONFIG_2	CONFIG_2	3.3V	3V3	76

4.3.1. Further Memory Items

The **NAT-AMC-LX2** provides several memory items attached to GPIO banks 1 and 2 of the LX2 CPU:

- MicroSD Card
- 2x eMMC with 16Gb storage capacity each
- 1Gb Serial NOR FLASH
- 4MB QSPI MRAM

Figure 2 – GPIO1: eMMC_1 and MicroSD Card

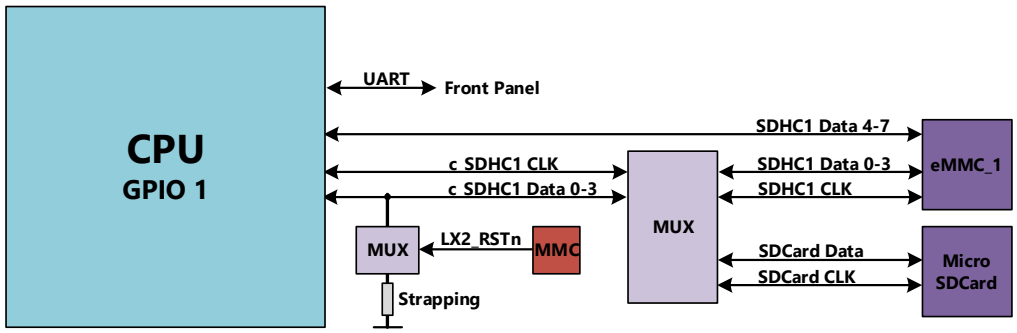


Table 4 – GPIO1: Signal Assignment

Signal Name	CPU Lane	CPU Pin#
UART_CTS	GPIO1_DAT08	A6
UART_RTS	GPIO1_DAT09	A5
UART_RX	GPIO1_DAT10	B5
UART_TX	GPIO1_DAT11	B6
SDHC1_DAT7	GPIO1_DAT12	C3
SDHC1_DAT6	GPIO1_DAT13	B3
SDHC1_DAT5	GPIO1_DAT14	A4
SDHC1_DAT4	GPIO1_DAT15	A3
c_SDHC1_CLK	GPIO1_DAT16	D1
c_SDHC1_DAT0	GPIO1_DAT17	F1
c_SDHC1_DAT1	GPIO1_DAT18	E2
c_SDHC1_DAT2	GPIO1_DAT19	C1
c_SDHC1_DAT3	GPIO1_DAT20	C2
c_SDHC1_CMD	GPIO1_DAT21	E1
CLKREQ_M2#	GPIO1_DAT24	D3
CE_CB_RESET#	GPIO1_DAT25	C4
SMB_ALERTn	GPIO1_DAT26	L5
SD/eMMC	GPIO1_DAT27	K5
CE_WAKE0#	GPIO1_DAT29	B2
LX2_I2C1_SDA	GPIO1_DAT30	E4
LX2_I2C1_SCL	GPIO1_DAT31	E3

Figure 3 – GPIO2: eMMC_2 and QSPI

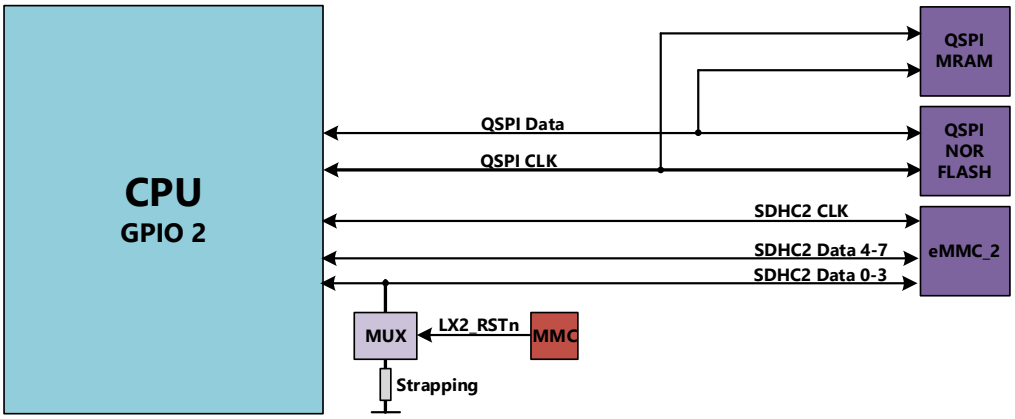


Table 5 – GPIO2: Signal Assignment

Signal Name	CPU Lane	CPU Pin#
c_SDHC2_CLK	GPIO2_DAT10	C25
SDHC2_DAT0	GPIO2_DAT11	A23
SDHC2_DAT1	GPIO2_DAT12	C24
SDHC2_DAT2	GPIO2_DAT13	B23
SDHC2_DAT3	GPIO2_DAT14	A24
SDHC2_DAT4	GPIO2_DAT15	C26
SDHC2_DAT5	GPIO2_DAT16	B27
SDHC2_DAT6	GPIO2_DAT17	A26
SDHC2_DAT7	GPIO2_DAT18	A27
SDHC2_CMD	GPIO2_DAT19	B25
QSPI_FLASH_CS1#	GPIO2_DAT20	D23
QSPI_FLASH_CS0#	GPIO2_DAT21	C23
c_QSPI_FLASH_CLK	GPIO2_DAT22	D22
QSPI_FLASH_DO	GPIO2_DAT24	F25
QSPI_FLASH_D1	GPIO2_DAT25	E24
QSPI_FLASH_D2	GPIO2_DAT26	E26
QSPI_FLASH_D3	GPIO2_DAT27	E27

4.4. Clocking

The onboard LMK 05028 PLL is supported by several oscillators.

Figure 4 – PLL Connectivity

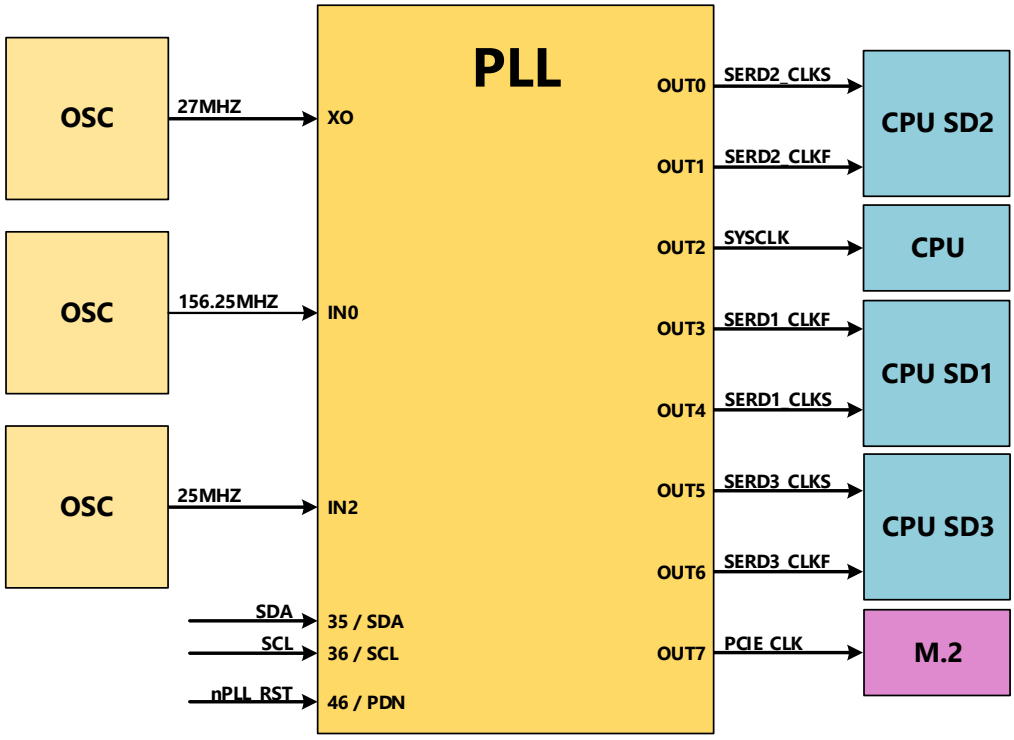


Table 6 – PLL Clock I/O Assignment

Pin #	Input-Signal	Pin Label	Pin Label	Output-Signal	Frequency (MHz)	Pin #
1	156.25MHZ_N	IN0_P	OUT0_P	SERD2_CLKS_P	161.1328125	22
2	156.25MHZ_P	IN0_N	OUT0_N	SERD2_CLKS_N		23
10	25MHZ_N	IN2_P	OUT1_N	SERD2_CLKF_N	100	26
11	25MHZ_P	IN_2_N	OUT1_P	SERD2_CLKF_P		27
43	27MHZ_N	XO_P	OUT2_P	SYSCLK_P	100	31
44	27_MHZ_P	XO_N	OUT2_N	SYSCLK_N		32
			OUT3_N	SERD1_CLKF_N	100	33
			OUT3_P	SERD1_CLKF_P		34
			OUT4_P	SERD1_CLKS_P	161.1328125	51
			OUT4_N	SERD1_CLKS_N		52
			OUT5_N	SERD3_CLKS_N	161.1328125	53
			OUT5_P	SERD3_CLKS_P		54
			OUT6_P	SERD3_CLKF_P	100	57
			OUT6_N	SERD3_CLKF_N		58
			OUT7_N	PCIE_CLK_N	100	61
			OUT7_P	PCIE_CLK_P		62

4.5. MMC

A Microchip ATxmega128 works as Module Management Controller (MMC).

4.6. Front Panel Interfaces

4.6.1. QSFP28 Interface

Typically, the **NAT-AMC-LX2's** QSFP28 slot is operated with an MPO receptable, which offers several transceiving options:

1x 40G / 100G Ethernet (SR4)

Four lanes are combined to one 40G / 100G port.

Figure 5 – QSFP28: SR4 Assignment

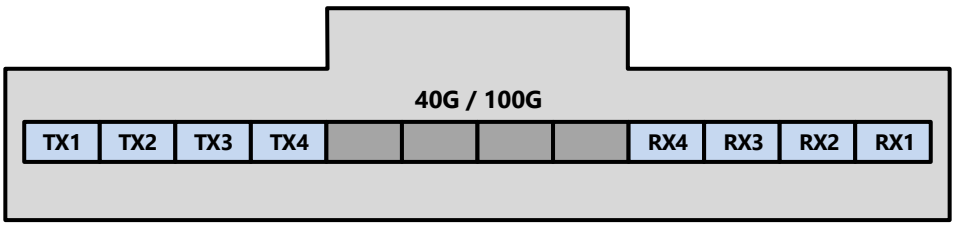


Figure 6 – QSFP28: MPO – MPO Cable for SR4 Transmission Mode

4x 10G / 25G Ethernet (SR)

The QSFP28 port is split up into four single lanes, each optical lane is operated separately. By software, the port must be configured to single connections (e.g. 4 x 25G), the interface mode changes from SR4 to SR.

Figure 7 – QSFP28: SR Assignment

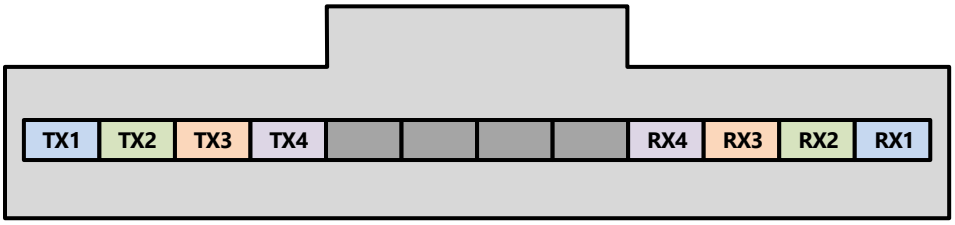
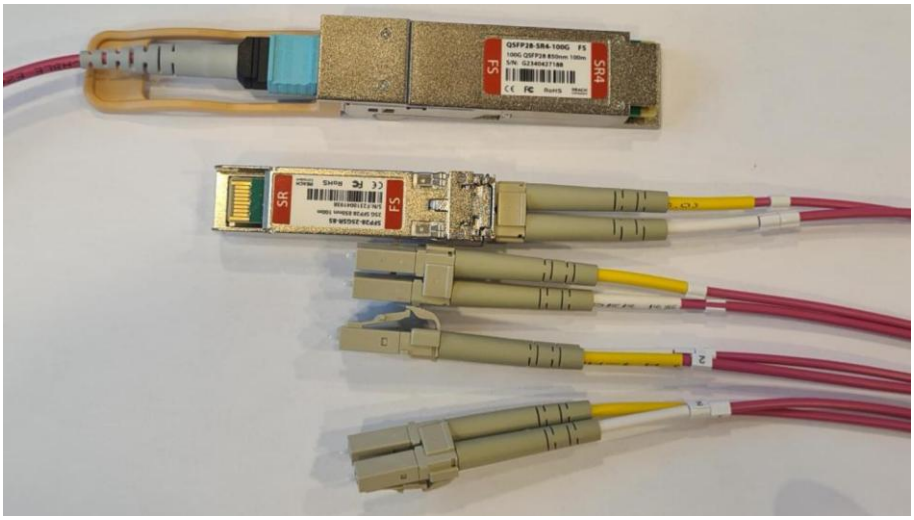


Figure 8 – QSFP28: MPO – 4xLC Cable for SR Transmission Mode



2x 50G Ethernet (SR2)

SR2 is supported by the **NAT-AMC-LX2** as well. The QSFP28 port is split into two optical lanes, a connection can be realized by an MPO – 2xMPO Cable.

Direct Attached Cable (DAC)

Beyond fiber connections, the QSFP28 transceiver cage can be equipped with a copper-based Direct Attached Cable (DAC).

Figure 9 – Direct Attached Cable (DAC)

Please keep in mind that depending on the field of application, speed, and distance, the transmission quality of this connection type may be insufficient.

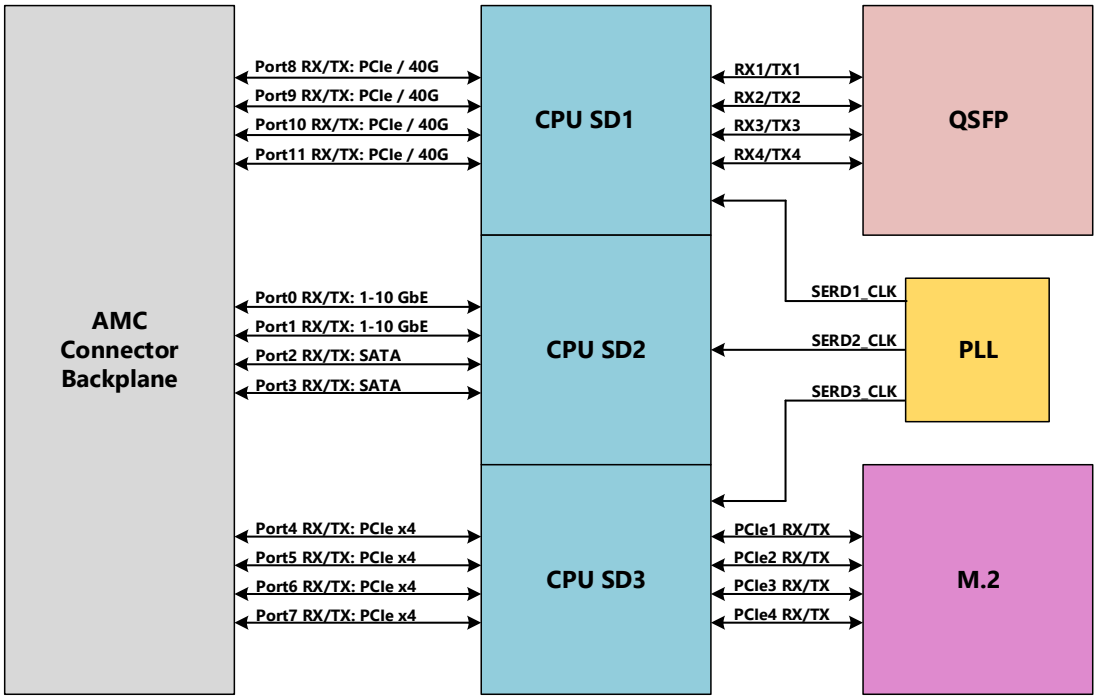
4.6.2. USB Interfaces

The **NAT-AMC-LX2** features two USB type C interfaces at the front plate. One is directly connected to the CPU; the other one is used for debug functionality. Please see Table 16 – Front Panel Connector Labelling and Function for details.

4.7. SerDes Connectivity

The diagram below gives an overview of the Serdes connectivity. Details are described in the following table.

Figure 10 – SerDes Connectivity Overview



Important note for all tables in this paragraph:

Polarity / assignment of several signals and dedicated CPU pins is swapped intentionally! This is indicated by **bold lettering**!

Table 7 – SerDes Signal Assignment CPU SD1 – Backplane

Signal Name	CPU SD1 Lane	CPU Pin#
PORT8_RX_N	**SD1_RX4_P**	**AU14**
PORT8_RX_P	**SD1_RX4_N**	**AT14**
PORT8_TX_N	**SD1_TX4_P**	**AM14**
PORT8_TX_P	**SD1_TX4_N**	**AL14**
PORT9_RX_N	**SD1_RX5_P**	**AW15**
PORT9_RX_P	**SD1_RX5_N**	**AV15**
PORT9_TX_P	SD1_TX5_P	AP15
PORT9_TX_N	SD1_TX5_N	AN15
PORT10_RX_N	**SD1_RX6_P**	**AU16**
PORT10_RX_P	**SD1_RX6_N**	**AT16**
PORT10_TX_N	**SD1_TX6_P**	**AM16**
PORT10_TX_P	**SD1_TX6_N**	**AL16**
PORT11_RX_N	**SD1_RX7_P**	**AW17**
PORT11_RX_P	**SD1_RX7_N**	**AV17**
PORT11_TX_P	SD1_TX7_P	AP17
PORT11_TX_N	SD1_TX7_N	AN17

Table 8 – SerDes Signal Assignment CPU SD1 – QSFP Transceiver

Signal Name	CPU SD1 Lane	CPU Pin#
QSFP_RX1_P	SD1_RX0_P	AW9
QSFP_RX1_N	SD1_RX0_N	AV9
QSFP_TX1_N	**SD1_TX0_P**	**AP9**
QSFP_TX1_P	**SD1_TX0_N**	**AN9**
QSFP_RX2_P	SD1_RX1_P	AU10
QSFP_RX2_N	SD1_RX1_N	AT10
QSFP_TX2_N	**SD1_TX1_P**	**AM10**
QSFP_TX2_P	**SD1_TX1_N**	**AL10**
QSFP_RX3_P	SD1_RX2_P	AW11
QSFP_RX3_N	SD1_RX2_N	AV11
QSFP_TX3_N	**SD1_TX2_P**	**AP11**
QSFP_TX3_P	**SD1_TX2_N**	**AN11**
QSFP_RX4_P	SD1_RX3_P	AU12
QSFP_RX4_N	SD1_RX3_N	AT12
QSFP_TX4_N	**SD1_TX3_P**	**AM12**
QSFP_TX4_P	**SD1_TX3_N**	**AL12**

Table 9 – SerDes Clock Assignment CPU SD1 – PLL

Signal Name	CPU SD1 Lane	CPU Pin#
SERD1_CLKF_P	**SD1_PLLS_REF_CLK_P**	**AR13**
SERD1_CLKF_N	**SD1_PLLS_REF_CLK_N**	**AP13**
SERD1_CLKS_P	**SD1_PLLF_REF_CLK_P**	**AW13**
SERD1_CLKS_N	**SD1_PLLF_REF_CLK_N**	**AV13**

Table 10 – SerDes Signal Assignment CPU SD2 – Backplane

Signal Name	CPU SD2 Lane	CPU Pin#
PORT0_RX_N	**SD2_RX6_P**	**AU26**
PORT0_RX_P	**SD2_RX6_N**	**AT26**
PORT0_TX_P	SD2_TX6_P	AM26
PORT0_TX_N	SD2_TX6_N	AL26
PORT1_RX_P	SD2_RX7_P	AW27
PORT1_RX_N	SD2_RX7_N	AV27
PORT1_TX_P	SD2_TX7_P	AP27
PORT1_TX_N	SD2_TX7_N	AN27
PORT2_RX_P	SD2_RX4_P	AU24
PORT2_RX_N	SD2_RX4_N	AT24
PORT2_TX_P	SD2_TX4_P	AM24
PORT2_TX_N	SD2_TX4_N	AL24
PORT3_RX_N	**SD2_RX5_P**	**AW25**
PORT3_RX_P	**SD2_RX5_N**	**AV25**
PORT3_TX_P	SD2_TX5_P	AP25
PORT3_TX_N	SD2_TX5_N	AN25

Table 11 – SerDes Clock Assignment CPU SD2 – PLL

Signal Name	CPU SD2 Lane	CPU Pin#
SERD2_CLKF_P	**SD2_PLLS_REF_CLK_P**	**AV23**
SERD2_CLKF_N	**SD2_PLLS_REF_CLK_N**	**AW23**
SERD2_CLKS_P	**SD2_PLLF_REF_CLK_P**	**AP23**
SERD2_CLKS_N	**SD2_PLLF_REF_CLK_N**	**AR23**

Table 12 – SerDes Signal Assignment CPU SD3 – Backplane

Signal Name	CPU SD3 Lane	CPU Pin#
PORT4_RX_P	SD3_RX0_P	A13
PORT4_RX_N	SD3_RX0_N	B13
PORT4_TX_P	SD3_TX0_P	F13
PORT4_TX_N	SD3_TX0_N	G13
PORT5_RX_P	SD3_RX1_P	C14
PORT5_RX_N	SD3_RX1_N	D14
PORT5_TX_N	SD3_TX1_P	H14
PORT5_TX_P	SD3_TX1_N	J14
PORT6_RX_N	**SD3_RX2_P**	**A15**
PORT6_RX_P	**SD3_RX2_N**	**B15**
PORT6_TX_P	SD3_TX2_P	F15
PORT6_TX_N	SD3_TX2_N	G15
PORT7_RX_P	SD3_RX3_P	C16
PORT7_RX_N	SD3_RX3_N	D16
PORT7_TX_P	SD3_TX3_P	H16
PORT7_TX_N	SD3_TX3_N	J16

Table 13 – SerDes Signal Assignment CPU SD3 – M.2 Interface

Signal Name	CPU SD3 Lane	CPU Pin#
M.2_PCIE1_RX_P	SD3_RX4_P	C18
M.2_PCIE1_RX_N	SD3_RX4_N	D18
M.2_PCIE1_TX_P	SD3_TX4_P	H18
M.2_PCIE1_TX_N	SD3_TX4_N	J18
M.2_PCIE2_RX_P	SD3_RX5_P	A19
M.2_PCIE2_RX_N	SD3_RX5_N	B19
M.2_PCIE2_TX_P	SD3_TX5_P	F19
M.2_PCIE2_TX_N	SD3_TX5_N	G19
M.2_PCIE3_RX_P	SD3_RX6_P	C20
M.2_PCIE3_RX_N	SD3_RX6_N	D20
M.2_PCIE3_TX_P	SD3_TX6_P	H20
M.2_PCIE3_TX_N	SD3_TX6_N	J20
M.2_PCIE4_RX_P	SD3_RX7_P	A21
M.2_PCIE4_RX_N	SD3_RX7_N	B21
M.2_PCIE4_TX_P	SD3_TX7_P	F21
M.2_PCIE4_TX_N	SD3_TX7_N	G21

Table 14 – SerDes Clock Assignment CPU SD3 – PLL

Signal Name	CPU SD3 Lane	CPU Pin#
SERD3_CLKF_N	SD3_PLLS_REF_CLK_P	B17
SERD3_CLKF_P	SD3_PLLS_REF_CLK_N	A17
SERD3_CLKS_P	SD3_PLLF_REF_CLK_P	F17
SERD3_CLKS_N	SD3_PLLF_REF_CLK_N	E17

5. HARDWARE

5.1. Front Panel and LEDs

The **NAT-AMC-COMex** is equipped with various LEDs described in the following section. The figure below shows the full-sized front panel; the interfaces for both sizes are identical.

Figure 11 – NAT-AMC-LX2: Front Panel Full-Sized

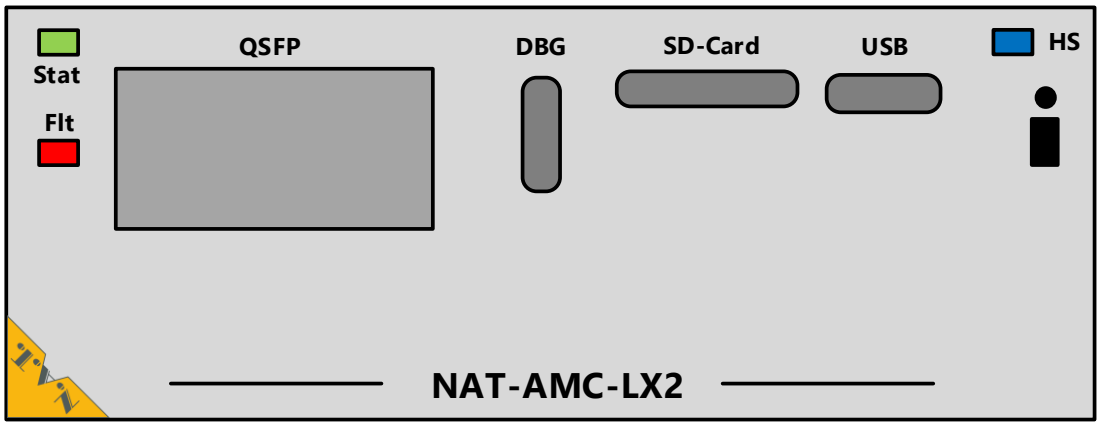


Table 15 – LED Functionality

LED	Color	Function	Description
Stat	Green	tbd	AMC Status – General Purpose
	Yellow	tbd	AMC Status – General Purpose
Flt	Red	ON	Temperature exceeding / underrunning threshold level
		OFF	Temperature OK
HS	Blue	ON	AMC Hot Swap LED please refer to chapter 3.3.2 Hot-Swap
		blink	
		OFF	

Note: Although appearing as one LED optically, the AMC GP LED consists of two LEDs (green and yellow) physically, sharing the same hole in the front plate.

5.2. Connector- and Switch Location

Figure 12 – Connector- and Switch Location

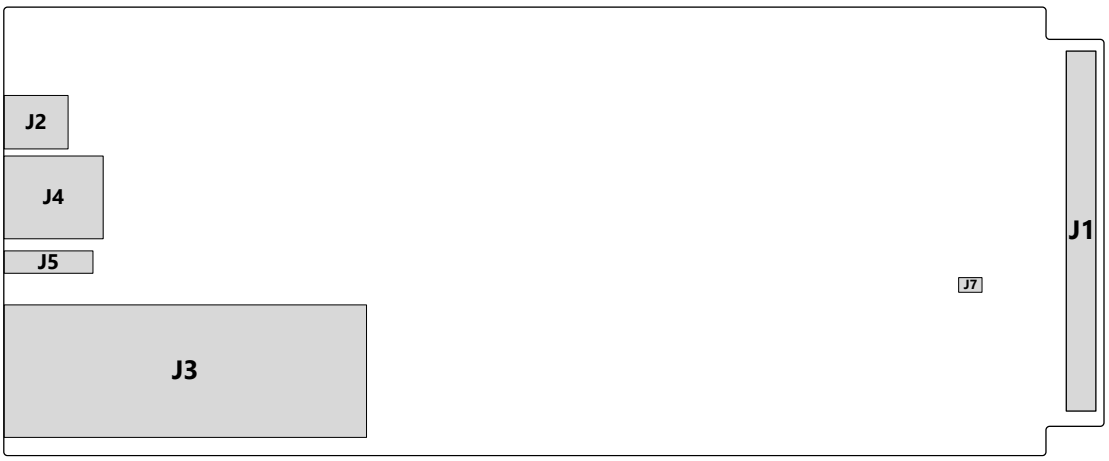


Table 16 – Front Panel Connector Labelling and Function

#	Label	Standard	Function
J2	USB	USB3 Type C	• Connects directly to host interface of LX2 CPU • Allows to control other devices
J3	QSFP	QSFP28 Transceiver Slot	• Typically populated by MPO receptables
J4	MMC	MicroSD-Card	• Custom use
J5	DBG	USB2 Type C	• Connects to the USB/UART converter • Used for controlling and debugging functionality

5.2.1. J1: AMC Edge Connector

The **NAT-AMC-LX2** connects to the backplane via J1.

Figure 13 – J1: AMC Edge Connector (top view)

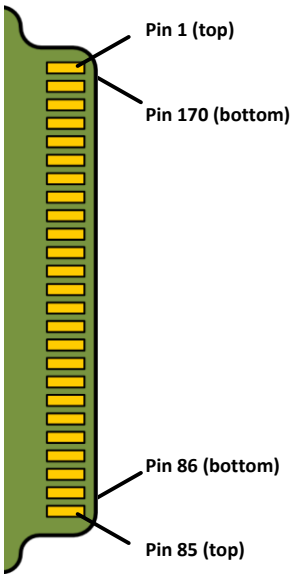


Table 17 – J1: AMC Edge Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	+12V	LX_TDI	169
3	/AMC_PS1	LX2_TDO	168
4	+3.3V_MP	LX2_TRST	167
5	BKP_GA0	LX2_TMS	166
6	nc	LX2_TCK	165
7	GND	GND	164
8	nc	nc	163
9	+12V	nc	162
10	GND	GND	161
11	PORT0_Tx_P	nc	160
12	PORT0_Tx_N	nc	159
13	GND	GND	158
14	PORT0_Rx_P	nc	157
15	PORT0_Rx_N	nc	156
16	GND	GND	155
17	BKP_GA1	nc	154
18	+12V	nc	153
19	GND	GND	152
20	PORT1_Tx_P	nc	151
21	PORT1_Tx_N	nc	150
22	GND	GND	149

Pin #	Signal	Signal	Pin #
23	PORT1_Rx_P	nc	148
24	PORT1_Rx_N	nc	147
25	GND	GND	146
26	BKP_GA2	nc	145
27	+12V	nc	144
28	GND	GND	143
29	PORT2_Tx_P	nc	142
30	PORT2_Tx_N	nc	141
31	GND	GND	140
32	PORT2_Rx_P	nc	139
33	PORT2_Rx_N	nc	138
34	GND	GND	137
35	PORT3_Tx_P	nc	136
36	PORT3_Tx_N	nc	135
37	GND	GND	134
38	PORT3_Rx_P	nc	133
39	PORT3_Rx_N	nc	132
40	GND	GND	131
41	BKP./ENABLE	nc	130
42	+12V	nc	129
43	GND	GND	128
44	PORT4_Tx_P	nc	127
45	PORT4_Tx_N	nc	126
46	GND	GND	125
47	PORT4_Rx_P	nc	124
48	PORT4_Rx_N	nc	123
49	GND	GND	122
50	PORT5_Tx_P	nc	121
51	PORT5_Tx_N	nc	120
52	GND	GND	119
53	PORT5_Rx_P	nc	118
54	PORT5_Rx_N	nc	117
55	GND	GND	116
56	IPMI_SCL	nc	115
57	+12V	nc	114
58	GND	GND	113
59	PORT6_Tx_P	nc	112
60	PORT6_Tx_N	nc	111
61	GND	GND	110
62	PORT6_Rx_P	PORT11_Tx_P	109
63	PORT6_Rx_N	PORT11_Tx_N	108
64	GND	GND	107
65	PORT7_Tx_P	PORT11_Rx_P	106
66	PORT7_Tx_N	PORT11_Rx_N	105
67	GND	GND	104
68	PORT7_Rx_P	PORT10_Tx_P	103
69	PORT7_Rx_N	PORT10_Tx_N	102
70	GND	GND	101
71	IPMI_SDA	PORT10_Rx_P	100

Pin #	Signal	Signal	Pin #
72	+12V	PORT10_Rx_N	99
73	GND	GND	98
74	AMC_TCLKA_P	PORT9_Tx_P	97
75	AMC_TCKLA_N	PORT9_Tx_N	96
76	GND	GND	95
77	AMC_TCLKB_P	PORT9_Rx_P	94
78	AMC_TCKLB_N	PORT9_Rx_N	93
79	GND	GND	92
80	AMC_FCLKA_P	PORT8_Tx_P	91
81	AMC_FCKLA_N	PORT8_Tx_N	90
82	GND	GND	89
83	/AMC_PS0	PORT8_Rx_P	88
84	+12V	PORT8_Rx_N	87
85	GND	GND	86

5.2.2. J7: Microcontroller Programming Header

J7 is a programming header for the Atmel ATxmega µC.

Table 18 – J7: Microcontroller Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V_MP	2
3	nc	nc	4
5	PDI_CLK	GND	6

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

- NAT Europe

6.2. External Reference Documentation

- NXP LX2160 Fact Sheet

6.3. Standards Compliance

- MTCA.0
- AMC.0
- AMC.1
- AMC.2
- IMPI V1.5
- HMP.1

6.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.7. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6.8. Abbreviation List

Table 19 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
ARM (CPU)	Processor Architecture with reduced instruction set
CPU	Central Processing Unit
DDR (RAM)	Double Data Rate RAM
eMMC	embedded Multimedia Card
FLASH	Non-Volatile Memory
GbE	Gigabit Ethernet
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
M.2	Specification for internally mounted computer expansion cards
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
MMC	Module Management Controller
MRAM	Magnetoresistive RAM
PCI(e)	Peripheral Component Interconnect (Express)
PLL	Phase-Locked Loop
PrAMC	Processor AMC
QSFP	Quad SFP
QSPI	Quad SPI
RAM	Random Access Memory
RNC	Radio Network Controller
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SerDes	Serializer/Deserializer
SFP	Small Form-Factor Pluggable
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SSD	Solid State Drive
TDP	Thermal Design Power
UART	Universal Asynchronous Receiver/Transmitter
VoIP	Voice over IP
VoP	Voice Operator Panel – softphone software

7. DOCUMENT'S HISTORY

Table 20 – Document's History

Rev	Date	Description	Author
1.0	26.02.2025	• initial release	Se
1.1	06.03.2025	• PLL channel assignment corrected	Se/te
1.2	31.03.2025	• Highlighted polarity swap for SerDes Assignment (Table 7 – SerDes Signal Assignment CPU SD1 – Backplane)	se