NXMC-4E1
E1 Line Interface XMC Module
Technical Reference Manual V1.1
HW Revision 1.0

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x. Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DMA	Direct Memory Access
E1	PDH signal – data rate 2.048 Mbit/s
EEPROM	Electrically Erasable PROM
FLASH	Non-volatile Memory
FPGA	Field Programmable Gate Array
I^2C	Inter-Integrated Circuit
IP	Internet Protocol
JTAG	Joint Test Action Group
LED	Light Emitting Diode
PCI(e)	Peripheral Component Interconnect (Express)
PDH	Plesiochronous Digital Hierarchy
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
PSTN	Public Switched Telephone Network
RAM	Random Access Memory
RX	Receiver
SPI	Serial Peripheral Interface
TDM	Time Division Multiplex
TX	Transmitter
VoIP	Voice over IP
XMC	Switch Memory Card

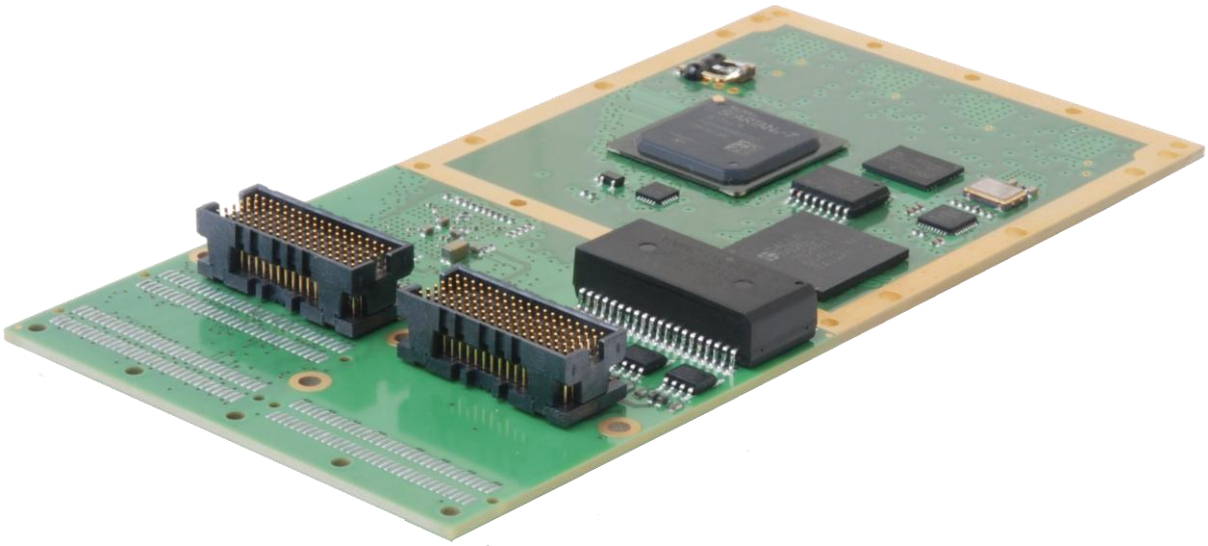
1 Introduction

The **NXMC-4E1** is a line interface Switched Mezzanine Card (XMC) to be mounted on a suitable carrier board (e.g. **NPCIe-XMC-4E1**). The carrier must provide physical E1-interfaces towards a face plate as the **NXMC-4E1** does not.

The **NXMC-4E1** processes incoming data from E1- into PCI- or PCIe-standard (assembly option), the data is delivered directly to the host memory. A typical application of the **NXMC-4E1** may be the conversion between PSTN and VoIP (software required, e.g. Asterisk).

The following figure shows a photo of the **NXMC-4E1.**

Figure 1: NXMC-4E1 (PCIe-Option)



2 Overview

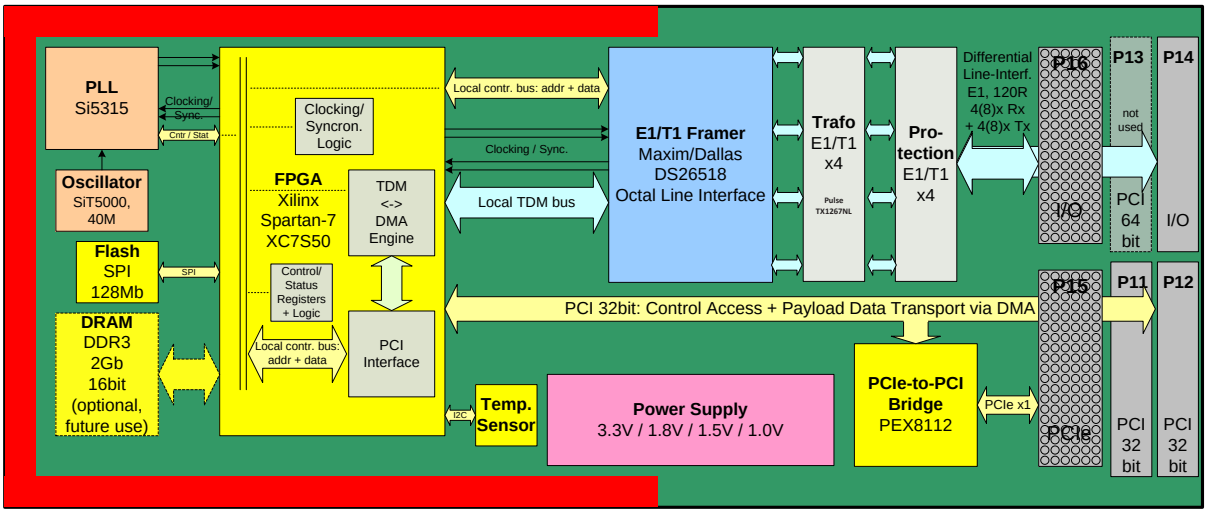
2.1 Major Features

- XILINX Spartan-7 FPGA XC7S50
- Maxim/Dallas DS26518 E1/T1-Framer
- PLX PEX8112 PCIe-to-PCI Bridge
- FLASH-memory and FPGA-attached DRAM for future extensions

2.2 Block Diagram

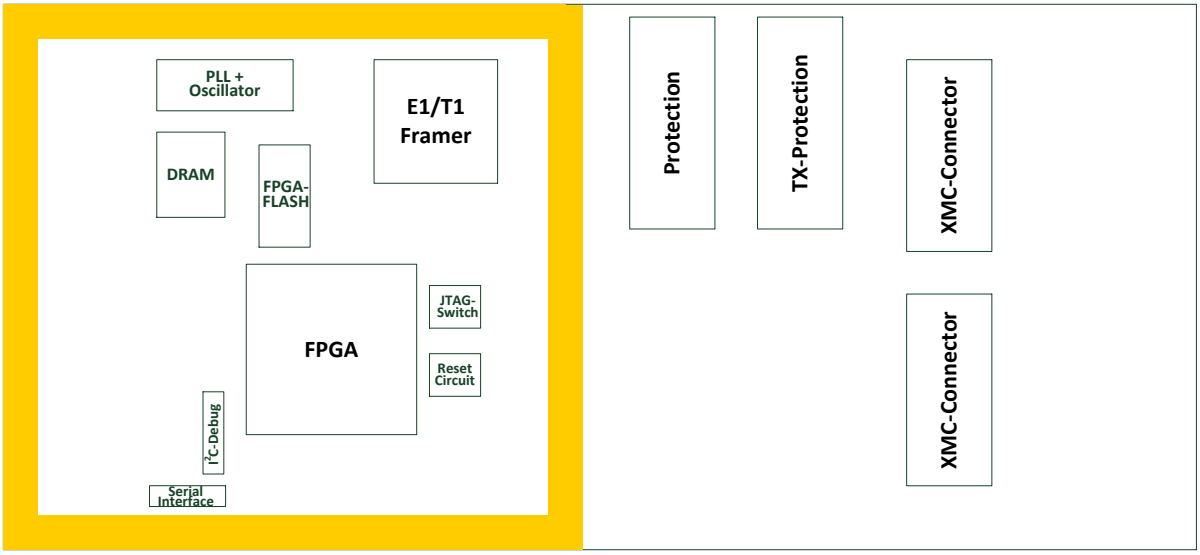
The following figure shows a detailed block diagram of the **NXMC-4E1**.

Figure 2: NXMC-4E1 – Block Diagram

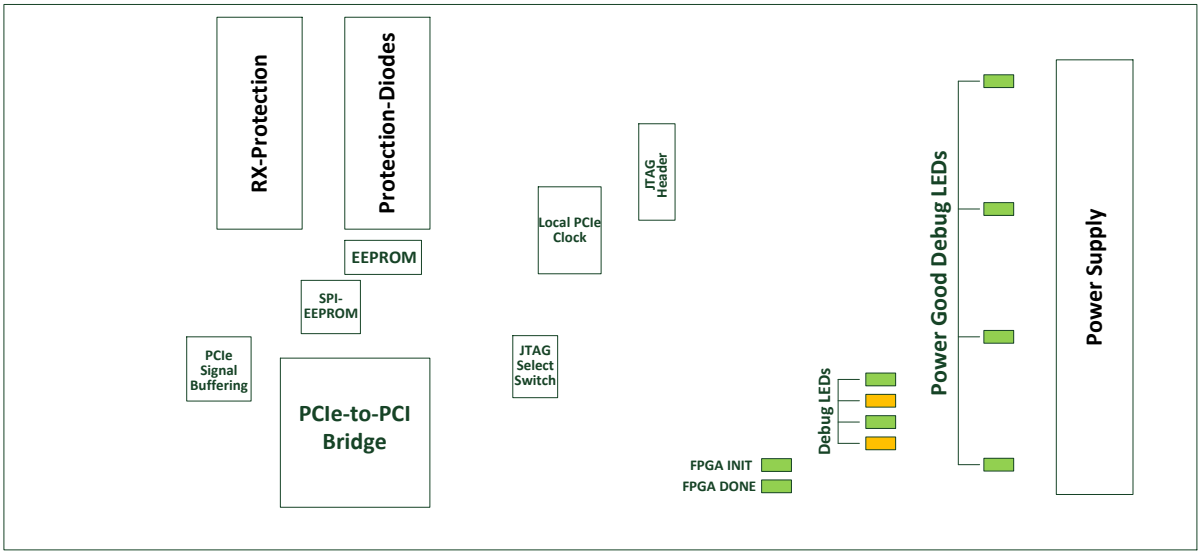


2.3 Location Diagram

Figure 3: NXMC-4E1 – PCIe-Option – Location Diagram

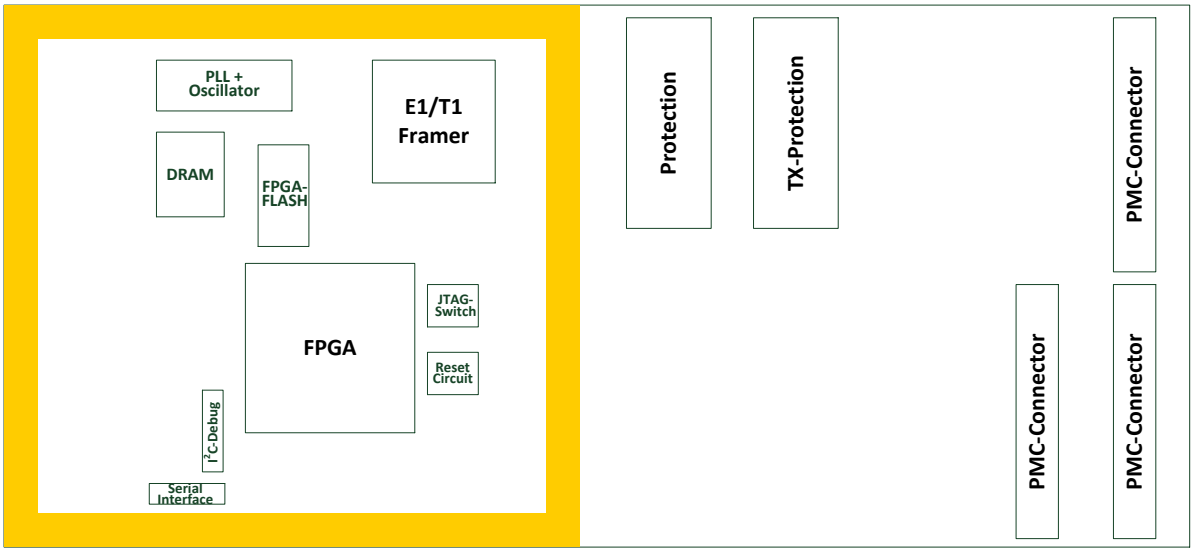


Top View

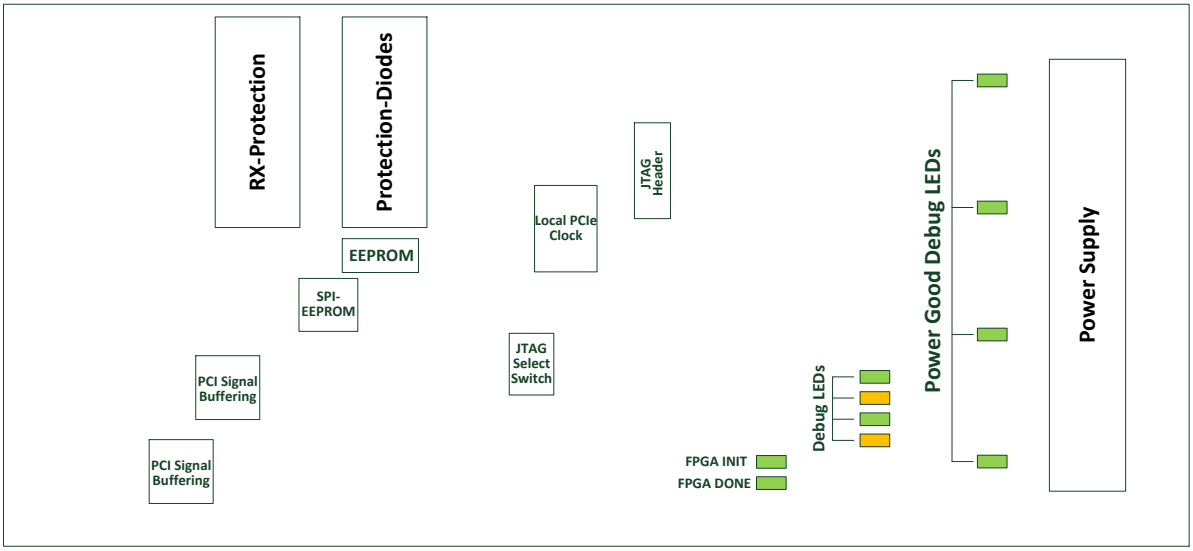


Bottom View

Figure 4: NXMC-4E1 – PCI-Option – Location Diagram



Top View



Bottom View

3 Board Features

The **NXMC-4E1** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 FPGA

The central component on the **NXMC-4E1** is a Xilinx Spartan-7 XC7S50 FPGA which implements a PCI interface that connects the PCI to an internal local-bus-system. On this local-bus various sections are memory-mapped:

- General control/status registers
- Clock/synchronization control/status block
- Access to E1-framer
- DMA engine control/status

So the **NXMC-4E1** uses just one PCI-window (size < 1MB) being mapped into the host PCI memory.

3.2 E1-Framer

The **NXMC-4E1** is equipped with a Maxim/Dallas DS26518, a high-sensitive E1/T1 framer chip which transmits data from/to standard E1 to/from TDM.

3.3 PCIe-to-PCI Bridge

PCIe-to-PCI-conversion is processed by a PLX PEX8112 PCIe-to-PCI Bridge.

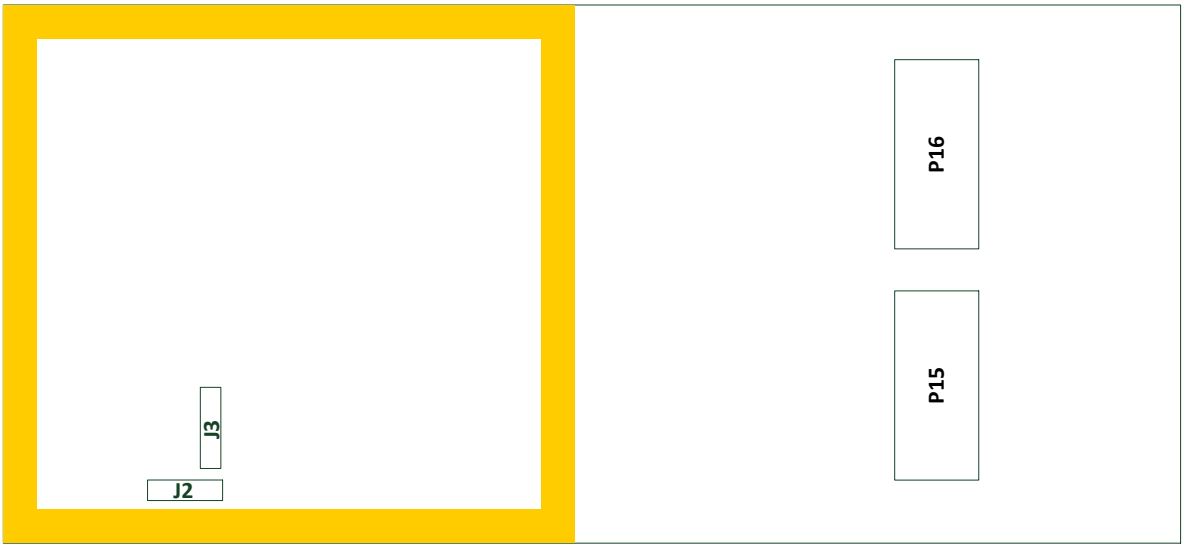
3.4 Memory

The **NXMC-4E1** provides 64 MB SPI-FLASH and 512 MB 8-bit-wide DDR3 DRAM (optional), both directly connected to the FPGA, for future use.

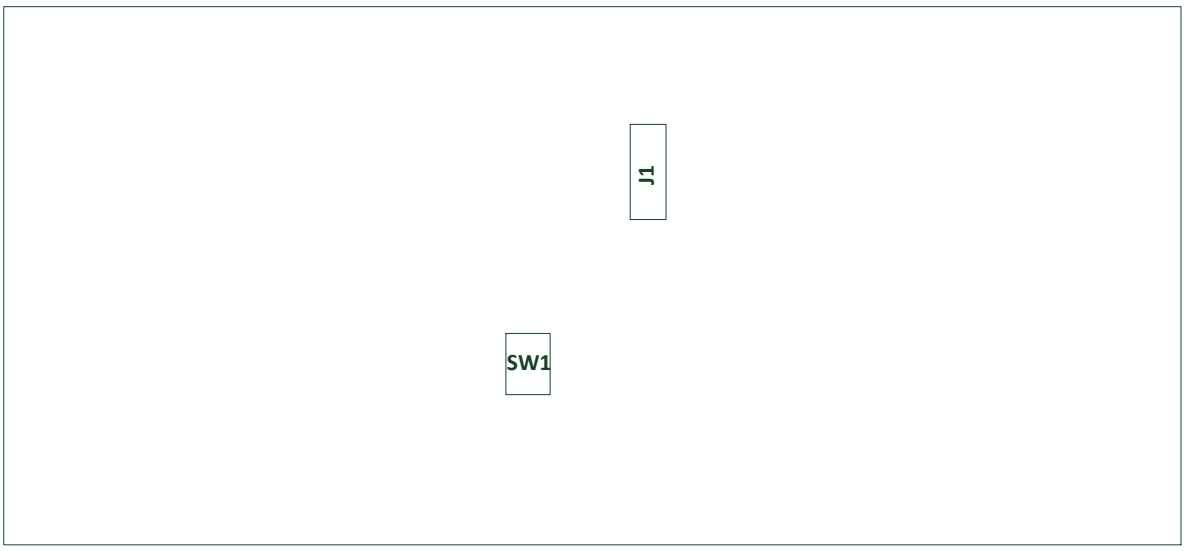
4 Hardware

4.1 Connectors PCIe-Option

Figure 5: NXMC-4E1 – PCIe-Option – Connector Location – Overview



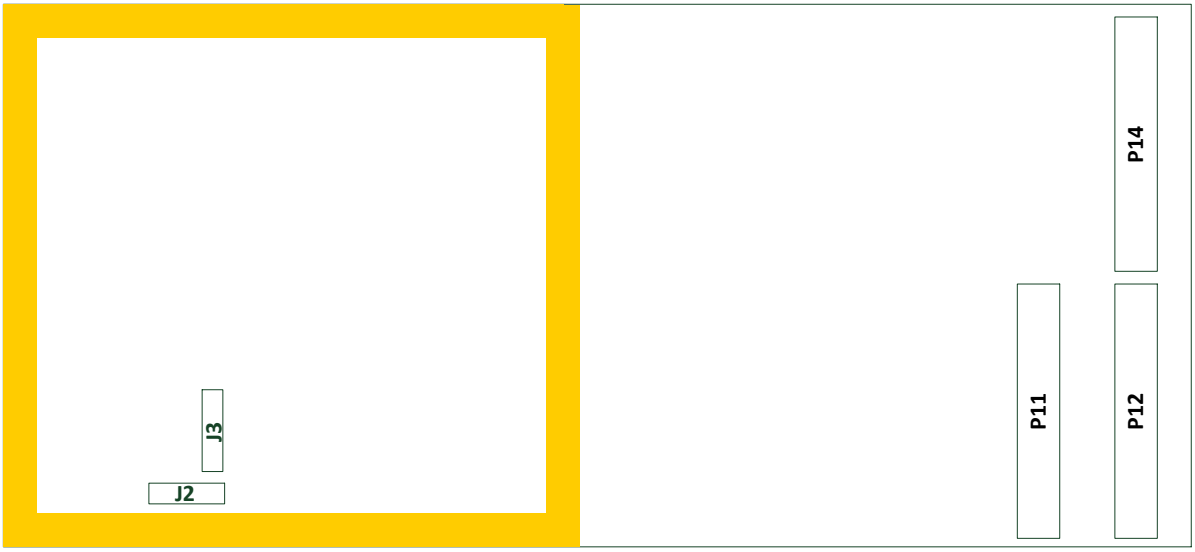
Top View



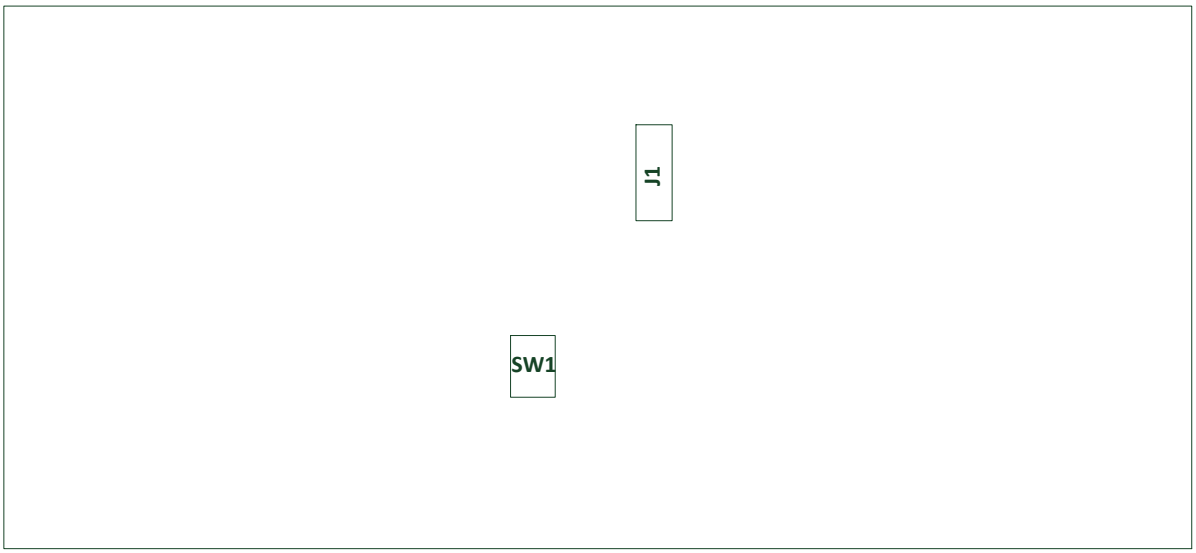
Bottom View

4.2 Connectors PCI-Option

Figure 6: NXMC-4E1 – PCI-Option – Connector Location – Overview



Top View



Bottom View

Please refer to the following tables to look up the connector pin assignment of the **NXMC-4E1**.

4.3 Connector Pin Assignments

4.3.1 J1 – JTAG Programming Header

Connector J1 serves as JTAG programming-port.

Table 2: J1 – JTAG Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	+3.3V	2
3	HDR_TDI	HDR_TDO	4
5	HDR_TMS	HDR_TCK	6

4.3.2 J2 – Serial Interface

A serial interface is provided by J2.

Table 3: J2 – Serial Interface – Pin Assignment

Pin #	Signal	Signal	Pin #
1	UART_TX	UART_RX	2
3	GND	-	-

4.3.3 J3 – I^2C-Debug Interface

J3 serves as I^2C-Debug interface.

Table 4: J3 – I^2C-Debug Interface – Pin Assignment

Pin #	Signal	Signal	Pin #
1	XMC_SDA_BUF	XMC_SCL_BUF	2
3	GND	-	-

4.3.4 P11 – PMC Connector – Pin Assignment

Table 5: P11 – PMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	JTAG_TCK	nc	2
3	GND	/INTA	4
5	/INTB	/INTC	6
7	GND	PWR_IN_12V_5V	8
9	/INTD	nc	10
11	GND	nc	12
13	PCI_CLK_PMC	GND	14
15	GND	/PMC_GNT	16
17	/PMC_REQ	PWR_IN_12V_5V	18

Pin #	Signal	Signal	Pin #
19	+3.3V_PMC	PCI_AD31	20
21	PCI_AD28	PCI_AD27	22
23	PCI_AD25	GND	24
25	GND	/CBE3	26
27	PCI_AD22	PCI_AD21	28
29	PCI_AD19	PWR_IN_12V_5V	30
31	+3.3V_PMC	PCI_AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	PWR_IN_12V_5V	38
39	GND	/LOCK	40
41	nc	nc	42
43	PAR	GND	44
45	+3.3V_PMC	PCI_AD15	46
47	PCI_AD12	PCI_AD11	48
49	PCI_AD9	PWR_IN_12V_5V	50
51	GND	/CBE0	52
53	PCI_AD6	PCI_AD5	54
55	PCI_AD4	GND	56
57	+3.3V_PMC	PCI_AD3	58
59	PCI_AD2	PCI_AD1	60
61	PCI_AD0	PWR_IN_12V_5V	62
63	GND	/REQ64	64

4.3.5 P12 – PMC Connector – Pin Assignment

Table 6: P12 – PMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	+12V_PMC	nc	2
3	JTAG_TMS	JTAG_TDO	4
5	JTAG_TDI	GND	6
7	GND	nc	8
9	nc	nc	10
11	PMC_BS_MD2	+3.3V_PMC	12
13	/PCI_RST	PMC_BS_MD3	14
15	+3.3V_PMC	PMC_BS_MD4	16
17	/PME	GND	18
19	PCI_AD30	PCI_AD29	20
21	GND	PCI_AD26	22
23	PCI_AD24	+3.3V_PMC	24
25	/IDSEL	PCI_AD23	26
27	+3.3V_PMC	PCI_AD20	28
29	PCI_AD18	GND	30
31	PCI_AD16	/CBE2	32
33	GND	IDSELB	34
35	/TRDY	+3.3V_PMC	36
37	GND	/STOP	38

Pin #	Signal	Signal	Pin #
39	/PERR	GND	40
41	+3.3V_PMC	/SERR	42
43	/CBE1	GND	44
45	PCI_AD14	PCI_AD13	46
47	M66EN	PCI_AD10	48
49	PCI_AD8	+3.3V_PMC	50
51	PCI_AD7	/REQB	52
53	+3.3V_PMC	/GNTB	54
55	nc	GND	56
57	nc	EREADY	58
59	GND	/RESETOUT	60
61	/ACK64	+3.3V_PMC	62
63	GND	/MONARCH	64

4.3.6 P14 – PMC Connector – Pin Assignment

Table 7: P14 – PMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	TX1_S_P	nc	2
3	TX1_S_N	nc	4
5	nc	nc	6
7	nc	nc	8
9	RX1_S_P	nc	10
11	RX1_S_N	nc	12
13	nc	nc	14
15	nc	nc	16
17	TX2_S_P	nc	18
19	TX2_S_N	nc	20
21	nc	nc	22
23	nc	nc	24
25	RX2_S_P	nc	26
27	RX2_S_N	nc	28
29	nc	nc	30
31	nc	nc	32
33	nc	nc	34
35	nc	nc	36
37	RX3_S_P	nc	38
39	RX3_S_N	nc	40
41	nc	nc	42
43	nc	nc	44
45	TX3_S_P	nc	46
47	TX3_S_N	nc	48
49	nc	nc	50
51	nc	nc	52
53	RX4_S_P	nc	54
55	RX4_S_N	nc	56
57	nc	nc	58

Pin #	Signal	Signal	Pin #
59	nc	nc	60
61	TX4_S_P	nc	62
63	TX4_S_N	nc	64

4.3.7 P15 – XMC Connector – Pin Assignment

Table 8: P15 – XMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	PET0_P	GND	A2
A3	nc	GND	A4
A5	nc	GND	A6
A7	nc	GND	A8
A9	nc	GND	A10
A11	PER0_P	GND	A12
A13	nc	GND	A14
A15	nc	GND	A16
A17	nc	GND	A18
A19	XMC_REFCLK_P	-	-
B1	PET0_N	GND	B2
B3	nc	GND	B4
B5	nc	GND	B6
B7	nc	GND	B8
B9	nc	GND	B10
B11	PER0_n	GND	B12
B13	nc	GND	B14
B15	nc	GND	B16
B17	nc	GND	B18
B19	XMC_REFCLK_N	-	-
C1	XMC_3.3V	nc	C2
C3	XMC_3.3V	JTAG_TCK	C4
C5	XMC_3.3V	JTAG_TMS	C6
C7	XMC_3.3V	JTAG_TDI	C8
C9	nc	JTAG_TDO	C10
C11	XMC_MBIST#	XMC_GA1	C12
C13	nc	XMC_GA2	C14
C15	nc	XMC_MVMRO	C16
C17	nc	nc	C18
C19	nc	-	-
D1	nc	GND	D2
D3	nc	GND	D4
D5	nc	GND	D6
D7	nc	GND	D8
D9	nc	GND	D10
D11	nc	GND	D12
D13	nc	GND	D14
D15	nc	GND	D16
D17	nc	GND	D18

Pin #	Signal	Signal	Pin #
D19	XMC_WAKE#	-	-
E1	nc	GND	E2
E3	nc	GND	E4
E5	nc	GND	E6
E7	nc	GND	E8
E9	nc	GND	E10
E11	nc	GND	E12
E13	nc	GND	E14
E15	nc	GND	E16
E17	nc	GND	E18
E19	nc	-	-
F1	PWR_IN_12V_5V	XMC_MRSTI#	F2
F3	PWR_IN_12V_5V	XMC_MRSTO#	F4
F5	PWR_IN_12V_5V	XMC_12V+	F6
F7	PWR_IN_12V_5V	nc	F8
F9	PWR_IN_12V_5V	XMC_GA0	F10
F11	PWR_IN_12V_5V	GND	F12
F13	PWR_IN_12V_5V	XMC_SDA	F14
F15	PWR_IN_12V_5V	XMC_SCL	F16
F17	nc	nc	F18
F19	nc	-	-

4.3.8 P16 – XMC Connector – Pin Assignment

Table 9: P16 – XMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	TX1_P	nc	A2
A3	nc	nc	A4
A5	nc	nc	A6
A7	TX2_P	nc	A8
A9	nc	nc	A10
A11	nc	nc	A12
A13	TX3_P	nc	A14
A15	nc	nc	A16
A17	nc	nc	A18
A19	TX4_P	-	-
B1	TX1_N	nc	B2
B3	nc	nc	B4
B5	nc	nc	B6
B7	TX2_N	nc	B8
B9	nc	nc	B10
B11	nc	nc	B12
B13	TX3_N	nc	B14
B15	nc	nc	B16
B17	nc	nc	B18
B19	TX4_N	-	-
C1	nc	nc	C2

Pin #	Signal	Signal	Pin #
C3	nc	nc	C4
C5	nc	nc	C6
C7	nc	nc	C8
C9	nc	nc	C10
C11	nc	nc	C12
C13	nc	nc	C14
C15	nc	nc	C16
C17	nc	nc	C18
C19	nc	-	-
D1	RX1_P	nc	D2
D3	nc	nc	D4
D5	nc	nc	D6
D7	RX2_P	nc	D8
D9	nc	nc	D10
D11	nc	nc	D12
D13	RX3_P	nc	D14
D15	nc	nc	D16
D17	nc	nc	D18
D19	RX4_P	-	-
E1	RX1_N	nc	E2
E3	nc	nc	E4
E5	nc	nc	E6
E7	RX2_N	nc	E8
E9	nc	nc	E10
E11	nc	nc	E12
E13	RX3_N	nc	E14
E15	nc	nc	E16
E17	nc	nc	E18
E19	RX4_N	-	-
F1	nc	nc	F2
F3	nc	nc	F4
F5	nc	nc	F6
F7	nc	nc	F8
F9	nc	nc	F10
F11	nc	nc	F12
F13	nc	nc	F14
F15	nc	nc	F16
F17	nc	nc	F18
F19	nc	-	-

4.3.9 SW1 – JTAG Select

The table below gives an overview of the operating parameters configurable via SW1. Details are given in the following subchapters.

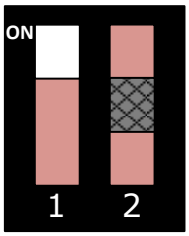
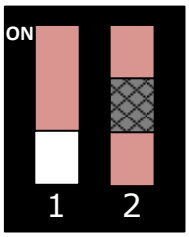
Table 10: SW1 – Pin-Assignment – Overview

Switch #	Function
1	JTAG Select
2	E1 line-to-line loopback enable

4.3.9.1 SW1 – Switch 1 – JTAG Select

By operating switch1 of SW1 the JTAG Mode can be selected according to the following table.

Table 11: SW1 – Switch 1 – JTAG Mode Select

SW1 – Switch 1	Function
	Select onboard JTAG-Header
	Select XMC/PMC connector JTAG

Default:
Switch 1 of SW1 is toggled to OFF, XMC/PMC connector JTAG is selected.

4.3.9.2 SW1 – Switch 2 – E1-Loopback

By operating switch2 of SW1 a loopback a loopback from line to line can be enabled. Here the incoming E1 data normally passes the framer towards FPGA, and is then looped-back in the FPGA towards framer again instead of sending data coming from the host.

5 NXMC-4E1 Programming Notes

The FPGA on the **NXMC-4E1** implements various logical blocks. The table below shows the memory map for the logical sub-blocks of the design. Refer to the following sub-chapters for detailed information.
All devices shown in this memory map can be accessed via PCI/PCIe.

Table 12: FPGA Memory Map

Address Offset	Logical Block
0x0000000	General Purpose Status (Read Only)
0x0000100	General Purpose Registers (Read/Write)
0x0002000	DMA Engine
0x0004000	SPI FLASH ENGINE
0x0008000	FRAMER ACCESS

Table 13: FPGA Register Description – Overview

General Purpose – Read Only – 16 bit	
0x0000000	VENDOR_ID
0x0000002	BOARD_ID
0x0000004	MAGIC_VAL_1
0x0000006	SERIAL_NO
0x0000008	PCB_VERSION
0x000000A	FPGA_VERSION
0x000000C	PLL_STATUS
0x000000E	tbd
General Purpose – Read/Write – 16 bit	
0x0000100	RESET
0x0000102	tbd
0x0000104	CLOCK_CNTRL
0x0000106	tbd
0x000010A	tbd
0x000010C	tbd
0x000010E	tbd
DMA Engine – 16 bit	
0x0002000	drop_dma_base_ptr_h
0x0002002	drop_dma_base_ptr_l
0x0002004	drop_dma_enable
0x0002006	drop_dma_blk_num
0x0002008	drop_dma_blk_size
0x000200A	drop_dma_blk_dist
0x000200C	drop_dbg_mode
0x000200E	irq_interval
0x0002010	drop_fnd_val_cnt
0x0002012	drop_disc_fr_cnt
0x0002014	drop_cur_blk_num
0x0002016	drop_last_hd
0x0002018	tbd
0x000201A	tbd
0x000201C	tbd
0x000201E	tbd

DMA Engine – 16 bit	
0x0002020	add_dma_base_ptr_h
0x0002022	add_dma_base_ptr_l
0x0002024	add_dma_enable
0x0002026	add_dma_blk_num
0x0002028	add_dma_blk_size
0x000202A	add_dma_blk_dist
0x000202C	add_dbg_mode
0x000202E	tbd
0x0002030	add_fnd_inval_cnt
0x0002032	add_disc_fr_cnt
0x0002034	add_cur_blk_num
0x0002036	add_last_hd
0x0002038	add_cur_hd_addr_h
0x000203A	add_cur_hd_addr_l
0x000203C	last_state_at_fs
0x000203E	tbd
SPI FLASH ENGINE	
0x0004000	SPI FLASH ENGINE
FRAMER ACCESS	
0x0008000	FRAMER ACCESS

5.1 General Purpose – Read Only

5.1.1 0x0000000 – VENDOR_ID

Bit	Name	Description	Default	Access
15..0	VENDOR_ID	holds Vendor-ID	0x1A16	Read Only

5.1.2 0x0000002 – BOARD_ID

This read-only register can be used by the device driver to probe register access. It holds the N.A.T. internal board-ID of the **NXMC-4E1.**

Bit	Name	Description	Default	Access
15..0	BOARD_ID	holds internal Board-ID	0x1301	Read Only

5.1.3 0x0000004 – MAGIC_VAL_1

This read-only register can be used by the device driver to probe register access.

Bit	Name	Description	Default	Access
15..0	MAGIC_VAL_1	Testing purposes	0xAA55	Read Only

5.1.4 0x0000006 – SERIAL_NO

Bit	Name	Description	Default	Access
15..8	auto_rd_bytes(1)	holds serial number read from SPI FLASH	na	Read Only
7..0	auto_rd_bytes(0)	holds serial number read from SPI FLASH	na	Read Only

5.1.5 0x0000008 – PCB_VERSION

Bit	Name	Description	Default	Access
15..8	FUNC_TYPE	tbd	0x0000	Read Only
7..0	PCB_VERSION	holds PCB-Version	0x0010	Read Only

5.1.6 0x000000A – FPGA_VERSION

Bit	Name	Description	Default	Access
15..8	FPGA_VERSION	holds FPGA-Version	0x0010	Read Only
7..0	DEVEL_VERSION	holds Development-Version	na	Read Only

5.1.7 0x000000C – PLL_STAT

Bit	Name	Description	Default	Access
15..4	tbd	tbd	na	Read Only
3	pll_cs_ca	in automatic reference selection mode a '1' indicates input 2 is used	na	Read Only
2	pll_los2	a '1' indicates PLL loss-of-signal for input 2	na	Read Only
1	pll_los1	a '1' indicates PLL loss-of-signal for input 1	na	Read Only
0	pll_lol	a '1' indicates PLL loss-of-lock	na	Read Only

5.2 General Purpose – Read/Write

5.2.1 0x0000100 – RESET

This register is used to trigger a reset to the whole FPGA logic, FPGA blocks or external devices. Writing a '1' to a bit triggers the reset. The device specific bits are not self resetting and must be written to '0' again for normal operation.

Bit	Name	Description	Default	Access
15..3	tbd	tbd	0	Read/Write
2	PLL	PLL reset	0	Read/Write
1	FR	E1 Framer reset	0	Read/Write
0	ALL	complete board reset	0	Read/Write

5.2.2 0x0000104 – CLOCK_CNTR

Bit	Name	Description	Default	Access
15..13	tbd	tbd	0	Read/Write
12	refclkio_oe	a '1' enables the framer REFCLKIO signal	0	Read/Write
11	tbd	tbd	0	Read/Write
10..8	pll_ref2_sel	see table below	na	Read/Write
7	tbd	tbd	0	Read/Write
6..4	pll_ref1_sel	see table below	na	Read/Write
3	txdis	a '1' disables the E1 framer Tx	0	Read/Write
2	pll_cs_ca	a '1' enables PLL revertive autoswitching mode	0	Read/Write
1	pll_autosel	a '1' enables PLL autoswitching	0	Read/Write
0	en_tdm_lb	a '1' enables E1 loopback from line to line	0	Read/Write

pll_refx_sel_values	
0x0	free-running local oscillator
0x1	LIF 0
0x2	LIF 1
0x3	LIF 2
0x4	LIF 3
others	constant low

5.3 DMA Engine – Read/Write

5.3.1 0x0002000 – DROP_DMA_BASE_PTR_H

Bit	Name	Description	Default	Access
15..0	drop_dma_base_ptr_h	tbd	na	Read/Write

5.3.2 0x0002002 – DROP_DMA_BASE_PTR_L

Bit	Name	Description	Default	Access
15..0	drop_dma_base_ptr_l	tbd	na	Read/Write

5.3.3 0x0002004 – DROP_DMA_ENABLE

Bit	Name	Description	Default	Access
15..1	tbd	tbd	na	Read/Write
0	en	tbd	na	Read/Write

5.3.4 0x0002006 – DROP_DMA_BLK_NUM

Bit	Name	Description	Default	Access
15..0	drop_dma_blk_num	tbd	na	Read/Write

5.3.5 0x0002008 – DROP_DMA_BLK_SIZE

Bit	Name	Description	Default	Access
15..0	drop_dma_blk_size	tbd	na	Read/Write

5.3.6 0x000200A – DROP_DMA_BLK_DIST

Bit	Name	Description	Default	Access

15..0	drop_dma_blk_dist	tbd	na	Read/Write

5.3.7 0x000200C – DROP_DBG_MODE

Bit	Name	Description	Default	Access
15..5	tbd	tbd	na	Read/Write
4	drop_chk_dis	tbd	na	Read/Write
3..0	drop_dbg_mode	tbd	na	Read/Write

5.3.8 0x000200E – IRQ_INTERVAL

Bit	Name	Description	Default	Access
15..8	tbd	tbd	na	Read/Write
7..0	irq_interval	tbd	na	Read/Write

5.3.9 0x0002010 – DROP_FND_VAL_CNT

Bit	Name	Description	Default	Access
15..0	drop_fnd_val_cnt	tbd	na	Read/Write

5.3.10 0x0002012 – DROP_DISC_FR_CNT

Bit	Name	Description	Default	Access
15..0	drop_disc_fr_cnt	tbd	na	Read/Write

5.3.11 0x0002014 – DROP_CUR_BLK_NUM

Bit	Name	Description	Default	Access
15..0	drop_cur_blk_num	tbd	na	Read/Write

5.3.12 0x0002016 – DROP_LAST_HD

Bit	Name	Description	Default	Access

15..0	drop_last_hd	tbd	na	Read/Write

5.3.13 0x0002020 – ADD_DMA_BASE_PTR_H

Bit	Name	Description	Default	Access
15..0	add_dma_base_ptr_h	tbd	na	Read/Write

5.3.14 0x0002022 – ADD_DMA_BASE_PTR_L

Bit	Name	Description	Default	Access
15..0	add_dma_base_ptr_l	tbd	na	Read/Write

5.3.15 0x0002024 – ADD_DMA_ENABLE

Bit	Name	Description	Default	Access
15..1	tbd	tbd	na	Read/Write
0	en	tbd	na	Read/Write

5.3.16 0x0002026 – ADD_DMA_BLK_NUM

Bit	Name	Description	Default	Access
15..0	add_dma_blk_num	tbd	na	Read/Write

5.3.17 0x0002028 – ADD_DMA_BLK_SIZE

Bit	Name	Description	Default	Access
15..0	add_dma_blk_size	tbd	na	Read/Write

5.3.18 0x000202A – ADD_DMA_BLK_DIST

Bit	Name	Description	Default	Access
15..0	add_dma_blk_dist	tbd	na	Read/Write

5.3.19 0x000202C – ADD_DBG_MODE

Bit	Name	Description	Default	Access
15..8	read_burst_len	tbd	na	Read/Write
7..5	tbd	tbd	na	Read/Write
4	use_read_multiple	tbd	na	Read/Write
3..0	add_dbg_mode	tbd	na	Read/Write

5.3.20 0x0002030 – ADD_FND_INVAL_CNT

Bit	Name	Description	Default	Access
15..0	add_fnd_inval_cnt	tbd	na	Read/Write

5.3.21 0x0002032 – ADD_DISC_FR_CNT

Bit	Name	Description	Default	Access
15..0	add_disc_fr_cnt	tbd	na	Read/Write

5.3.22 0x0002034 – ADD_CUR_BLK_NUM

Bit	Name	Description	Default	Access
15..0	add_cur_blk_num	tbd	na	Read/Write

5.3.23 0x0002036 – ADD_LAST_HD

Bit	Name	Description	Default	Access
15..0	add_last_hd	tbd	na	Read/Write

5.3.24 0x0002038 – ADD_CUR_HD_ADDR_H

Bit	Name	Description	Default	Access
15..0	add_cur_hd_addr_h	tbd	na	Read/Write

5.3.25 0x000203A – ADD_CUR_HD_ADDR_L

Bit	Name	Description	Default	Access
15..0	add_cur_hd_addr_l	tbd	na	Read/Write

5.3.26 0x000203C – LAST_STATE_AT_FS

Bit	Name	Description	Default	Access
15..0	last_state_at_fs	tbd	na	Read/Write

5.4 SPI FLASH ENGINE

A logic unit that offers access to the FPGA SPI Flash configuration memory can be accesses via byte-wide read or write accesses at offset 0x2000.

5.5 FRAMER ACCESS

The framer registers can be accessed at offset 0x8000 using byte-wide read or write accesses. Please refer to the DS25518 manual for further information here.

6 Board Specification

Table 14: NXMC-4E1 Features - Overview

FPGA	XILINX Spartan 7 XC7S50
XMC-Module	Switch Mezzanine Card (XMC)
Power Consumption	12V / 0.5A max
Operating Temperature	-40°C – +85°C with conduction cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	ANSI/VITA 42.0 – 2016 ANSI/VITA 42.3 – 2006 (R2014)

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NXMC-4E1** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NXMC-4E1** read this installation section
- Before installing or uninstalling the **NXMC-4E1**, read the Installation Guide and the User's Manual of the carrier board used.
- Before installing or uninstalling the **NXMC-4E1** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NXMC-4E1** is connected to the carrier board with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires only
- An XMC carrier board for installing the **NXMC-4E1**
- power supply

7.2.2 Power supply

The power supply for the **NXMC-4E1** must meet the following specifications:
- required for the module:
  - +12V / 0.5A max.
  - + 3,3V / 0.15A max.

7.2.3 Automatic Power Up

In the following situations the **NXMC-4E1**will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCI(e) Reset.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Xilinx Spartan-7 XC7S50 – DS189 (v1.4) – 12/2017
[2] Maxim/Dallas DS26518 8-Port T1/E1/J1 Transceiver – DS Rev: 103008 – 10/2008
[3] PLX PEX8112 PCIe-to-PCI Bridge – Databook V1.2 10/2008

Appendix B: Document's History

Revision	Date	Description	Author
1.0	7.03.2018	initial release	se
1.1	16.05.2018	Added pdf content marks	te