NPCIe-XMC-4E1
PCIe Carrier Module
Technical Reference Manual V1.1
HW Revision 1.x

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*. Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
E1	PDH signal – data rate 2.048 Mbit/s
FPGA	Field Programmable Gate Array
I²C	Inter-Integrated Circuit
LED	Light Emitting Diode
PCI(e)	Peripheral Component Interconnect (Express)
USB	Universal Serial Bus
XMC	Switch Mezzanine Card

1 Introduction

The **NPCIe-XMC-4E1** is a carrier board used to operate an XMC mezzanine card (especially **NXMC-4E1**) in a standard PC with PCI Express extension slots. The **NPCIe-XMC-4E1** owns four RJ45 connectors which provide the XMC's E1 interfaces to the face plate and an optional available Micro-USB-Port which enables programming a Xilinx-FPGA located on the XMC. For further information regarding the programming process, please refer to chapter 3 Software.

The LEDs featured by the RJ45 connectors can by controlled by an I²C-Buffer (assembly option) via I²C from the mezzanine.

The following figures show photos of the **NPCIe-XMC-4E1.**

Figure 1: NPCIe-XMC-4E1 Carrier

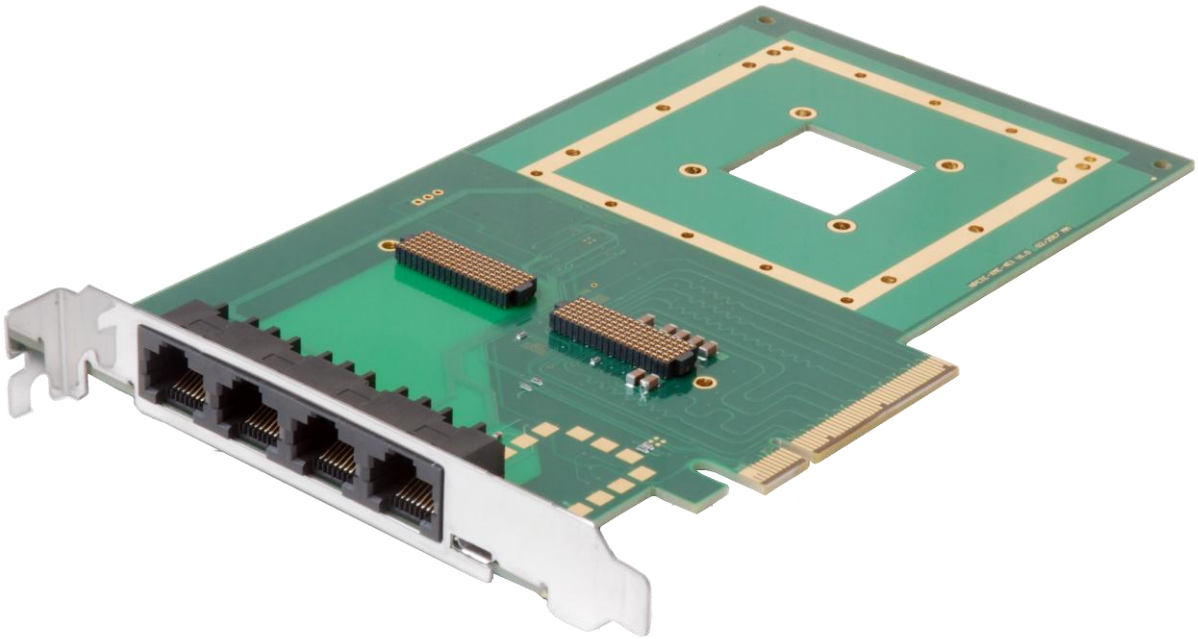
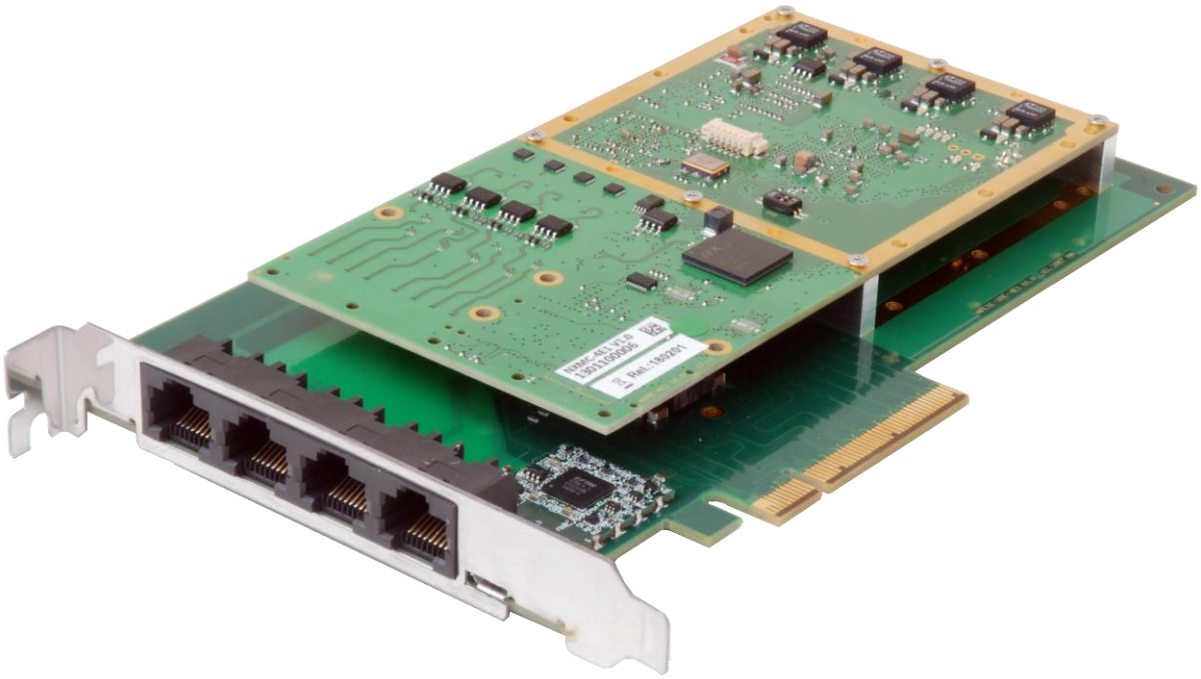


Figure 2: NPCIe-XMC-4E1 Carrier with XMC attached

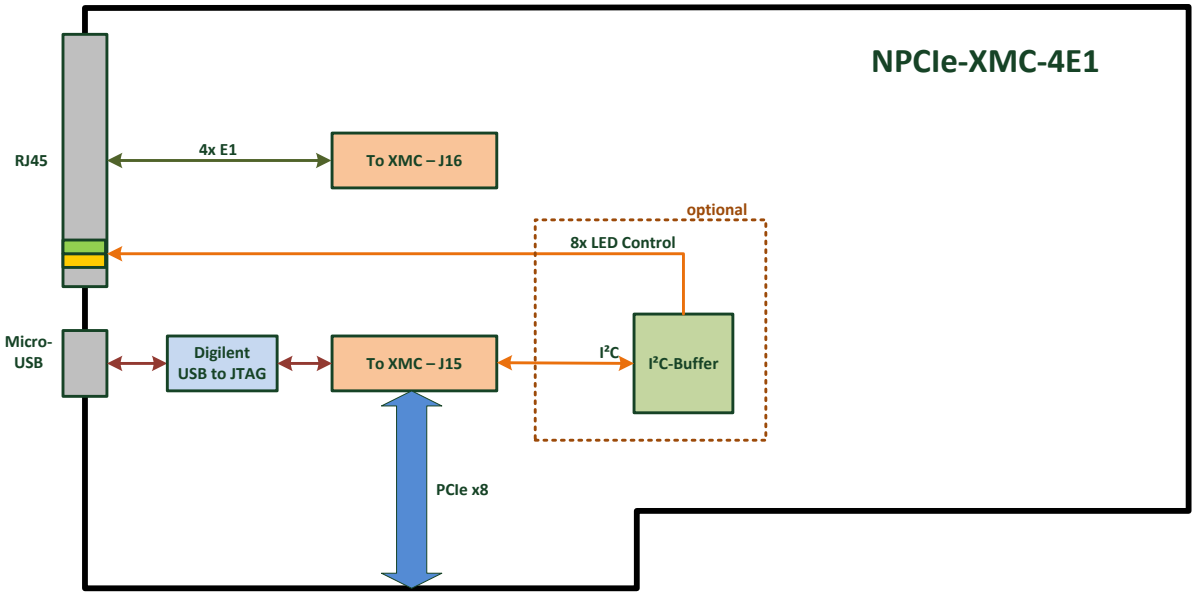


2 Hardware

2.1 Block Diagram

The following figure shows a detailed block diagram of the **NPCIe-XMC-4E1**.

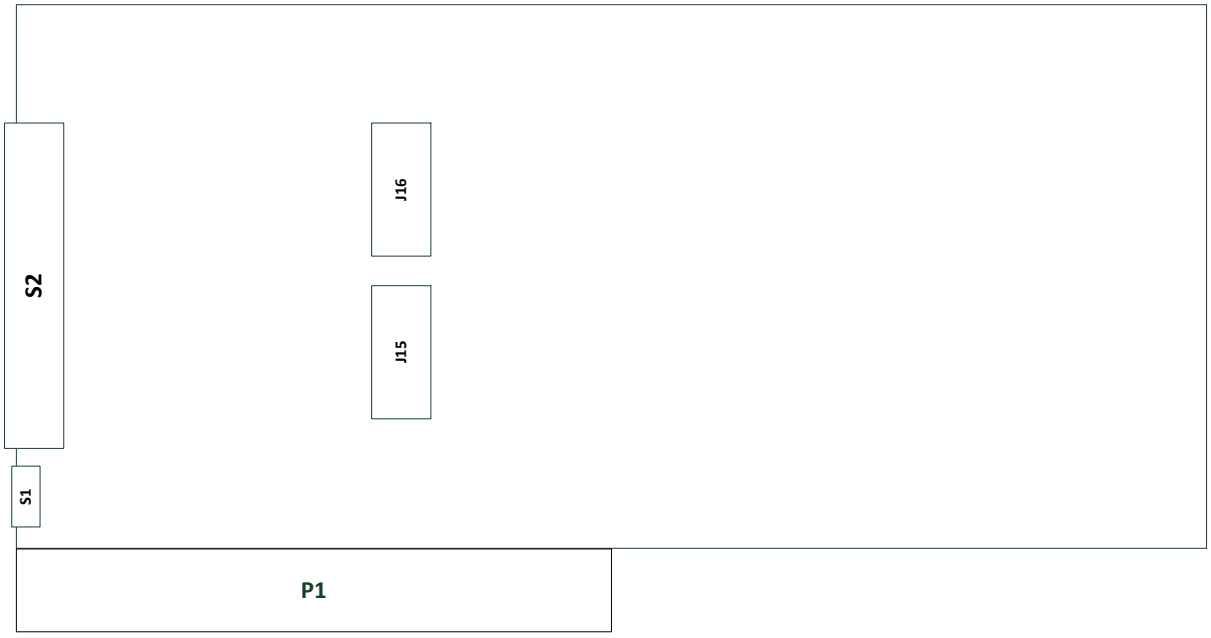
Figure 3: NPCIe-XMC-4E1 – Block Diagram



2.2 Connectors and Switches

The following figure shows a detailed connector and switch diagram of the **NPCIe-XMC-4E1**.

Figure 4: NPCIe-XMC-4E1 – Connector and Switch Location – Overview



Top View

Please refer to the following tables to look up the connector pin assignment of the **NPCIe-XMC-4E1**.

2.2.1 P1 – PCIe Connector

Table 2: P1 – PCIe Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
A1	PCIE_AUX.MPRESENT#	+12V	B1
A2	+12V	+12V	B2
A3	+12V	+12V	B3
A4	GND	GND	B4
A5	PCIE_AUX.TCK	PCIE_AUX.SCL	B5
A6	PCIE_AUX.TDI	PCIE_AUX.SDA	B6
A7	PCIE_AUX.TDO	GND	B7
A8	PCIE_AUX.TMS	+3V3	B8
A9	+3V3	PCIE_AUX.TRST#	B9
A10	+3V3	nc	B10
A11	PCIE_AUX.MRSTI#	PCIE_AUX.WAKE#	B11
A12	GND	nc	B12
A13	PCIE_AUX.CLK_P	GND	B13
A14	PCIE_AUX.CLK_N	PCIE.RX0_P	B14
A15	GND	PCIE.RX0_N	B15
A16	PCIE.TX0_P	GND	B16
A17	PCIE.TX0_N	nc	B17
A18	GND	GND	B18
A19	nc	PCIE.RX1_P	B19
A20	GND	PCIE.RX1_N	B20
A21	PCIE.TX1_P	GND	B21
A22	PCIE.TX1_N	GND	B22
A23	GDN	PCIE.RX2_P	B23
A24	GND	PCIE.RX2_N	B24
A25	PCIE.TX2_P	GND	B25
A26	PCIE.TX2_N	GND	B26
A27	GND	PCIE.RX3_P	B27
A28	GND	PCIE.RX3_N	B28
A29	PCIE.TX3_P	GND	B29
A30	PCIE.TX3_N	nc	B30
A31	GND	nc	B31
A32	nc	GND	B32
A33	nc	PCIE.RX4_P	B33
A34	GND	PCIE.RX4_N	B34
A35	PCIE.TX4_P	GND	B35
A36	PCIE.TX4_N	GND	B36
A37	GND	PCIE.RX5_P	B37
A38	GND	PCIE.RX5_N	B38
A39	PCIE.TX5_P	GND	B39
A40	PCIE.TX5_N	GND	B40
A41	GND	PCIE.RX6_P	B41
A42	GND	PCIE.RX6_N	B42
A43	PCIE.TX6_P	GND	B43

Pin #	Signal	Signal	Pin #
A44	PCIE.TX6_N	GND	B44
A45	GND	PCIE.RX7_P	B45
A46	GND	PCIE.RX7_N	B46
A47	PCIE.TX7_P	GND	B47
A48	PCIE.TX7_N	PCIE_AUX.MPRESENT#	B48
A49	GND	GND	B49

2.2.2 J15 – XMC Connector – Pin Assignment

Table 3: J15 – XMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	PCIE.TX0_P	GND	A2
A3	PCIE.TX2_P	GND	A4
A5	PCIE.TX4_P	GND	A6
A7	PCIE.TX6_P	GND	A8
A9	nc	GND	A10
A11	PCIE.RX0_P	GND	A12
A13	PCIE.RX2_P	GND	A14
A15	PCIE.RX4_P	GND	A16
A17	PCIE.RX6_P	GND	A18
A19	XMC_AUX.CLK_P	-	-
B1	PCIE.TX0_N	GND	B2
B3	PCIE-TX2_N	GND	B4
B5	PCIE.TX4_N	GND	B6
B7	PCIE.TX6_N	GND	B8
B9	nc	GND	B10
B11	PCIE.RX0_N	GND	B12
B13	PCIE.RX2_N	GND	B14
B15	PCIE.RX4_N	GND	B16
B17	PCIE.RX6_N	GND	B18
B19	XMC_AUX.CLK_N	-	-
C1	+3.3V	XMC_ TRST#	C2
C3	+3.3V	XMC_TCK	C4
C5	+3.3V	XMC_ TMS	C6
C7	+3.3V	XMC_ TDI	C8
C9	nc	XMC_ TDO	C10
C11	nc	+3V3	C12
C13	+3.3V	+3V3	C14
C15	nc	nc	C16
C17	nc	nc	C18
C19	nc	-	-
D1	PCIE.TX1_P	GND	D2
D3	PCIE-TX3_P	GND	D4
D5	PCIE.TX5_P	GND	D6
D7	PCIE.TX7_P	GND	D8

Pin #	Signal	Signal	Pin #
D9	nc	GND	D10
D11	PCIE.RX1_P	GND	D12
D13	PCIE.RX3_P	GND	D14
D15	PCIE.RX5_P	GND	D16
D17	PCIE.RX7_P	GND	D18
D19	XMC_AUX.WAKE#	-	-
E1	PCIE.TX1_N	GND	E2
E3	PCIE-TX3_N	GND	E4
E5	PCIE.TX5_N	GND	E6
E7	PCIE.TX7_N	GND	E8
E9	nc	GND	E10
E11	PCIE.RX1_N	GND	E12
E13	PCIE.RX3_N	GND	E14
E15	PCIE.RX5_N	GND	E16
E17	PCIE.RX7_N	GND	E18
E19	PCIE.ROOT0#	-	-
F1	+12V	PCIE_AUX.MRSTI#	F2
F3	+12V	nc	F4
F5	+12V	+12V	F6
F7	+12V	nc	F8
F9	+12V	+3V3	F10
F11	+12V	PCIE_AUX.MPRESENT#	F12
F13	+12V	XMC_SDA	F14
F15	+12V	XMC_ SCL	F16
F17	nc	nc	F18
F19	nc	-	-

2.2.3 J16 – XMC Connector – Pin Assignment

Table 4: J16 – XMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	TX1_S_P	nc	A2
A3	nc	nc	A4
A5	nc	nc	A6
A7	TX2_S_P	nc	A8
A9	nc	nc	A10
A11	nc	nc	A12
A13	TX3_S_P	nc	A14
A15	nc	nc	A16
A17	nc	nc	A18
A19	TX4_S_P	-	-
B1	TX1_S_N	nc	B2
B3	nc	nc	B4
B5	nc	nc	B6
B7	TX2_S_N	nc	B8

Pin #	Signal	Signal	Pin #
B9	nc	nc	B10
B11	nc	nc	B12
B13	TX3_S_N	nc	B14
B15	nc	nc	B16
B17	nc	nc	B18
B19	TX4_S_N	-	-
C1	nc	nc	C2
C3	nc	nc	C4
C5	nc	nc	C6
C7	nc	nc	C8
C9	nc	nc	C10
C11	nc	nc	C12
C13	nc	nc	C14
C15	nc	nc	C16
C17	nc	nc	C18
C19	nc	-	-
D1	RX1_S_P	nc	D2
D3	nc	nc	D4
D5	nc	nc	D6
D7	RX2_S_P	nc	D8
D9	nc	nc	D10
D11	nc	nc	D12
D13	RX3_S_P	nc	D14
D15	nc	nc	D16
D17	nc	nc	D18
D19	RX4_S_P	-	-
E1	RX1_S_N	nc	E2
E3	nc	nc	E4
E5	nc	nc	E6
E7	RX2_S_N	nc	E8
E9	nc	nc	E10
E11	nc	nc	E12
E13	RX3_S_N	nc	E14
E15	nc	nc	E16
E17	nc	nc	E18
E19	RX4_S_N	-	-
F1	nc	nc	F2
F3	nc	nc	F4
F5	nc	nc	F6
F7	nc	nc	F8
F9	nc	nc	F10
F11	nc	nc	F12
F13	nc	nc	F14
F15	nc	nc	F16
F17	nc	nc	F18
F19	nc	-	-

2.2.4 S1 – FPGA Programming Port

S1 offers a FPGA Programming Port for a Xilinx-FPGA located on the mezzanine board via USB-Connector towards the face plate.

Table 5: S1 – FPGA Programming Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC	D-	2
3	D+	ID	4
5	GND	GND	6
7	GND	GND	8
9	GND	GND	10
11	GND	-	-

2.2.5 S2 A-D – RJ45 Connectors

S2 A-D provide the E1 interfaces of the **NXMC-4E1** mezzanine board to the face plate.

Table 6: S2A – RJ45 Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX4_P	RX4_N	2
3	nc	TX4_P	4
5	TX4_N	nc	6
7	nc	nc	8

Table 7: S2B – RJ45 Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX3_P	RX3_N	2
3	nc	TX3_P	4
5	TX3_N	nc	6
7	nc	nc	8

Table 8: S2C – RJ45 Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX2_P	RX2_N	2
3	nc	TX2_P	4
5	TX2_N	nc	6
7	nc	nc	8

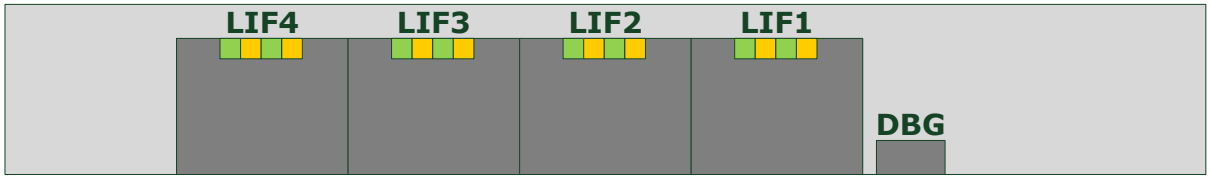
Table 9: S2D – RJ45 Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX1_P	RX1_N	2
3	nc	TX1_P	4
5	TX1_N	nc	6
7	nc	nc	8

2.3 Front Panel and LEDs

The **NPCIe-XMC-4E1** module is equipped with two bi-coloured LEDs (yellow/green) in each RJ45 connector reflecting the line interface status.

Figure 5: NPCIe-XMC-4E1 – Face Plate

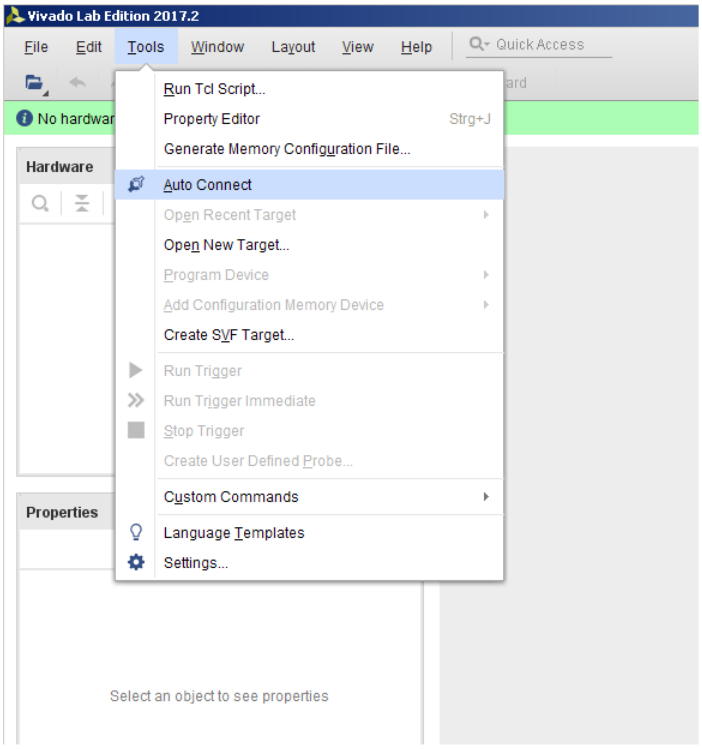


3 Software

For programming the FPGA-device located on the **NXMC-4E1** mezzanine card, Xilinx Vivado Lab Edition needs to be installed. The following steps must be performed:

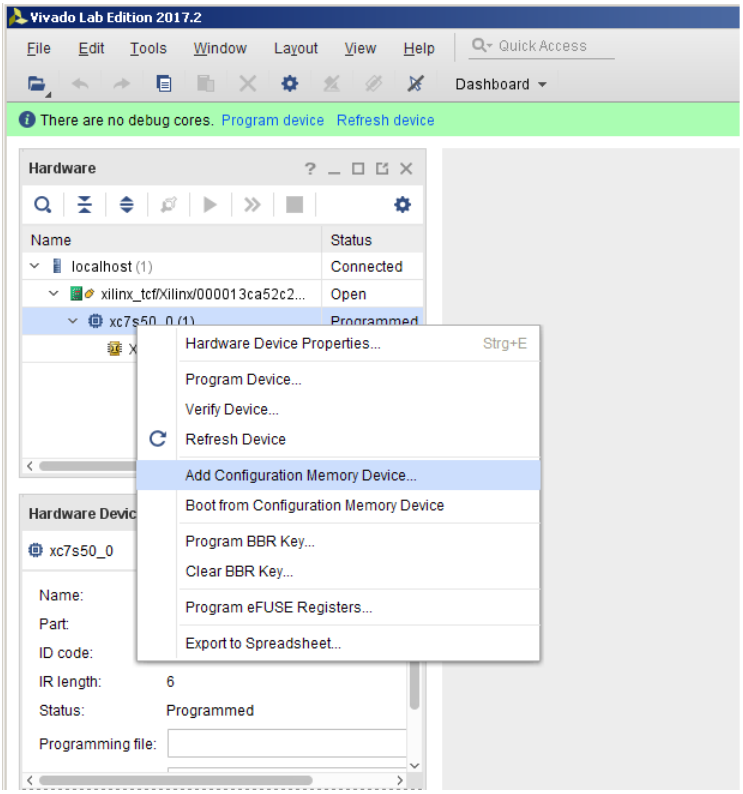
- Make sure that on the **NXMC-4E1** module both DIP-Switches are turned to OFF (to switch the FPGA-JTAG towards the XMC-Connector)
- Download and install Xilinx Vivado Lab Edition from https://www.xilinx.com/support/download.html
- Connect via standard micro-USB cable to the micro-USB jack of the **NPCIe-XMC-4E1** carrier
- Wait some seconds for the PC to install the appropriate driver
- Start the Xilinx Vivado Lab Edition tool
- Select "***Hardware Manager***"
- Select ***"Tools"*** -> ***"Auto Connect"***

Figure 6: NPCIe-XMC-4E1 – FPGA-Programming Step 1



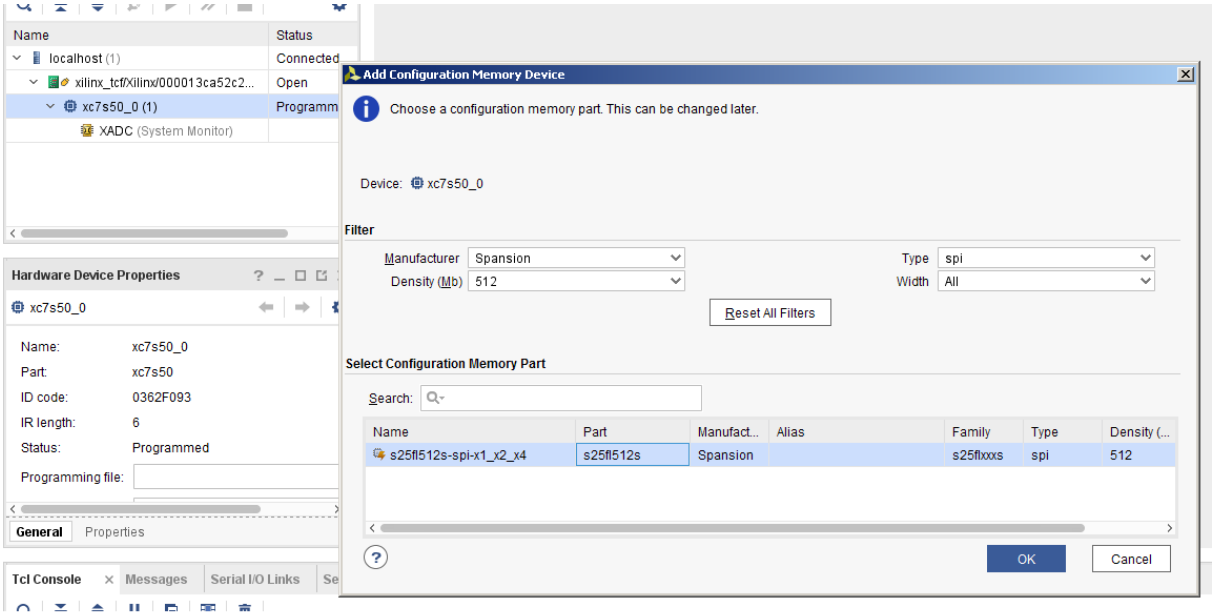
- The configuration device must be added (XC7S50 device connected to the JTAG tool); right-click on ***"XC7S50"*** and select ***"Add Configuration Memory Device"***

Figure 7: NPCIe-XMC-4E1 – FPGA-Programming Step 2



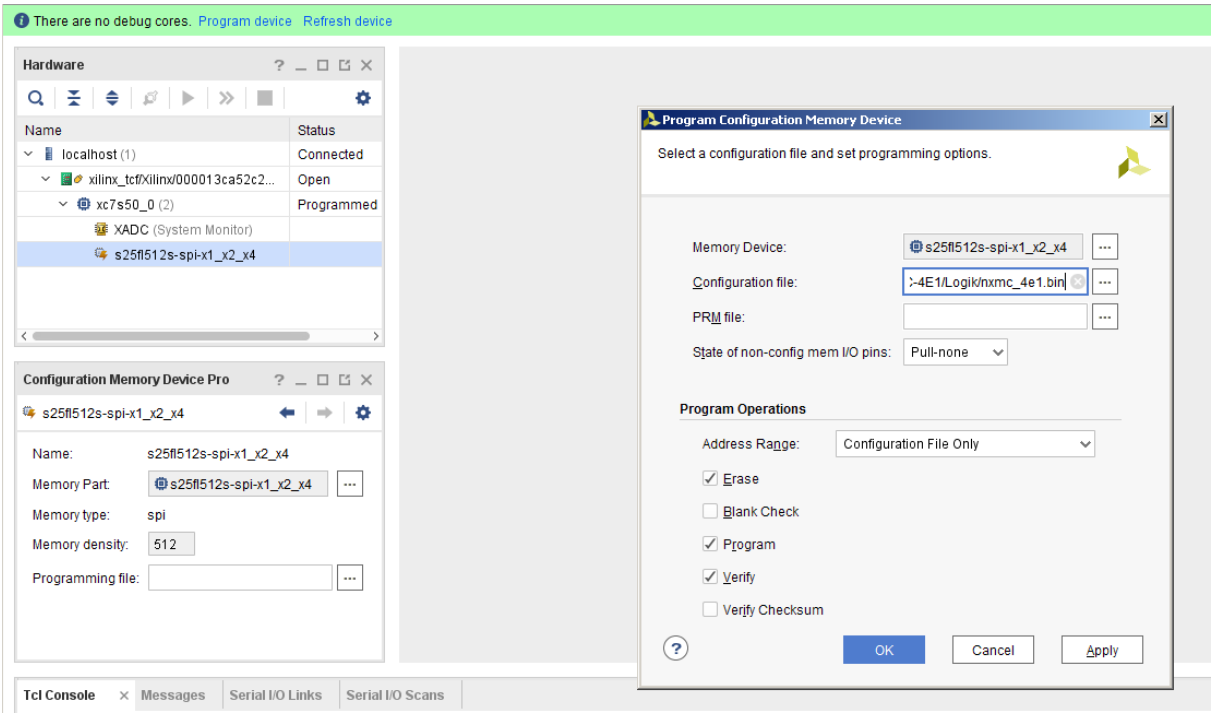
- Select the device ***"s25fl512s"*** as shown below

Figure 8: NPCIe-XMC-4E1 – FPGA-Programming Step 3



- Choose ***"Configuration File"*** -> ***"nxmc_4e1_1.0.14.bin"***

Figure 9: NPCIe-XMC-4E1 – FPGA-Programming Step 4



- By hitting the ***"OK button"***, programming starts and should take about one minute
- After a power cycle, the new FPGA image will be active

4 Board Specification

Table 10: NPCIe-XMC-4E1 Features – Overview

PCIe-Module	Standard height, half length PCI Express x8 add-in card
Front-I/O	4x RJ45 Micro-USB
Power Consumption	Depends on XMC
Operating Temperature	Depends on XMC
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh at +55°C (non-condensing)
Standards compliance	PCI Express Base Specification Rev. 1.1 PCI Express CEM Specification Rev. 2.0 CE, RoHS, EN61000, EN5022, EN55024

5 Installation

5.1 Safety Note

To ensure proper functioning of the **NPCIe-XMC-4E1** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NPCIe-XMC-4E1**read this installation section
- Before installing or uninstalling the **NPCIe-XMC-4E1**, read the Installation Guide and the User's Manual of the PC/Server main board used, or of the PCIe system the board will be plugged into.
- Before installing or uninstalling the **NPCIe-XMC-4E1** switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPCIe-XMC-4E1**is connected to the main board or to the PCIe backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

5.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

5.2.1 Requirements

The installation requires only
- an PCIe main board or a PCIe backplane for connecting the **NPCIe-XMC-4E1**

5.2.2 Power supply

The power supply for the **NPCIe-XMC-4E1** must meet the following specifications:
- required for the module:
  - +12V: Depends on XMC
  - + 3,3V: Depends on XMC

5.3 Statement on Environmental Protection

5.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

5.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

5.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

5.3.4 Product Safety

The board complies with EN60950 and UL1950.

5.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Xilinx FPGA Programming Tool Vivado Lab Edition
https://www.xilinx.com/support/download.html

Appendix B: Document's History

Revision	Date	Description	Author
1.0	6.04.2018	initial release	se
1.1	16.05.2018	added FPGA programming information	se