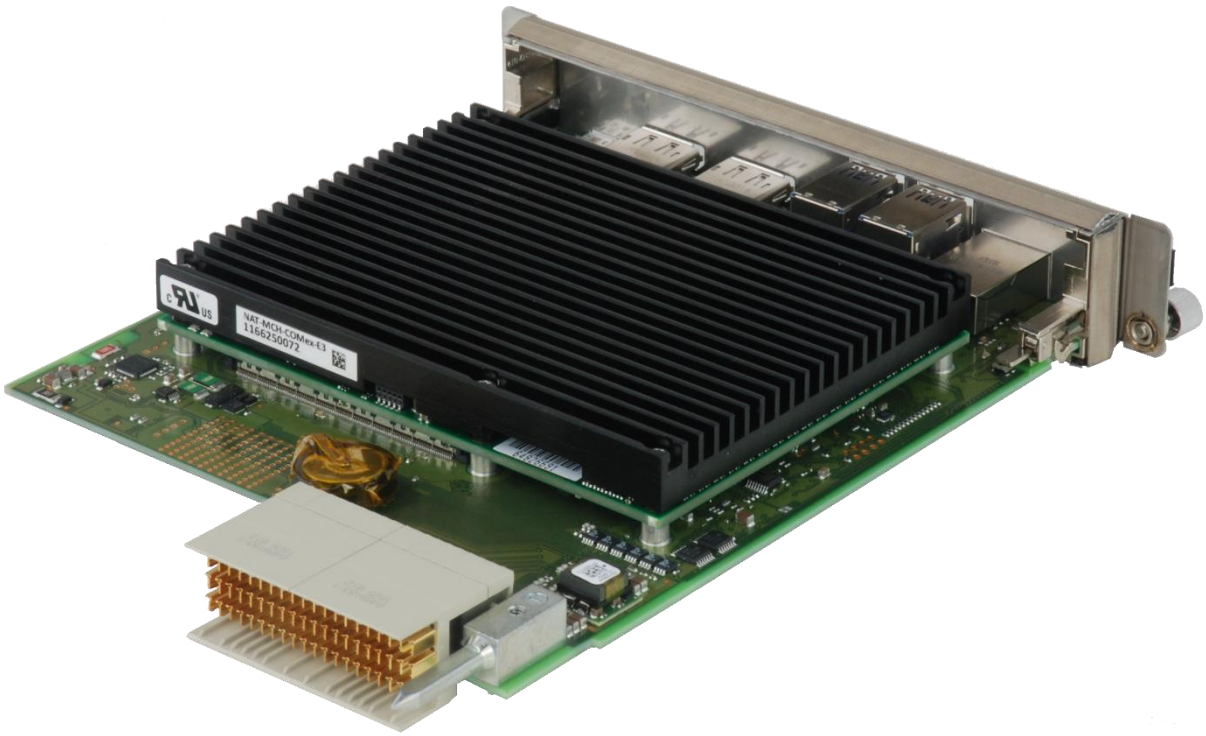
NAT-MCH-RTM / -RTM-BM / -RTM-FPGA

REAR TRANSITION MODULE FOR NAT-MCH-PHYS80

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.1

HW REVISION 2.4

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1. PREFACE

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The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-MCH-RTM's** functional capabilities. This board is available in three different variants; most information is valid for all variants, so – unless otherwise specified – for reasons of clarity it is referred to **NAT-MCH-RTM** only.

Preface

General information about this document

Introduction

Abstract on the **NAT-MCH-RTM's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-MCH-RTM** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-MCH-RTM's** main features

Configuration

Options to adapt the **NAT-MCH-RTM** to personal needs

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-MCH-RTM** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-MCH-RTM** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-MCH-PHYS80** and associated **NAT-MCH-RTM/-BM-FPGA**, both members of the **NAT-MCH** family of products, bring additional flexibility and scalability to MTCA.4 and MTCA.4.1 systems. The denomination Rear Transition Module (RTM) indicates, that the **NAT-MCH-RTM** uses the space behind the MCH slot(s) in a MicroTCA.4.1 chassis. It is a COMExpress Type 6 carrier module and if equipped with a COMExpress module, it works as a processor Advanced Mezzanine Card (PrAMC), storage, and graphic AMC, which releases AMC slot(s).

Moreover, the **NAT-MCH-RTM-BM** and **-BM-FPGA** allow the **NAT-MCH-PHYS80** to fully control the µRTM-backplane e.g. **NAT-LLRF**, which is located behind the standard MTCA.4 backplane for AMCs, and any item connected to this additional backplane, such as eRTM (extended RTM), RPM (Rear Power Modules) and (optionally) standard RTMs.

The **NAT-LLRF** backplane allows to combine systems that are traditionally separate - one for the digital part and one for the analogue part - into one single MicroTCA system. The required mechanics and the management extensions have been introduced to the PICMG MTCA.4.1 working group already in order to make these optional extensions available as part of the open MicroTCA.4.1 standard.

Using rear power modules, any RTM that connects to the µRTM-backplane (**NAT-LLRF** backplane) can be powered independently from its associated AMC, thus providing a higher power budget per AMC/RTM slot combination.

2.1. LLRF – Background

MicroTCA is a high-channel-density system standard. In order to increase system reliability and ease of maintenance, improve cable management, reduce performance limitations and the space occupied by external RF cabling, and finally for better EMC shielding of sensitive analog signals, N.A.T. GmbH has collaborated with DESY to develop a unique concept for extending the MicroTCA.4 system capabilities.

The MicroTCA low level RF backplane (**NAT-LLRF**) for µRTM cards is a hardware implementation of this new extension embedded in a MicroTCA.4 crate. The unit is a passive RTM backplane suited for the interconnection of high-precision RF and CLK signals and the delivery of high-performance managed analog power supply for µRTM and extended RTM (eRTM) modules. High-frequency signal distribution network was designed to operate in the DC – 6GHz band.

For more information about the **NAT-LLRF**, please refer to our homepage.

2.2. Variants

The basic functionality of the **NAT-MCH-RTM** variants is described below. Please regard that the main competence of the module appears when equipped with a COMExpress module.

2.2.1. NAT-MCH-RTM

The **NAT-MCH-RTM** is a double-wide full-size Rear Transition Module and COMExpress carrier.

2.2.2. NAT-MCH-RTM-BM

The **NAT-MCH-RTM-BM** owns Backplane Management and the Zone2 connector to control a µRTM backplane such as the **NAT-LLRF**.

The **NAT-MCH-PHYS80** together with the **NAT-MCH-RTM-BM** can handle up to two rear power modules, such as **NAT-RPM-AC600** (providing variable bipolar voltages for the LLRF backplane), or any standard MTCA power supply.

2.2.3. NAT-MCH-RTM-BM-FPGA

Moreover, the **NAT-MCH-RTM-BM-FPGA** provides an extra Zynq-FPGA to implement an extra bus (e.g. SPI) on the LLRF backplane to access eRTMs.

2.3. NAT-MCH-RTM-COMex

All variants of the **NAT-MCH-RTM** can be fitted with a COMExpress module Type 6 with Intel processors, e.g. Celeron® G-4932E, Core i3® 9100HL, or Xeon® E3 E-2276ML (others on request).

Thus, the **NAT-MCH-RTM-COMex**, **NAT-MCH-RTM-BM-COMex,** or **NAT-MCH-RTM-BM-FPGA-COMex** function as fully-featured replacements for a PrAMC, which would occupy one AMC payload slot.

2.4. Applications

In combination with the **NAT-MCH-PHYS80**, the **NAT-MCH-RTM-BM-FPGA** is working in science and research applications. For more information, please refer to chapter 6.1 Internal Reference Documentation.

2.5. Main Features

Table 1 – Technical Data

	NAT-MCH-RTM	NAT-MCH-RTM-BM	NAT-MCH-RTM-BM-FPGA
Form Factor	• Double-wide full-size Rear Transition Module and COMExpress carrier		
Mounting Slot	• For any type of COMExpress-Type 6 module validated by N.A.T.		
CPU (on COMEx)	• Celeron® G-4932E • Core i3® 9100HL • Xeon® E3 E-2276ML • (others on request)		
FPGA	• n/a		• XILINX Zynq-7000 SoC
Memory (on COMex)	• ECC and Non-ECC for 2x 8GB up to 2x 32GB DDR4		
Rear Panel Connections (via COMex)	• 2x DisplayPort (high resolution graphics) • 4x USB3.0 • 1x 1GbE		
Zone3 Connections	• 2x SATA connection to two SSD slots on **NAT-MCH-PHYS80** • One x16 PCIe Gen3 link to fat pipe switch (Fabrics D-S) on **NAT-MCH-PHYS80** • One 1GbE connection to GbE switch (Fabric A) on **NAT-MCH-PHYS80**		

	NAT-MCH-RTM	NAT-MCH-RTM-BM	NAT-MCH-RTM-BM-FPGA
Zone2 Connections	• n/a	• I^2C interface to EEPROM • IPMI to two Rear Power Modules • IPMI to three eRTMs, which have no connection to front AMCs	• I^2C interface to EEPROM • IPMI to two Rear Power Modules • IPMI to three eRTMs, which have no connection to front AMCs • FPGA for application specific intercommunication bus, e.g. SPI on LLRF to access eRTMs
Storage	• 1x standard SATA-SSD (2.5“) with 128 GB mounted on **NAT-MCH-PHYS80** • 2x half-slim SATA-SSD in RAID mode on request mounted on **NAT-MCH-PHYS80**		
Operating System	• Linux, Windows, WindRiver O/S (VxWorks, Linux, Hypervisor)		
Operating Environment	• Default: 0°C to +55°C (with forced cooling) • Humidity: 10% to 90% at +55°C (non-condensing)		
Storage Environment	• Default: -40°C to +85°C • Humidity: 10% to 90% (non-condensing)		
Compliance	• MTCA.0 R2.0, MTCA.4 R1.0, MTCA.4.1 R1.0, AMC.0 R2.0, AMC.1, AMC.2, AMC.4, IMPI V1.5 & V2.0, EN60950, UL1950, RoHS		

3. QUICK START

To ensure proper functioning of the **NAT-MCH-RTM** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the connectors to ensure proper contact when connecting the **NAT-MCH-RTM** to the MTCA-System.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

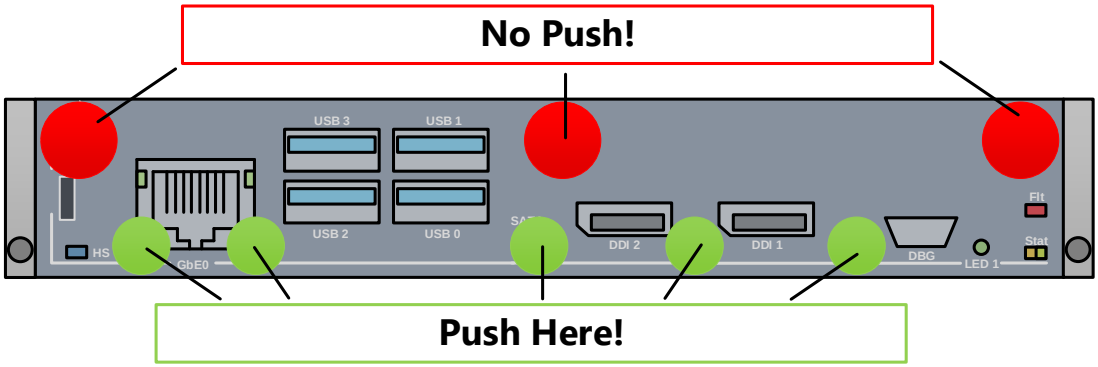
3.2. Mechanical Requirements

Insert the **NAT-MCH-RTM *first*** and ensure a proper connection, ***before*** pushing the **NAT-MCH-PHYS80** into the system!

Important: when installing the **NAT-MCH-RTM** to an MTCA-System, make sure to avoid any torsion force impact on the PCB to prevent the module from damaging!

Therefore, always push ***in line*** with the PCB. The following figures illustrates, which spots on the rear panel are safe to use, and which areas ***must not*** be used to push the **NAT-MCH-RTM** into its mating connector.

Figure 1 – Pushing Points for Mounting



The installation requires a MicroTCA.4 backplane and a **NAT-MCH-PHYS80** for connecting the **NAT-MCH-RTM**, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-MCH-RTM**, read the Installation Guide and the User's Manual of the **NAT-MCH-PHYS80** and the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is Hot-Swap capable, if you don't switch off the power.

Ensure that the **NAT-MCH-RTM** is connected to the **NAT-MCH-PHYS80** and the LLRF-backplane (if supported) with the connector(s) completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the rear panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAT-MCH-RTM** must meet the following specifications:

+12V / 1.0A max. (Optional COMExpress module not included!)

3.3.2. Hot-Swap

The **NAT-MCH-RTM** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-MCH-RTM** or the system it is plugged into from damage!

Insertion of a hot-swap-capable module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-MCH-RTM** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board

- If the information provided by the **NAT-MCH-RTM** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable module

- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAT-MCH-RTM** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

Essentially, the **NAT-MCH-RTM** works as COMExpress carrier module, so the board itself does not include too many complex functional blocks. Hence the block diagrams below show the interwork with a COMExpress module only.

The following figures give an overview of all three variants of the **NAT-MCH-RTM**.

Figure 2 – Block Diagram NAT-MCH-RTM

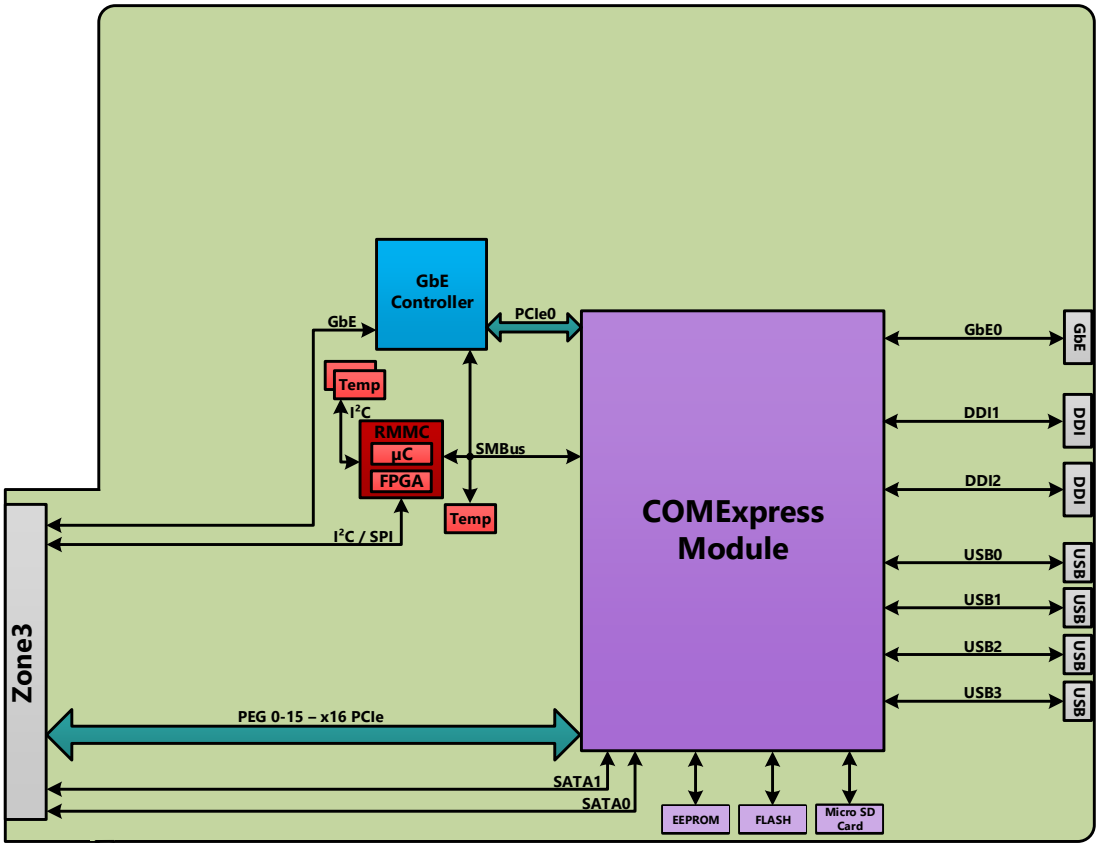


Figure 3 – Block Diagram NAT-MCH-RTM-BM

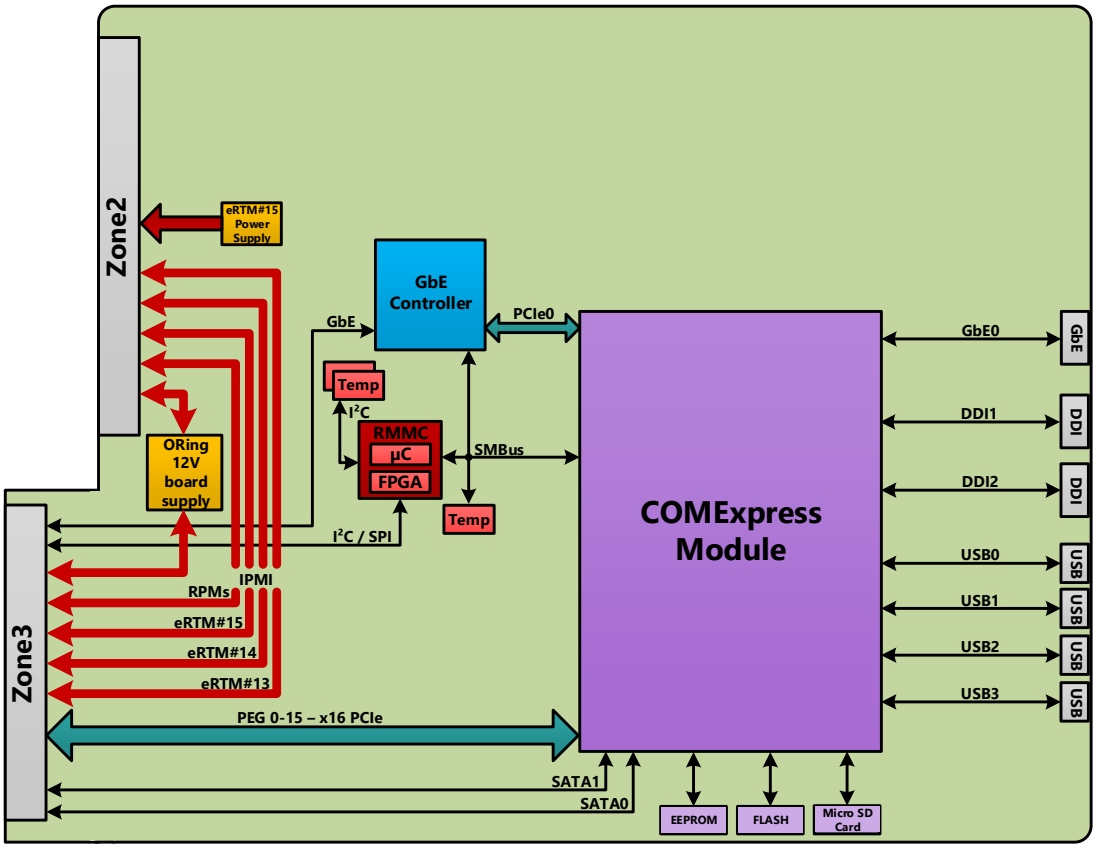
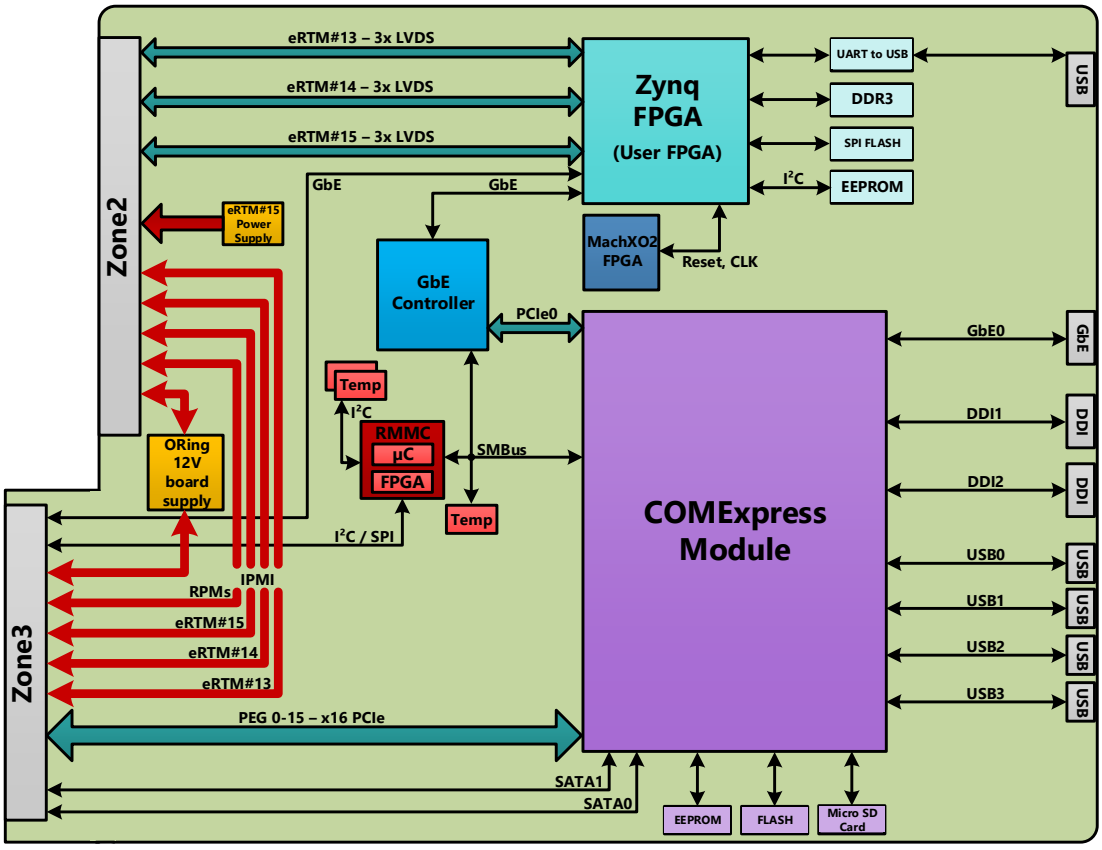


Figure 4 – Block Diagram NAT-MCH-RTM-BM-FPGA



4.1. Gigabit Ethernet Controller

The **NAT-MCH-RTM** features an Intel I350 Ethernet Controller with 1000Base-T, SGMII, and SerDes interface.

4.2. FPGA

Depending on the variant, the **NAT-MCH-RTM** is equipped with a different number of FPGAs, which are described in the following paragraphs.

4.2.1. NAT-MCH-RTM

The **NAT-MCH-RTM** features a Lattice MachXO2 LCMXO2-2000 FPGA, which in combination with the Atmel AVR-Microcontroller works as Rear Module Management Controller. Please see chapter 4.4 Rear Module Management Controller (RMMC) for details.

4.2.2. NAT-MCH-RTM-BM-FPGA

In addition to the standard assembly, the **NAT-MCH-RTM-BM-FPGA** owns a XILINX Zynq FPGA and another Lattice-FPGA.

4.2.2.1. Zynq

The **NAT-MCH-RTM-BM-FPGA** is equipped with a XILINX Zynq-7000 FPGA which gives the opportunity to implement separate busses e.g. SPI on LLRF backplane to access eRTMs.

4.2.2.2. MachXO2

A second Lattice MachXO2 FPGA – LCMXO2-1200 – is assembled to support the Zynq FPGA regarding reset- and clock tasks.

4.3. Memory

According to the variant, the **NAT-MCH-RTM** is equipped with a different numbers and types of memory, which are described in the following paragraphs.

4.3.1. NAT-MCH-RTM

4.3.1.1. EEPROM

The **NAT-MCH-RTM** is assembled with an 8K Serial EEPROM connected to the COMExpress-Module.

4.3.1.2. FLASH

The **NAT-MCH-RTM** features a 32MB SPI-FLASH and another 256MB SPI-FLASH.

4.3.1.3. Micro-SD-Card

The appropriate slot on the **NAT-MCH-RTM** offers the opportunity, to equip the board with a Micro-SD-Card.

4.3.2. NAT-MCH-RTM-BM-FPGA

The Zynq FPGA on the **NAT-MCH-RTM-BM-FPGA** is surrounded by a number of additional memory devices.

4.3.2.1. EEPROM

The **NAT-MCH-RTM-BM-FPGA** is equipped with a 2K Serial EEPROM.

4.3.2.2. SPI FLASH

Two 256Mbit SPI-FLASH components are assembled on the **NAT-MCH-RTM-BM-FPGA**.

4.3.2.3. DDR3 SDRAM

The **NAT-MCH-RTM-BM-FPGA** features two 4GB DDR3-1600 SDRAM chips.

4.4. Rear Module Management Controller (RMMC)

The Rear Module Management Controller of the **NAT-MCH-RTM** is made up of an Atmel ATmega1284 AVR Microcontroller and a Lattice MachXO2 LCMXO2-2000 FPGA.

4.5. COMExpress-Module (optional)

The **NAT-MCH-RTM** can be equipped with any COMExpress module Type 6 validated by N.A.T.. The I/O as available from the COMExpress module is brought to the rear panel of the **NAT-MCH-RTM**.

The board connects to the **NAT-MCH-PHYS80** via the Zone3 connector and offers the COMExpress module an x16 PCIExpress Gen3 path to the PCIe switch on the **NAT-MCH-PHYS80,** as well as a SATA connection. The **NAT-MCH-PHYS80** is a double-wide, full-size MCH, with a special clock module providing low jitter and skew, and a PCIe switch module, providing Gen3 (30Gbps) bandwidth at the fat pipe, and can be equipped with one or two SATA Flash Drives (SSD).

4.6. Rear Panel Interfaces

If equipped with a COMExpress module, the **NAT-MCH-RTM** owns various interfaces at the rear panel, which are described in the following sections.

4.6.1. Ethernet Uplink Port

The GbE0 interface is connected to the rear panel via an RJ45 connector.

4.6.2. USB3.0

The **NAT-MCH-RTM** features four USB3.0 interfaces at the rear panel.

4.6.3. Display Ports

The **NAT-MCH-RTM** offers two high resolution graphic ports at the rear panel.

4.6.4. SATA

The signals of the SATA-SSDs mounted on the **NAT-MCH-PHYS80** are routed to the rear panel by the COMExpress module.

4.6.5. Debug Connector

The COMExpress module features two serial ports which both are routed to the MachXO2 FPGA of the **NAT-MCH-RTM**. Per default the second serial port of the COMExpress module (CE SER1) is connected to the **NAT-MCH** Telnet Bridge, and the Micro-USB serial connects to the Zynq FPGA.

Via register entry, the user can select which of these serial interfaces connects to the Micro-USB terminal on the rear plate, and which is routed to the **NAT-MCH**'s Telnet Bridge interface. Use `'Diag → RTM diag submenue → Read FPGA/Atmel register'`. At `'0x1F'` the following values should be found, corresponding to defaults: `MCH-UART => CE SER1, FP-UART => Zynq`

By use of `'Write FPGA/Atmel register'`, values can be changed.

Table 2 – Routing of COMExpress Serial Ports

Bit	Name	Description	Default	Access
4..7		Source for MCH-UART (Telnet Bridge)	0x2	R/W
0..3		Source for Micro-USB at rear plate	0x3	R/W

Assignments: 0x1: COMExpress SER0 / 0x2: COMExpress SER1 / 0x3: Zynq FPGA

4.7. Power Supply

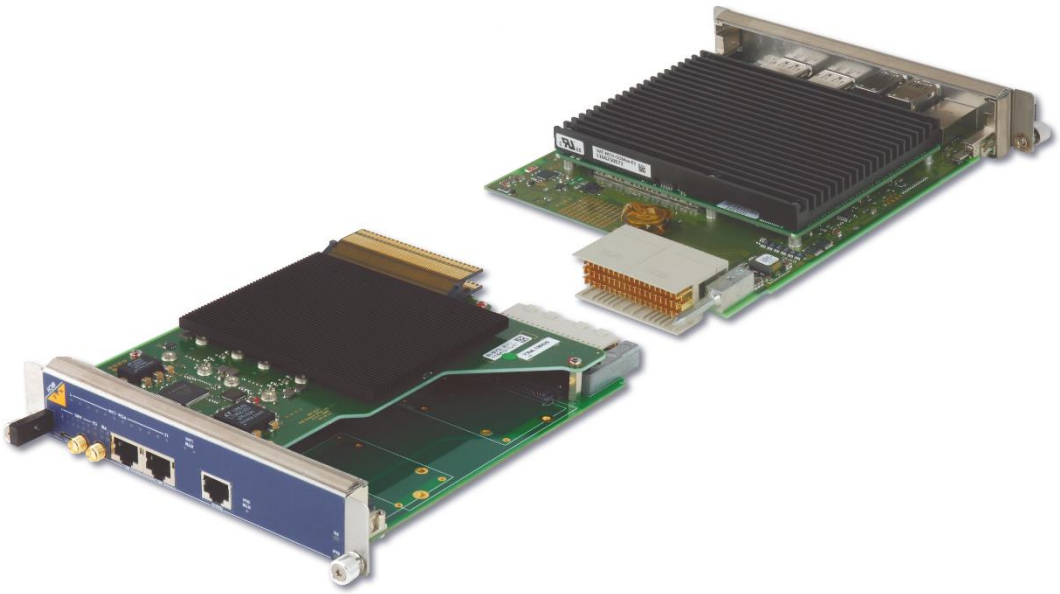
The **NAT-MCH-RTM** can make use of two power sources: the **NAT-MCH-PHYS80** via the Zone3 connector, or – if available - Rear Power Modules (RPM) via Zone2 connector (**-BM** / **-BM-FPGA** version only.)

The **NAT-MCH-RTM** on the other hand generates the voltage rails required by the ComExpress module.

4.8. Backplane Interfaces

The **NAT-MCH-RTM** works in combination with the **NAT-MCH-PHYS80**. The photo below shows the combination of both modules.

Figure 5 – NAT-MCH-RTM in combination with NAT-MCH-PHYS80



4.8.1. Zone3-Connector

4.8.1.1. Power Supply and Management

The **NAT-MCH-PHYS80** provides a local generated 3.3V management power and a switched version of the MCH's 12V payload power to the **NAT-MCH-RTM**. Both supplies are ramped and over-current controlled to support hot-swapping. For management issues, an IPMB-L interface is supported.

Note: Due to the maximum current capability of the Zone3 connector pins, this solution is restricted to a maximum of 3A for the whole RTM including all components.

4.8.1.2. NAT-MCH-RTM-Interfaces

The **NAT-MCH-PHYS80** features a PCIe Gen3 connection up to x16, a GbE interface, and two SATA interfaces towards the **NAT-MCH-RTM**.

If the attached **NAT-MCH-RTM** owns a Backplane Manager, the **NAT-MCH-PHYS80** can be connected to the µRTM-Backplane vie Zone2 connector and thus is able to control the µRTM-Backplane itself as well as any module connected to it, such as eRTM, RPM, or standard RTM.

For more information on the **NAT-MCH-PHYS80** and its features, please check the manual and/or fact sheet available on our website.

4.8.2. Zone2- Connector (NAT-MCH-RTM-BM / -BM-FPGA only)

4.8.2.1. Power Supply

As the power supply via Zone3 connector is limited to a maximum of 3A, a second power source via Zone2 connector is available. This increases the maximum available current to the same amount as a standard AMC but requires a rear backplane and at least one Rear Power Module.

4.8.2.2. Backplane Manager

The Backplane Manager of the **NAT-MCH-RTM-BM** / **-BM-FPGA** allows the usage of eRTMs in a MTCA.4 system. An eRTM is a standalone RTM, which needs no AMC in the front, as it is plugged into the rear backplane directly.

To manage these eRTMs and the related Rear Power Modules, the Backplane Manager is basically connecting the required I^2C connections from the Zone3 to the Zone2 connector. The main management is done on the **NAT-MCH-PHYS80**. To isolate the front and the rear backplane, these I^2C connections on the **NAT-MCH-RTM-BM** /**-BM-FPGA** are realized via I^2C expander.

4.8.2.3. eRTM15 Power Supply

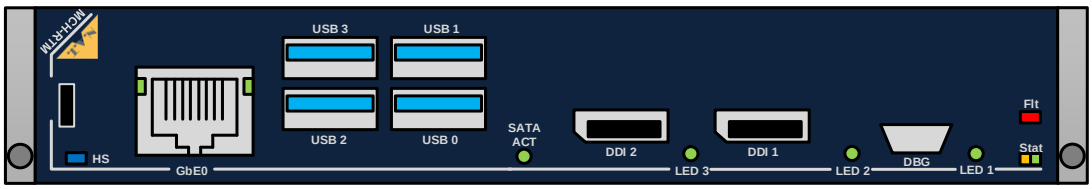
For simple systems that support a rear backplane but do not have any RPM, the **NAT-MCH-RTM-BM** / **-BM-FPGA** can act as a simplified Rear Power Module for eRTM15 only. If more eRTMs are desired, one or more (Rear) Power Modules are required.

5. HARDWARE

5.1. Rear Panel and LEDs

The **NAT-MCH-RTM** is equipped with various LEDs described in the following section.

Figure 6 – NAT-MCH-RTM: Rear Panel



The module contains the standard LEDs consisting of a blue hot-swap LED, a red fault indication LED and an orange/green general purpose status LED controlled by the RMMC. The fault indication LED turns to ***"On"*** if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to ***"Off"*** again. For detailed information on the behavior of the HS-LED, please refer to chapter 3.3.2 Hot-Swap.

Two LEDs integrated in the RJ45 Ethernet jack are driven directly by the COMExpress GBE0_LINK#, GBE0_LINK100#, GBE0_LINK1000n, and GBE0_ACT# signals.

LED 1-3 are also connected to the RMMC but can be controlled by the user via a register interface.

The "SATA ACT" LED reflects the status of optional mounted SATA-SDD(s) on the **NAT-MCH-PHYS80**.

5.2. Component-, Connector-, and Switch-Location

Figure 7 - NAT-MCH-RTM – Location Diagram – Top

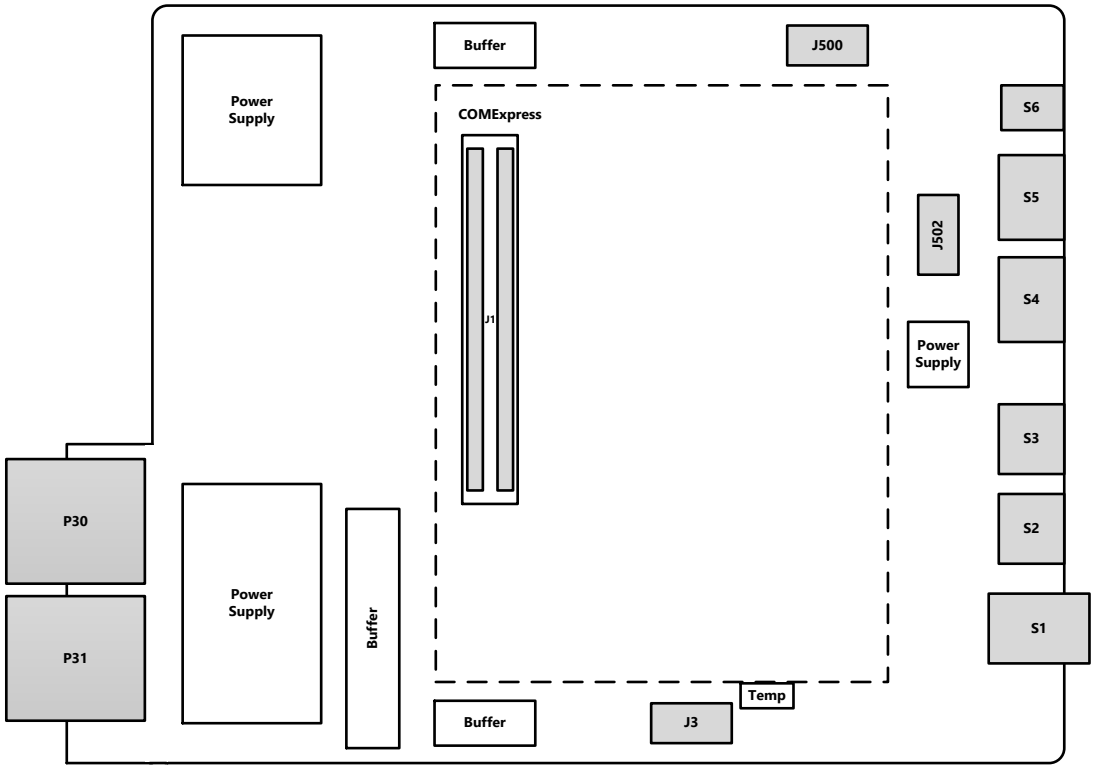


Figure 8 - NAT-MCH-RTM – Location Diagram – Bottom

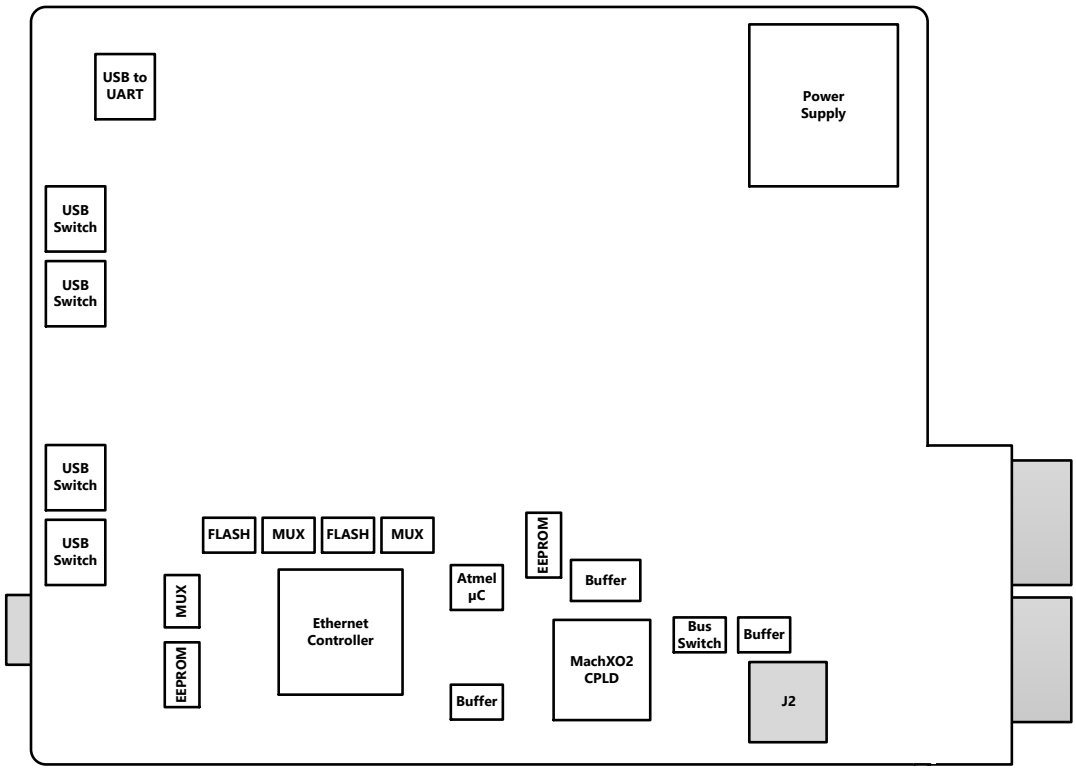


Figure 9 – NAT-MCH-RTM-BM / -BM-FPGA – Location Diagram – Top

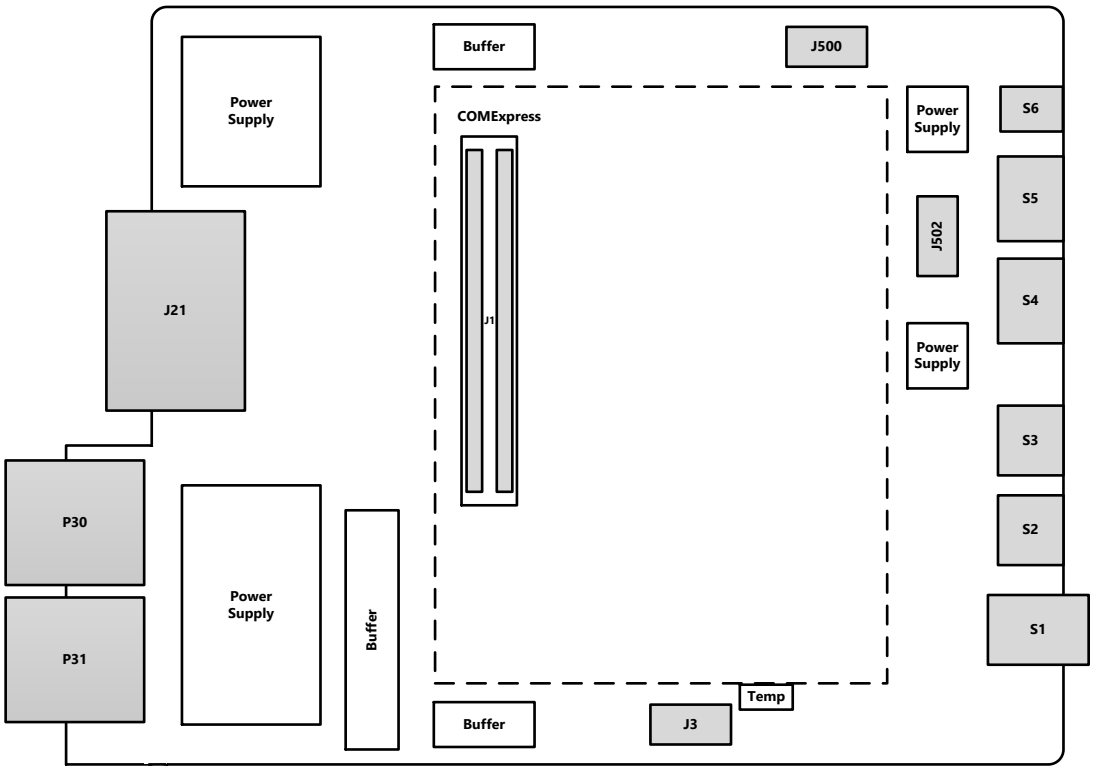
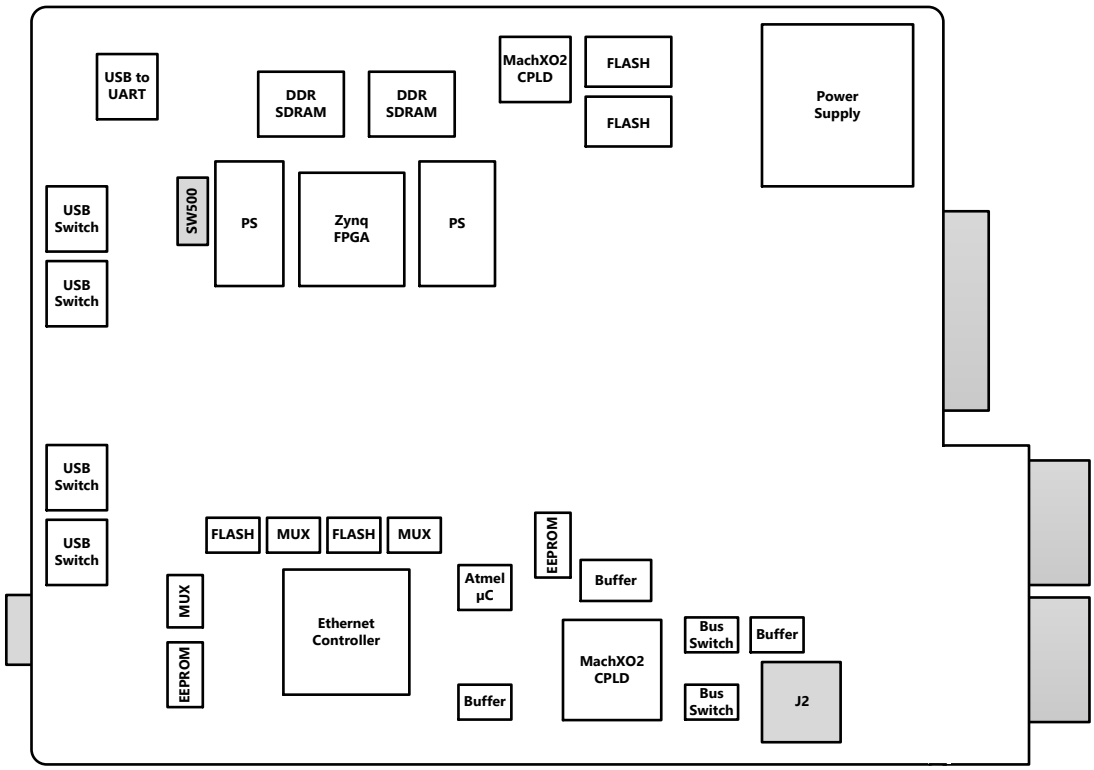


Figure 10 – NAT-MCH-RTM-BM / -BM-FPGA – Location Diagram – Bottom



Please refer to the following tables to look up the connector pin assignments of the **NAT-MCH-RTM**.

Connectors on top side: drawings imply the board is orientated with the Zone3 connector to the ***left*** side

Connectors on bottom side: drawings imply the board is orientated with the Zone3 connector to the ***right*** side

5.2.1. J1 A/B and J1 C/D: COMExpress Module Connectors

Connectors J1 A/B and J1 C/D connect to the optional COMExpress module.

Figure 11 – J1 A/B and J1 C/D: COMExpress Module Connectors

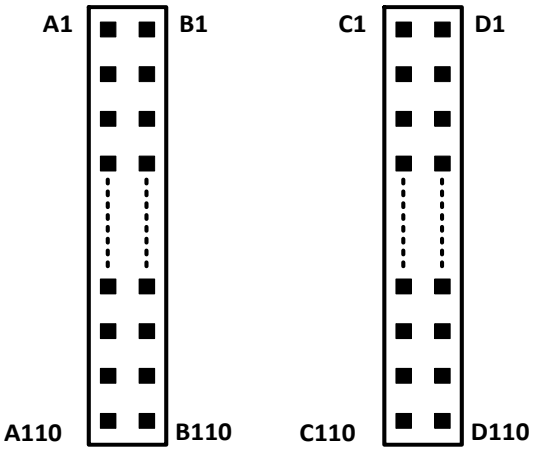


Table 3 – J1 A/B: COMExpress Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	GND	GND	B1
A2	GBE0_MDI3-	GBE0_ACT#	B2
A3	GBE0_MDI3+	NC	B3
A4	GBE0_LINK100#	NC	B4
A5	GBE0_LINK1000#	NC	B5
A6	GBE0_MDI2-	NC	B6
A7	GBE0_MDI2+	NC	B7
A8	GBE0_LINK#	NC	B8
A9	GBE0_MDI1-	NC	B9
A10	GBE0_MDI1+	NC	B10
A11	GND	GND	B11
A12	GBE0_MDI0-	PWRBTN#	B12
A13	GBE0_MDI0+	SMB_CK	B13
A14	GBE0_CTREF	SMB_DAT	B14
A15	SUS_S3#	SMB_ALERT#	B15
A16	RTM_SATA0-Tx+	RTM_SATA1-Tx+	B16
A17	RTM_SATA0-Tx-	RTM_SATA1-Tx-	B17
A18	SUS_S4#	SUS_STAT#	B18
A19	RTM_SATA0-Rx+	RTM_SATA1-Rx+	B19
A20	RTM_SATA0-Rx-	RTM_SATA1-Rx-	B20
A21	GND	GND	B21
A22	NC	NC	B22
A23	NC	NC	B23
A24	SUS_S5#	PWR_OK	B24
A25	NC	NC	B25

Pin #	Signal	Signal	Pin #
A26	NC	NC	B26
A27	BATLOW#	WDT	B27
A28	ATA_ACT#	NC	B28
A29	NC	NC	B29
A30	NC	NC	B30
A31	GND	GND	B31
A32	NC	NC	B32
A33	NC	I2C_CK	B33
A34	BIOS_DIS0#	I2C_DAT	B34
A35	THRMTRIP#	THRM#	B35
A36	NC	NC	B36
A37	NC	NC	B37
A38	NC	NC	B38
A39	USB4-	NC	B39
A40	USB4+	NC	B40
A41	GND	GND	B41
A42	USB2-	USB3-	B42
A43	USB2+	USB3+	B43
A44	USB_2_3_OC#	USB_0_1_OC#	B44
A45	USB0-	USB1-	B45
A46	USB0+	USB1+	B46
A47	VCC_RTC	NC	B47
A48	EXCD0_PERST#	NC	B48
A49	EXCD0_CPPE#	SYS_RESET#	B49
A50	NC	CB_RESET#	B50
A51	GND	GND	B51
A52	NC	NC	B52
A53	NC	NC	B53
A54	SD_DATA0	SD_CMD	B54
A55	NC	NC	B55
A56	NC	NC	B56
A57	GND	SD_WP	B57
A58	NC	NC	B58
A59	NC	NC	B59
A60	GND	GND	B60
A61	NC	NC	B61
A62	NC	NC	B62
A63	SD_DATA1	SD_CD#	B63
A64	PCIE_TX1+	PCIe1-Rx+	B64
A65	PCIE_TX1-	PCIe1-Rx-	B65
A66	GND	WAKE0#	B66
A67	SD_DATA2	WAKE1#	B67
A68	PCIE_TX0+	PCIe0-Rx+	B68
A69	PCIE_TX0-	PCIe0-Rx-	B69
A70	GND	GND	B70
A71	NC	NC	B71
A72	NC	NC	B72
A73	NC	NC	B73
A74	NC	NC	B74

Pin #	Signal	Signal	Pin #
A75	NC	NC	B75
A76	NC	NC	B76
A77	NC	NC	B77
A78	NC	NC	B78
A79	NC	NC	B79
A80	GND	GND	B80
A81	NC	NC	B81
A82	NC	NC	B82
A83	NC	NC	B83
A84	NC	+5V	B84
A85	SD_DATA3	+5V	B85
A86	RSVD	+5V	B86
A87	RSVD	+5V	B87
A88	PCIe_CLK_REF+	BIOS_DIS1#	B88
A89	PCIe_CLK_REF-	NC	B89
A90	GND	GND	B90
A91	SPI_POWER	NC	B91
A92	SPI_MOSI	NC	B92
A93	SD_CLK	NC	B93
A94	SPI_CLK	NC	B94
A95	SPI_MISO	NC	B95
A96	TPM_PP	NC	B96
A97	TYPE10#	SPI_CS#	B97
A98	SER0_TX	NC	B98
A99	SER0_RX	NC	B99
A100	GND	GND	B100
A101	SER0_TX	NC	B101
A102	SER0_RX	NC	B102
A103	LID#	SLEEP#	B103
A104	+12V	+12V	B104
A105	+12V	+12V	B105
A106	+12V	+12V	B106
A107	+12V	+12V	B107
A108	+12V	+12V	B108
A109	+12V	+12V	B109
A110	GND	GND	B110

Table 4 – J1 C/D: COMExpress Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
C1	GND	GND	D1
C2	GND	GND	D2
C3	USB0_SSRX-	USB0_SSTX-	D3
C4	USB0_SSRX+	USB0_SSTX+	D4
C5	GND	GND	D5
C6	USB1_SSRX-	USB1_SSTX-	D6
C7	USB1_SSRX+	USB1_SSTX+	D7
C8	GND	GND	D8
C9	USB2_SSRX-	USB2_SSTX-	D9
C10	USB2_SSRX+	USB2_SSTX+	D10
C11	GND	GND	D11
C12	USB3_SSRX-	USB3_SSTX-	D12
C13	USB3_SSRX+	USB3_SSTX+	D13
C14	GND	GND	D14
C15	NC	DDI1_AUX+	D15
C16	NC	DDI1_AUX-	D16
C17	RSVD	RSVD	D17
C18	RSVD	RSCD	D18
C19	NC	NC	D19
C20	NC	NC	D20
C21	GND	GND	D21
C22	NC	NC	D22
C23	NC	NC	D23
C24	DDI1_HPD	RSVD	D24
C25	NC	RSVD	D25
C26	NC	DDI1_PAIR0+	D26
C27	RSVD	DDI1_PAIR0-	D27
C28	RSVD	RSVD	D28
C29	NC	DDI1_PAIR1+	D29
C30	NC	DDI1_PAIR1-	D30
C31	GND	GND	D31
C32	DDI2_AUX+	DDI1_PAIR2+	D32
C33	DDI2_AUX-	DDI1_PAIR2-	D33
C34	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL	D34
C35	RSVD	RSVD	D35
C36	NC	DDI1_PAIR3+	D36
C37	NC	DDI1_PAIR3-	D37
C38	NC	RSVD	D38
C39	NC	DDI2_PAIR0+	D39
C40	NC	DDI2_PAIR0-	D40
C41	GND	GND	D41
C42	NC	DDI2_PAIR1+	D42
C43	NC	DDI2_PAIR1-	D43
C44	NC	DDI2_HPD	D44
C45	RSVD	RSVD	D45
C46	NC	DDI2_PAIR2+	D46
C47	NC	DDI2_PAIR2-	D47

Pin #	Signal	Signal	Pin #
C48	RSVD	RSVD	D48
C49	NC	DDI2_PAIR3+	D49
C50	NC	DDI2_PAIR3-	D50
C51	GND	GND	D51
C52	PEG_RX0+	PEG_TX0+	D52
C53	PEG_RX0-	PEG_TX0-	D53
C54	TYPE0#	PEG_LANE_RV#	D54
C55	PEG_RX1+	PEG_TX1+	D55
C56	PEG_RX1-	PEG_TX1-	D56
C57	TYPE1#	TYPE2#	D57
C58	PEG_RX2+	PEG_TX2+	D58
C59	PEG_RX2-	PEG_TX2-	D59
C60	GND	GND	D60
C61	PEG_RX3+	PEG_TX3+	D61
C62	PEG_RX3-	PEG_TX3-	D62
C63	RSVD	RSVD	D63
C64	RSVD	RSVD	D64
C65	PEG_RX4+	PEG_TX4+	D65
C66	PEG_RX4-	PEG_TX4-	D66
C67	RSVD	GND	D67
C68	PEG_RX5+	PEG_TX5+	D68
C69	PEG_RX5-	PEG_TX5-	D69
C70	GND	GND	D70
C71	PEG_RX6+	PEG_TX6+	D71
C72	PEG_RX6-	PEG_TX6-	D72
C73	GND	GND	D73
C74	PEG_RX7+	PEG_TX7+	D74
C75	PEG_RX7-	PEG_TX7-	D75
C76	GND	GND	D76
C77	RSVD	RSVD	D77
C78	PEG_RX8+	PEG_TX8+	D78
C79	PEG_RX8-	PEG_TX8-	D79
C80	GND	GND	D80
C81	PEG_RX9+	PEG_TX9+	D81
C82	PEG_RX9-	PEG_TX9-	D82
C83	RSVD	RSVD	D83
C84	GND	GND	D84
C85	PEG_RX10+	PEG_TX10+	D85
C86	PEG_RX10-	PEG_TX10-	D86
C87	GND	GND	D87
C88	PEG_RX11+	PEG_TX11+	D88
C89	PEG_RX11-	PEG_TX11-	D89
C90	GND	GND	D90
C91	PEG_RX12+	PEG_TX12+	D91
C92	PEG_RX12-	PEG_TX12-	D92
C93	GND	GND	D93
C94	PEG_RX13+	PEG_TX13+	D94
C95	PEG_RX13-	PEG_TX13-	D95
C96	GND	GND	D96

Pin #	Signal	Signal	Pin #
C97	RSVD	RSVD	D97
C98	PEG_RX14+	PEG_TX14+	D98
C99	PEG_RX14-	PEG_TX14-	D99
C100	GND	GND	D100
C101	PEG_RX15+	PEG_TX15+	D101
C102	PEG_RX15-	PEG_TX15-	D102
C103	GND	GND	D103
C104	+12V	+12V	D104
C105	+12V	+12V	D105
C106	+12V	+12V	D106
C107	+12V	+12V	D107
C108	+12V	+12V	D108
C109	+12V	+12V	D109
C110	GND	GND	D110

5.2.2. J2: MicroSD-Card Slot

The **NAT-MCH-RTM** can be equipped with a Micro-SD-Card which can be used as removable FLASH memory.

Figure 12 – J2: Micro-SD-Card Slot

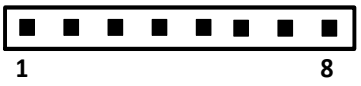


Table 5 – J2: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SD_DATA2	SD_DATA3	2
3	SD_CMD	+3.3V	4
5	SD_CLK	GND	6
7	SD_DATA0	SD_DATA1	8

5.2.3. J3: Lattice FPGA Programming Header

J3 offers programming access to the Lattice MacoXO2 on the **NAT-MCH-RTM**.

Figure 13 – J3: Lattice FPGA Programming Header

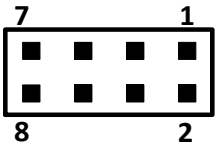


Table 6 – J3: Lattice FPGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RTM-MP	FPGA_TDO	2
3	FPGA_TDI	Nc	4
5	FPGA_JTAGENB	FPGA_TMS	6
7	GND	FPGA_TCK	8

5.2.4. J21: Zone2 Connector (NAT-MCH-RTM-BM / -BM-FPGA only)

J21 links to the rear backplane and is used for power, control signals, IPMI, and LVDS connection.

Figure 14 – J21: Zone2 Connector

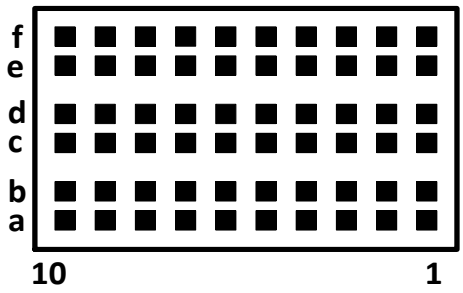


Table 7 – J21: Zone2 Connector – Pin Assignment

Col→ / Row ↓	a	b	ab	c	d	cd	e	f	ef	g	h	gh
1	LVDS13a_P	LVDS13a_N	GND	LVDS13b_P	LVDS13b_N	GND	LVDS13c_P	LVDS13c_N	GND	LVDS18a_P	LVDS18a_N	GND
2	LVDS14a_P	LVDS14a_N	GND	LVDS14b_P	LVDS14b_N	GND	LVDS14c_P	LVDS14c_N	GND	LVDS18b_P	LVDS18b_N	GND
3	LVDS15a_P	LVDS15a_N	GND	LVDS15b_P	LVDS15b_N	GND	LVDS15c_P	LVDS15c_N	GND	LVDS18c_P	LVDS18c_N	GND
4	LVDS16a_P	LVDS16a_N	GND	LVDS16b_P	LVDS16b_N	GND	LVDS16c_P	LVDS16c_N	GND	LVDS17b_P	LVDS17b_N	GND
5	LVDS17a_P	LVDS17a_N	GND	GA0	RFU	GND	LVDS17c_P	LVDS17c_N	GND	RFU	RFU	GND
6	SMP	PS_PM#	GND	GA1	PMP_C#	GND	PMP_B#	RST_PM_B#	GND	PM_OK#	PS1#	GND
7	SDA_L (#13)	SCL_L (#13)	GND	GA2	ENABLE#	GND	RST_PM_C#	RFU	GND	PP+12V (#15)	PP+12V (#15)	GND
8	SDA_L (#14)	SCL_L (#14)	GND	SDA_L (#15)	SCL_L (#15)	GND	I2C_SDA	I2C_SDL	GND	PP+12V (#15)	PP+12V (#15)	GND
9	Z2_12V	Z2_12V	GND	Z2_12V	Z2_12V	GND	PS1# (#15)	ENABLE# (#15)	GND	SDA_A	SCL_A	GND
10	Z2_12V	Z2_12V	GND	Z2_12V	Z2_12V	GND	MP+3.3V (#15)	PWR_ON (#15)	GND	SDA_B	SCL_B	GND

5.2.5. J500: XILINX Zynq FPGA Extension Header

J500 is an extension / debugging header connecting to the XILINX Zynq FPGA for future use.

Figure 15 – J500: XILINX Zynq FPGA Extension Header

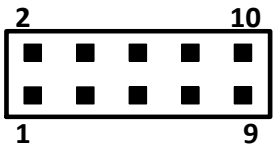


Table 8 – J500: XILINX Zynq FPGA Extension Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	EXT1	EXT2	2
3	EXT3	EXT4	4
5	EXT5	EXT6	6
7	EXT7	EXT8	8
9	FPGA3V3	GND	10

5.2.6. J502: Shared JTAG Header

J502 is a shared JTAG header which allows updating the XILINX Zynq FPGA and the Lattice MachX02 FPGA associated with the Zynq as well (**NAT-MCH-RTM-BM-FPGA** only). Configuration can be set via SW500, please refer to chapter 5.2.13 SW500: Boot Mode / FPGA Device Select for detailed information.

Figure 16 – J502: Shared JTAG Header

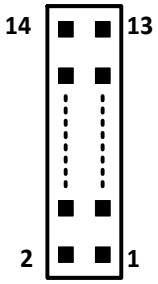


Table 9 – J502: Sheared JTAG Header– Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	V_PROG	2
3	GND	TMSPLD	4
5	GND	TCKPLD	6
7	GND	TPOPLD	8
9	GND	TDIPLD	10
11	GND	nc	12
13	GND	X_SYS_RSTn	14

5.2.7. P30/P31: Zone3 Connectors

P30 and P31 link to the **NAT-MCH-PHYS80**.

Figure 17 – P30/P31: Zone3 Connectors

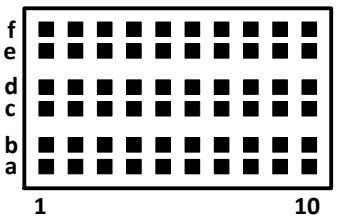


Table 10 – P30: Zone3 Connector – Pin Assignment

Col → / Row ↓	A	B	GND	C	D	GND	E	F	GND
1	Z3_12V	Z3_12V	GND	RTM_PS#	RTM_SDA	GND	RTM_TCK	RTM_TDO	GND
2	Z3_12V	Z3_12V	GND	RTM_MP	RTM_SCL	GND	RTM_TDI	RTM_TMS	GND
3	RTM_ETH1-Rx_P	RTM_ETH1-Rx_N	GND	RTM_ ETH0-Rx_P	RTM_ ETH0-Rx_N	GND	RTM_ PCIe00-Rx_P	RTM_ PCIe00-Rx_N	GND
4	RTM_ETH1-Tx_P	RTM_ETH1-Tx_N	GND	RTM_ ETH0-Tx_P	RTM_ ETH0-Tx_N	GND	RTM_ PCIe00-Tx_P	RTM_ PCIe00-Tx_N	GND
5	RTM_EN	MCH_SPICLK	GND	RTM_ SATA0-Rx_P	RTM_ SATA0-Rx_N	GND	RTM_ PCIe01-Rx_P	RTM_ PCIe01-Rx_N	GND
6	MCH_MISO	MCH_MOSI	GND	RTM_ SATA0-Tx_P	RTM_ SATA0-Tx_N	GND	RTM_ PCIe01-Tx_P	RTM_ PCIe01-Tx_N	GND
7	MCH_SPISEL0n	MCH_SPISEL1n	GND	RTM_ SATA1-Rx_P	RTM_ SATA1-Rx_N	GND	RTM_ PCIe02-Rx_P	RTM_ PCIe02-Rx_N	GND
8	RTM_IO1_0	RTM_IO1_1	GND	RTM_ SATA1-Tx_P	RTM_ SATA1-Tx_N	GND	RTM_ PCIe02-Tx_P	RTM_ PCIe02-Tx_N	GND
9	RTM_IO1_2	RTM_IO1_3	GND	MCH_ UART-RxD	MCH_ UART-TxD	GND	RTM_ PCIe03-Rx_P	RTM_ PCIe03-Rx_N	GND
10	RTM_IO1_4	RTM_IO1_5	GND	RTM_ PCIe-CLK0_P	RTM_ PCIe-CLK0_N	GND	RTM_ PCIe03-Tx_P	RTM_ PCIe03-Tx_N	GND

Table 11 – P31: Zone3 Connector – Pin Assignment

Col → / Row ↓	A	B	GND	C	D	GND	E	F	GND
1	RTM_IO1_6	RTM_IO1_7	GND	RTM_ PCIe04-Tx_P	RTM_ PCIe04-Tx_N	GND	RTM_ PCIe05-Tx_P	RTM_ PCIe05-Tx_N	GND
2	RTM_IO2_0	RTM_IO2_1	GND	RTM_ PCIe06-Tx_P	RTM_ PCIe06-Tx_N	GND	RTM_ PCIe07-Tx_P	RTM_ PCIe07-Tx_N	GND
3	RTM_IO2_2	RTM_IO2_3	GND	RTM_ PCIe04-Rx_P	RTM_ PCIe04-Rx_N	GND	RTM_ PCIe05-Rx_P	RTM_ PCIe05-Rx_N	GND
4	RTM_IO2_4	RTM_IO2_5	GND	RTM_ PCIe06-Rx_P	RTM_ PCIe06-Rx_N	GND	RTM_ PCIe07-Rx_P	RTM_ PCIe07-Rx_N	GND
5	RTM_IO2_6	RTM_IO2_7	GND	RTM_ PCIe08-Tx_P	RTM_ PCIe08-Tx_N	GND	RTM_ PCIe09-Tx_P	RTM_ PCIe09-Tx_N	GND
6	RTM_ PCIe08-Rx_P	RTM_ PCIe08-Rx_N	GND	RTM_ PCIe10-Tx_P	RTM_ PCIe10-Tx_N	GND	RTM_ PCIe11-Tx_P	RTM_ PCIe11-Tx_N	GND
7	RTM_ PCIe09-Rx_P	RTM_ PCIe09-Rx_N	GND	RTM_ PCIe12-Tx_P	RTM_ PCIe12-Tx_N	GND	RTM_ PCIe13-Tx_P	RTM_ PCIe13-Tx_N	GND
8	RTM_ PCIe10-Rx_P	RTM_ PCIe10-Rx_N	GND	RTM_ PCIe14-Tx_P	RTM_ PCIe14-Tx_N	GND	RTM_ PCIe15-Tx_P	RTM_ PCIe15-Tx_N	GND
9	RTM_ PCIe-CLK1_P	RTM_ PCIe-CLK1_N	GND	RTM_ PCIe11-Rx_P	RTM_ PCIe11-Rx_N	GND	RTM_ PCIe12-Rx_P	RTM_ PCIe12-Rx_N	GND
10	RTM_ PCIe15-Rx_P	RTM_ PCIe15-Rx_N	GND	RTM_ PCIe14-Rx_P	RTM_ PCIe14-Rx_N	GND	RTM_ PCIe13-Rx_P	RTM_ PCIe13-Rx_N	GND

5.2.8. S1: RJ45 Connector

Figure 18 – S1 RJ45 Ethernet Connector

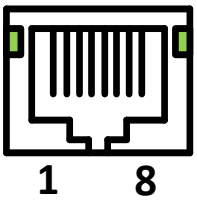


Table 12 – S1: RJ45 Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MX0+	MX0-	2
3	MX1+	MX2+	4
5	MX2-	MX1-	6
7	MX3+	MX3-	8

5.2.9. S2 A/B and S3 A/B: USB 3.0 Connectors

Figure 19 – S2/S3: USB 3.0 Connectors

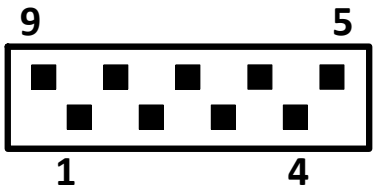


Table 13 – S2 A: USB3.0 Connector

Pin #	Signal	Signal	Pin #
1	USB2_VBUS	USB2_N	2
3	USB2_P	USB2_GND	4
5	USB2_SSRX_N	USB2_SSRX_P	6
7	USB2_GND_D	USB2_SSTX_N	8
9	USB2_SSTX_P		

Table 14 – S2 B: USB3.0 Connector

Pin #	Signal	Signal	Pin #
10	USB3_VBUS	USB3_N	11
12	USB3_P	USB3_GND	13
14	USB3_SSRX_N	USB3_SSRX_P	15
16	USB3_GND_D	USB3_SSTX_N	17
18	USB3_SSTX_P		

Table 15 – S3 A: USB3.0 Connector

Pin #	Signal	Signal	Pin #
1	USB0_VBUS	USB0_N	2
3	USB0_P	USB0_GND	4
5	USB0_SSRX_N	USB0_SSRX_P	6
7	USB0_GND_D	USB0_SSTX_N	8
9	USB0_SSTX_P		

Table 16 – S3 B: USB3.0 Connector

Pin #	Signal	Signal	Pin #
10	USB1_VBUS	USB1_N	11
12	USB1_P	USB1_GND	13
14	USB1_SSRX_N	USB1_SSRX_P	15
16	USB1_GND_D	USB1_SSTX_N	17
18	USB1_SSTX_P		

5.2.10. S4/S5: Display Port Connectors

S4 and S5 provide a high resolution graphics interface towards the rear plate.

Figure 20 – S4/S5: Display Port Connectors

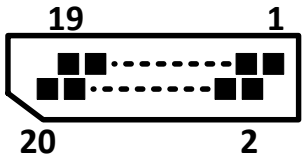


Table 17 – S4: Display Port Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	C_DDI1_PAIR0_P	GND	2
3	C_DDI1_PAIR0_N	C_DDI1_PAIR1_P	4
5	GND	C_DDI1_PAIR1_N	6
7	C_DDI1_PAIR2_P	GND	8
9	C_DDI1_PAIR2_N	C_DDI1_PAIR3_P	10
11	GND	C_DDI1_PAIR3_P	12
13	DDI1_DDC_AUX_SEL	DDI1_CONFIG2	14
15	DDI1_AUX_P	GND	16
17	DDI1_AUX_N	DDI1_HPD	18
19	GND	DDI1_PWR(+3.3V)	20

Table 18 – S5: Display Port Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	C_DDI2_PAIR0_P	GND	2
3	C_DDI2_PAIR0_N	C_DDI2_PAIR1_P	4
5	GND	C_DDI2_PAIR1_N	6
7	C_DDI2_PAIR2_P	GND	8
9	C_DDI2_PAIR2_N	C_DDI2_PAIR3_P	10
11	GND	C_DDI2_PAIR3_P	12
13	DDI2_DDC_AUX_SEL	DDI2_CONFIG2	14
15	DDI2_AUX_P	GND	16
17	DDI2_AUX_N	DDI2_HPD	18
19	GND	DDI2_PWR(+3.3V)	20

5.2.11. S6: Debug Connector

S6 features a Micro-USB debug interface on the **NAT-MCH-RTM**.

Figure 21 – S6: USB Debug Connector

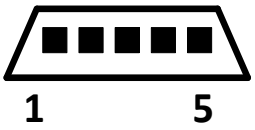


Table 19 – S6: USB Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC	D-	2
3	D+	Nc	4
5	GND	SGND	6
7	SGND	SGND	8
9	SGND	SGND	10
11	SGND		

5.2.12. SW1: Hot-Swap-Switch

Switch SW1 is used to support hot-swapping of the module. It conforms to PICMG AMC.0.

5.2.13. SW500: Boot Mode / FPGA Device Select

SW500 -1 determines which boot source is used for the XILINX Zynq FPGA.

SW500 -2 determines which FPGA device is addressed for programming.

The tables below provide information on the operating parameters and configuration options of SW500.

Figure 22 – SW500: Boot Mode / FPGA Device Select

Table 20 – SW500: Boot Mode / FPGA Device Select – Operating Parameters

Switch #	Function
SW500 -1	On: MicroSD-Card selected as boot source ***OFF: SPI Flash selected as boot source***
SW500 -2	On: Lattice MachXO2 FPGA is selected for programming ***OFF: XILINX Zynq FPGA is selected for programming***

Note:

Default configuration is labelled with ***bold, italic letters***.

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

- **NAT-MCH** User's Manual:
  https://www.nateurope.com/manuals/nat_mch_man_usr.pdf
- **NAT-MCH-PHYS80**:
  https://www.nateurope.com/manuals/nat_mch_phys_v2x_man_hw.pdf
- Application:
  https://www.nateurope.com/documents/SS_High_Energy_Physics.pdf

6.2. External Reference Documentation

- Lattice MachXO2 FPGA Family Data Sheet, DS1035, V3.3, 03/2017
- XILINX Zynq-7000 SoC FPGA Data Sheet Overview, DS190, V1.11.1, 07/2018
- Intel Ethernet Controller I350 Data Sheet, Document #336626-001, Rev.2.6, 10/2017

6.3. Standards Compliance

- MTCA.0 R2.0
- MTCA.4 R1.0
- MTCA.4.1 R1.0
- AMC.0 R2.0
- AMC.1
- AMC.2
- AMC.4
- IMPI V1.5 & V2.0
- EN60950
- UL1950

6.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.7. Product Safety

The board complies with EN60950 and UL1950.

6.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6.9. Abbreviation List

Table 21 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
BM	Backplane Manager
CLK	Clock
COM Express	Computer-On-Module Express
CPU	Central Processing Unit
DDI	Dual Display Interface
DDR3 SDRAM	Double Data Rate Synchronous Dynamic RAM
DESY	Deutsches Elektronen-Synchrotron
ECC	Error Correcting Code
EEPROM	Electrically Erasable PROM
EMC	Electromagnetic Compatibility
eRTM	Extended RTM
FLASH	Non-Volatile Memory
FLASH	Free Electron LASer - DESY facility
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LLRF	Low Latency Radio Frequency
LVDS	Low Voltage Differential Signaling
µC	Microcontroller

Abbreviation	Description
µRTM	Micro RTM
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
PCI(e)	Peripheral Component Interconnect (Express)
PrAMC	Processor AMC
(P)ROM	(Programmable) Read Only Memory
RAID	Redundant Array of Inexpensive Disks
RAM	Random Access Memory
RF	Radio Frequency
RMMC	Rear Module Management Controller
RPM	Rear Power Module
RTM	Rear Transition Module
SATA	Serial Advanced Technology Attachment
SD-Card	Secure Digital Memory Card
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SoC	System On A Chip
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SSD	Solid State Drive
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XFEL	X-Ray Free Electron Laser - DESY facility

7. DOCUMENT'S HISTORY

Table 22 – Document's History

Rev	Date	Description	Author
1.0	05.02.2019	• initial release	se
1.1	29.07.2021	• Minor changes, e.g. typos • Reworked information about supported COMex module types • Reworked information about supported SATA-SSD types • Updated Chapter 3 Quick Start: added information about safe mounting of the **NAT-MCH-RTM** • Updated Block Diagrams Figure 2 - Figure 4 (Design only) • Updated Figure 6 • Updated Chapter 6 Specifications and Compliances	se