NAT-MCH-PHYS / NAT-MCH-PHYS80

MTCA CARRIER HUB FOR MTCA.4 AND MTCA.4.1

DESIGNED BY N.A.T. GMBH

TECHNICAL REFERENCE MANUAL V1.1

HW REVISION 2.X

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1. PREFACE

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-MCH-PHYS'** and **NAT-MCH-PHYS80's** functional capabilities. Most information is valid for both variants, so – unless otherwise specified – for reasons of clarity it is referred to **NAT-MCH-PHYS** only.

Preface

General information about this document

Introduction

Abstract on the **NAT-MCH-PHYS'** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-MCH-PHYS** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-MCH-PHYS'** main features

Hardware

Information about locations, components, and connectors

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-MCH-PHYS** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-MCH-PHYS** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-MCH-PHYS** is based on the **NAT-MCH-M4**, a double-width MCH baseboard for MicroTCA.4 systems, combined with the **NAT-MCH-CLK-PHYS**, a special low latency and low jitter clock module, and the **NAT-MCH-PCIex48** PCIe Gen3 hub module. It addresses the requirements for management and high bandwidth switching to AMCs in PCIe based MTCA.4 systems, targeting large control and data acquisition applications.

The **NAT-MCH-PHYS80**, which consists as well of the **NAT-MCH-M4** base plus the **NAT-MCH-CLK-PHYS**, is moreover equipped with the **NAT-MCH-PCIex80** hub module, which features an 80-port PCIe Gen3 switch. Combined with the Rear Transition Module with quad-core Intel Xeon E3 CPU, this is the most powerful single-slot solution for management, data switching, and processing that is available for MTCA.4 and MTCA.4.1 systems. The option for optical and copper uplinks makes it ideal for large control and data acquisition applications such as high and low energy physics research institutions.

2.1. Basic Functionality

2.1.1. Redundant Management

The **NAT-MCH-PHYS** fully supports redundant management and power environments. Frequent exchange of the internal databases with the secondary MCH and a heartbeat mechanism ensure an immediate switch-over from the primary to the secondary MCH whenever it becomes necessary (PCIe fat pipe switch over may require additional precautions).

2.1.1.1. NAT-MCH-PHYS

The **NAT-MCH-PHYS** can handle up to four power modules, such as the **NAT-PM-DC840** or **NAT-PM-AC600**, for N+1 configurations.

2.1.1.2. NAT-MCH-PHYS80

The **NAT-MCH-PHYS80** can handle up to four -48V, +24V or AC power modules, such as **NAT-PM-DC840, NAT-PM-DC600LV, NAT-PMAC600, NAT-PM-AC600D, NAT-PM-1000**, or a combination of them for N+1 configurations.

The **NAT-MCH-PHYS80** together with the **NAT-MCH-RTM-BM** (LLRF backplane management) can handle in addition up to two rear power modules, such as **NAT-RPM-AC600** (providing variable bipolar voltages for the LLRF backplane), or any standard MTCA power supply.

2.1.2. Clocking

The clock module **NAT-MCH-CLK-PHYS** has been specially designed for physics and scientific research applications, providing very low jitter and constant latency.

2.1.3. PCIe Gen3 Switching

2.1.3.1. NAT-MCH-PHYS

The PCIe hub module provides a 48-port PCIe Gen3 switch that allows each of the 12 AMCs in a MicroTCA.4 system to be connected by an x4 link.

2.1.3.2. NAT-MCH-PHYS80

The PCIe hub module provides an 80-port PCIe Gen3 switch that allows each of the 12 AMCs in a MicroTCA.4.x system to be connected by an x4 link. It provides either two x8 or one x16 optional optical PCIe uplink(s) to external high performance servers or other MTCA.4 systems.

2.1.4. Software Support and Updates

Apart from the Java GUI **NATview**, the **NAT-MCH-PHYS** also supports external management solutions, which are based on the Remote Management Control Protocol (RMCP), such as **NATview** or the open-source tool ipmitool.

Furthermore, using the **NAT-MIB** the **NAT-MCH-PHYS** can also be integrated into environments based on the Simple Network Management Protocol (SNMP). The **NAT-MCH-PHYS** can be configured using either uploadable text based script files or via the integrated web interfaces using a standard web browser. Finally, the integrated debug and configuration facilities can be accessed via a serial console or using Telnet.

2.2. Applications

The **NAT-MCH-PHYS** as well as the **NAT-MCH-PHYS80** are working in the DESY research centers at the FLASH and XFEL facilities. For more information, please refer to chapter 6.1 Internal Reference Documentation.

2.3. Main Features

Table 1 – Technical Data

	NAT-MCH-PHYS	NAT-MCH-PHYS80
Form Factor	Double-width, full-size AMC Width: 147 mm, Depth: 180.6 mm	
CPU	NXP (Freescale) ColdFire MCF54452 CPU @ 266 MHz	
Memory	DDR2 RAM: 32 / 64 MB FLASH: 16 / 32 / 64 MB	DDR2 RAM: 32 / 64 MB FLASH: 16 / 32 / 64 MB SATA-SSD (optional) • 1x 2.5" Standard SSD or • 2x Half-Slim SSD
IPMI and Compliance	13 AMCs 2 front and 2 rear cooling units 1-4 power modules incl. N+1 redundancy PICMG AMC.0 PICMG 2.9 Update to 2nd MCH	
Fabric A Gigabit Ethernet	12 AMCs + optional AMC13 in 2nd MCH slot PICMG AMC.2 R1.0 PICMG SFP.1 R1.0	
Fabric D-G	PCI Express Gen3 to 12 AMCs • x1 or x4 to 12 AMCs PICMG AMC.1 R1.0	PCI Express Gen3 to 12 AMCs • x1 or x4 to 12 AMCs • One x16 or two x8 to optical uplink (optional) • x16 to RTM or to one AMC slot (requires backplane support) PICMG AMC.1 R1.0
Clock Distribution NAT-MCH-CLK-PHYS	CLK1 and CLK2 by special low jitter and low latency circuitry (**NAT-MCH-CLK-PHYS**) CLK3 fixed mean 100 MHz PCIe clock (HCSL)	
Carrier Manager	Management of up to 13 AMCs, 4 cooling units, and 1-4 power modules Supports redundant architectures and fail-over procedure Supports configurable emergency shutdown of AMCs or entire system	Management of up to 13 AMCs, 4 cooling units, and 1-4 power modules Management of 4 eRTMs and 2 rear power modules via LLRF backplane Supports redundant architectures and fail-over procedure Supports configurable emergency shutdown of AMCs or entire system
System and Shelf Manager	For detached or stand-alone operation, both managers are available on-board, hook-in for external managers via 1 GbE port at front panel	
Operating System Support	O/S: OK1 API: HPI compliant	

Indicator LEDs	3 standard AMC LEDs 12 bi-color LEDs for AMC slot states 2 bi-color LEDs for cooling units 4 bi-color LEDs for power modules 12 bi-color LEDs for PCIe links status (failed, Gen1, Gen2, or Gen3)	3 standard AMC LEDs 12 bi-color LEDs for AMC slot states 2 bi-color LEDs for cooling units 4 bi-color LEDs for power modules 12 bi-color LEDs for PCIe links status (failed Gen1, Gen2, or Gen3) 2 bi-color LEDs for PCIe-Uplink 2 bi-color LEDs for RTM-PCIe-Link
Front Panel Connectors	2x 1GbE for management connection and Fabric A system up-link (load sharing supported) External clock reference (bi-directional) Serial and USB console connectors	2x 1GbE for management connection and Fabric A system up-link (load sharing supported) External clock reference (bi-directional) Serial and USB console connectors Fabric D-G uplink (two x8 or one x16***)***
Order Codes: NAT-MCH – [Options]		
-PHYS	Double-wide full-size MCH for MTCA.4 applications featuring PCIe x48	na
-PHYS80	na	Double-width full-size MCH for MTCA.4 applications featuring PCIex80
-PHYS80-UPLNK	na	Like –PHYS80 with additional optical uplinks (either two x8 or one x16) for PCIe
-RTM-UPLNK	na	Double-wide full-size RTM providing one copper uplink (x16) for PCIe
-RTM	na	Double-wide full-size RTM and COM Express carrier
-RTM-BM	na	As above plus Backplane Management and Zone2 connector for µRTM backplanes, e.g LLRF backplane
-RTM-BM-FPGA	na	As -RTM-BM plus ZYNQ-FPGA to implement separate bus e.g. SPI on LLRF backplane to access eRTMs
-COMex-E3	na	COM Express module Type 6 with Quad Core Intel® Xeon® Processor E3 (E3-1505LV5 25W 4c/8t HDP530 2.0GHz 8MB incl. ECC up to 16 GB DDR3-1066)
Operating Environment	Default: 0°C to +55°C (with forced cooling) Humidity: 10% to 90% at +55°C (non-condensing)	
Storage Environment	Default: -40°C to +85°C Humidity: 10% to 90% (non-condensing)	

3. QUICK START

To ensure proper functioning of the **NAT-MCH-PHYS** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the MCH-Connector to ensure proper contact when inserting the **NAT-MCH-PHYS** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The installation requires an µTCA-Backplane for connecting the **NAT-MCH-PHYS**, a power supply, and cooling devices.

Before installing or uninstalling the **NAT-MCH-PHYS**, read the Installation Guide and the User's Manual of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is Hot-Swap-capable, if you do not switch off the power.

Ensure that the **NAT-MCH-PHYS** is connected to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. SATA-SSD

The **NAT-MCH-PHYS80** features two interfaces for optional SATA-SSDs, which allow the installation of one standard SATA-SSD (2.5") or two Half-Slim-SATA-SSDs. Mounting holes for both sizes are provided on the PCB.

The following pictures show the **NAT-MCH-PHYS80** with mounted SSDs.

Figure 1 – NAT-MCH-PHYS80 with installed 2.5" SATA-SSD

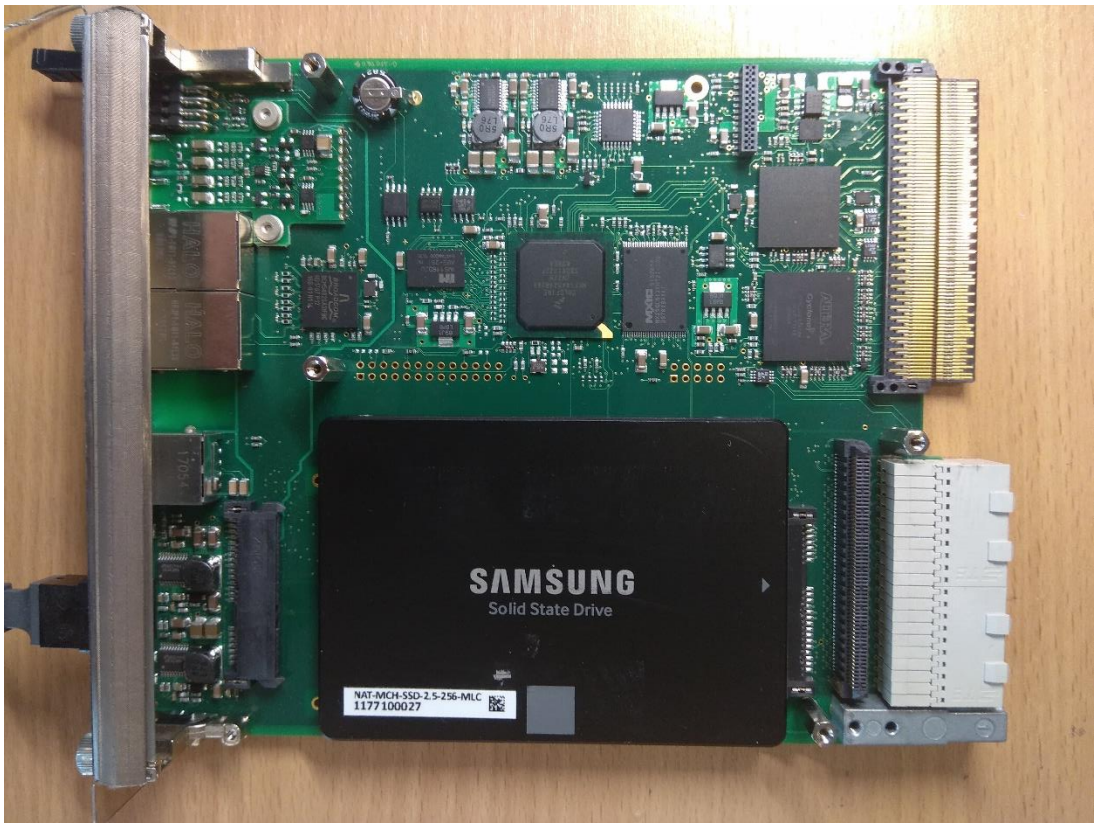
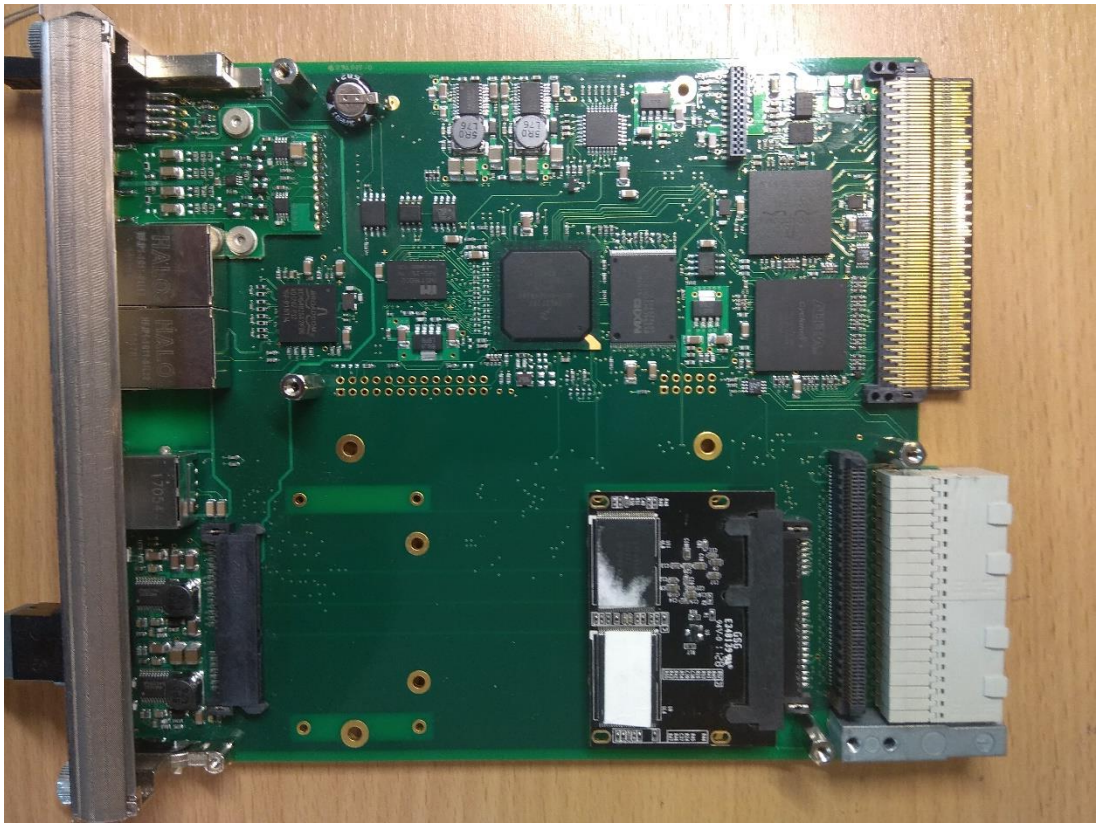


Figure 2 - NAT-MCH-PHYS80 with installed Half-Slim SATA-SSD



Both configurations show the SATA-SSD connected to SATA0 via connector J7. For detailed information on the pin assignment, please refer to chapter 5.2.7 J7/J8: SATA Connectors (NAT-MCH-PHYS80 only).

3.4. Voltage Requirements

3.4.1. Power supply

The power supply for the **NAT-MCH-PHYS** must meet the following specifications:

+12V / 7.3A max. (+12V / 4.5A typ.)

3.4.2. Hot-Swap

The **NAT-MCH-PHYS** supports Hot-Swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAT-MCH-PHYS** or the system it is plugged into from damage!

Insertion of a Hot-Swap-capable Module

- Ensure the module and the backplane/carrier support Hot-Swapping
- Ensure that the Hot-Swap-handle is in "unlock"-position (pulled out)
- Push the **NAT-MCH-PHYS** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the Hot-Swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAT-MCH-PHYS** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a Hot-Swap-capable Module

- Pull the Hot-Swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAT-MCH-PHYS** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

The **NAT-MCH-PHYS** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figures give an overview on the functional blocks of both variants.

Figure 3 – Block Diagram NAT-MCH-PHYS

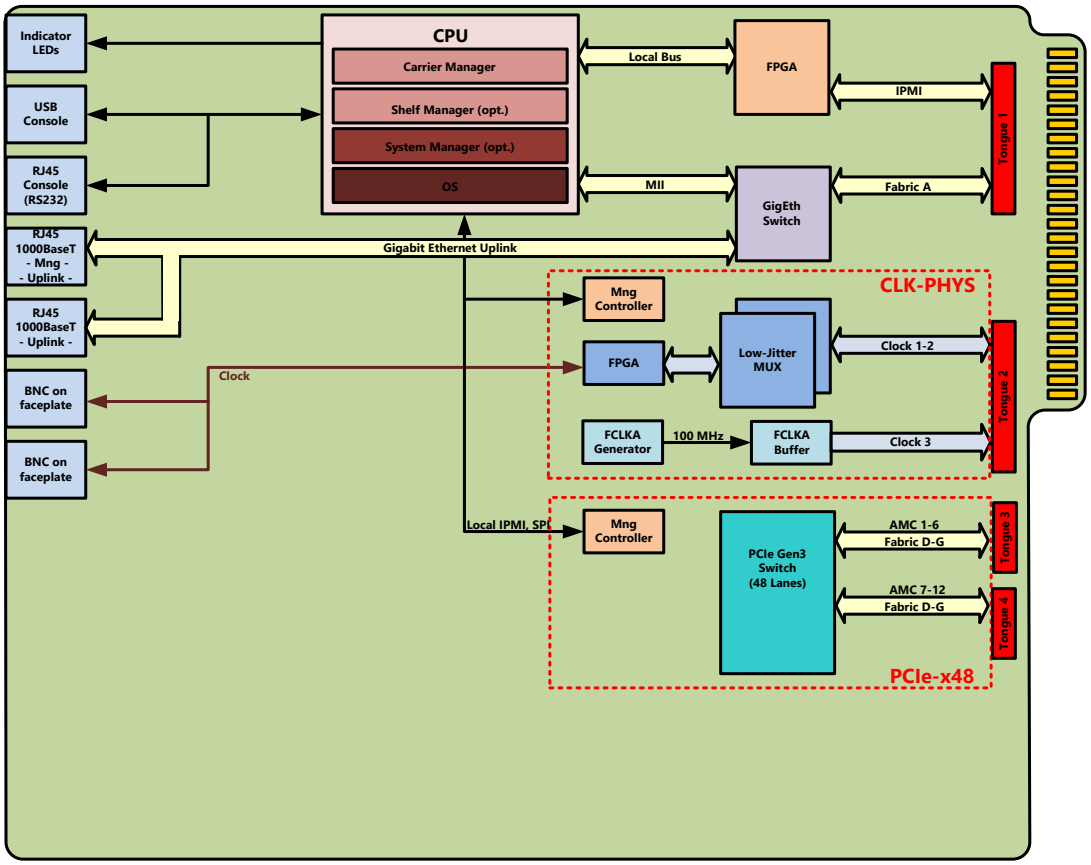
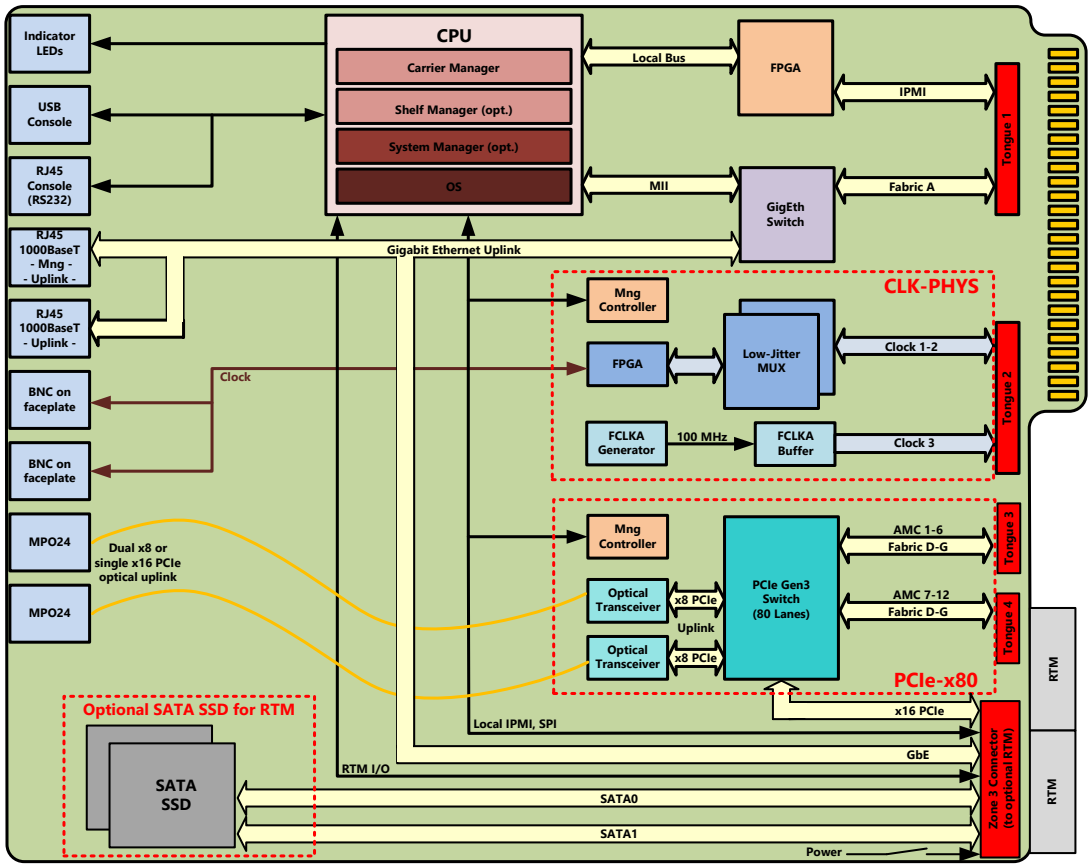


Figure 4 – Block Diagram NAT-MCH-PHYS80



4.1. CPU

The **NAT-MCH-PHYS** features a 32-bit CPU ColdFire MCF54452 (Freescale) which is based on the V4e ColdFire core. The MCF54452 includes a memory management unit (MMU), a dual precision floating-point unit (FPU), and an enhanced multiply-accumulate unit (EMAC), delivering 308 (Drystone 2.1) MIPS at 266 MHz.

The processor has integrated a 32 KB I-Cache, a 32 KB D-Cache and 32 KB on-chip system SRAM. The MCF54452 is equipped with a 32-bit DDR2 266 controller at 133 MHz clock rate.

It integrates the following interfaces:

- two 10/100 Ethernet Controllers (FECs)
- DSPI – SPI with DMA capability
- I^2C interface
- 16-channel DMA controller
- USB Interface

4.2. FPGA

The **NAT-MCH-PHYS** is equipped with an Intel/Altera Cyclone FPGA, which acts as IPMI-Controller for the AMCs operating in the MTCA-System. Moreover, it provides PCIe-Hot-Plug functionality to PCIe-based AMCs.

4.3. Memory

4.3.1. DDR2SDRAM

The on-board DDR2SDRAM memory is 16 bit wide and provides 32 or 64 MB (assembly option). The interface to the SDRAM is implemented in the ColdFire MCF54452 CPU. By programming several registers, the SDRAM controller can be adapted to different RAM architectures.

4.3.2. FLASH

FLASH memory is connected to the demultiplexed upper 16 data bits D0 – 15 of the local bus and to the latched address lines. Its size (16, 32, or 64 MB) depends on the assembly option. The FLASH memory on the **NAT-MCH-PHYS** can be programmed by the CPU (by appropriate software) or via the BDM port.

4.3.3. SATA SSD (NAT-MCH-PHYS80 only)

Optionally, one standard 2.5" SATA SDD or two Half-Slim SATA-SSDs can be installed on the **NAT-MCH-PHYS80**. The baseboard offers two SATA connectors including power supply and the required mounting holes with SATA0 via connector J7 and SATA1 via connector J8. For detailed information, please refer to chapter 5.2.7 J7/J8: SATA Connectors (NAT-MCH-PHYS80 only).

The SATA connections are directly routed to the Zone3 RTM Connector J30. For detailed information, please refer to chapter 5.2.8 J30/J31: Zone3 Connectors (NAT-MCH-PHYS80 only).

4.4. Ethernet Switch

The Broadcom BCM5396 Gigabit Ethernet Switch provides a layer 2, non-blocking, low-latency Gigabit Ethernet switch, supporting VPN as well as a port based rate control. The BCM5396 supports Fabric A switching according to MicroTCA.0 R1.0 and PICMG SFP.1 R1.0, serving up to 12 AMCs as well as the update channel from the second **NAT-MCH** in redundant environments. Also supported are two uplink ports at the front panel of the **NAT-MCH-PHYS80** in order to interconnect to other carriers, shelves or systems. Please refer to chapter 4.6.1 Ethernet Uplink Ports for details.

The configuration register of the BMC5396 can be accessed through the MCF54452's PHY message channel interface.

For frame management the BMC5396 is connected to the MCF54452's TSEC0 through the MII interface.

4.5. I²C Devices

Three I²C Devices are available on the **NAT-MCH-PHYS**, which are connected to the MCF54452 via I²C bus

- An EEPROM (24C08) used for storage of board-specific information (address 0x50)
- Two temperature sensors (LM75), which sense the board temperature near CPU and near FPGA (addresses 0x9C and 0x9E)

4.6. Front Panel Interfaces

The **NAT-MCH-PHYS** is equipped with various interfaces at the front panel, which are described in the following sections.

4.6.1. Ethernet Uplink Ports

Two ports of the BCM5396 Gigabit Ethernet Switch are wired to connectors GbE1 and GbE2 via a Broadcom BCM5482 1000BaseT physical layer chip. Via this device, the user may access fabric A also from the front panel.

GbE1: The switch interfaces the network to fabric A and to the ColdFire CPU. Therefore, this port can be used to update the ColdFire Software and to permit communication with external shelf or system managers.

GbE2: Together with GbE1, this port can be used to increase the bandwidth of the uplink. Instead of the second GbE-Interface, the **NAT-MCH-PHYS** can be equipped with a RJ45 clock interface (see chapter 4.6.3.2 RJ45-Clock-Interface for details).

Configuration settings of the BCM5482 are done by CPU ports. The BCM5461 PHY has to be set up in GBIC mode (1000BaseT to 1000BaseX translation). Like all other I/O devices, the BCM5461 PHY is resettable by programming an FPGA register.

4.6.2. USB Debug Port

The front panel micro USB connector available on the **NAT-MCH-PHYS** is connected to the USB capable Atmel Atmega16U2. This microcontroller implements a serial interface device, which is connected to the ColdFire MCF54452 UART. It provides a console interface for configuration, monitoring, and debugging.

The microcontroller USB interface is running in USB device mode. It is powered independently from the board power supply by USB, so a terminal connection will not get lost after reboot or power-cycle.

4.6.3. Clock Interface

The **NAT-MCH-PHYS** can be equipped with various External Reference Clock Transceiver Modules. The available transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL, and CMOS), and the supported connectors.

The external clock interfaces are routed from the transceiver module to the CLK-Module. Therefore, the external clock interfaces can only be used in collaboration with a **NAT-MCH CLK**-Module.

4.6.3.1. Coax-I/O

The Coax-I/O transceiver module supports two SMA connectors at the faceplate. Each connector is attached to its independent amplifier circuit, which can be configured as receiver or transmitter.

Configured as transmitter, the output signal coming from the **CLK-Module** FPGA is transmitted via a simple CMOS driver. This driver is connected to the SMA connector via AC-coupling.

The amplifier circuit first comes really into operation if configured as receiver. The receiver part is designed to be able to work with a wide range of input voltages, as well as signal forms (e.g. sine wave, rectangle).

To be independent of any DC-offset the receiver part is also connected via AC-coupling.

The main part of the amplifier is a comparator that transfers the input signal from the SMA connector into a rectangle signal with a peak-to-peak voltage of 3.3V. The signal mapping for the Coax-I/O module can be found below:

Table 2 - Coax-I/O signal mapping

Schematic Name	Script Name	Function Coax-ID
Extref1_p	EXT single ended 1	SMA_1 Rx
Extref1_n	EXT single ended 2	SMA_1 Tx
Extref2_p	EXT single ended 3	SMA_2 Rx
Extref2_n	EXT single ended 4	SMA_2 Tx

Table 3 – Coax-I/O electrical characteristics

Parameter	Min.	Typ.	Max.	Unit
Input Voltage peak to peak	0.3		5	V
Output Voltage peak to peak (with 50 Ohm sink termination)		1		V
Input Frequency	1		50M	Hz
Output Frequency	250		125M	Hz
Termination Resistance		50		Ω

4.6.3.2. RJ45-Clock-Interface

Instead of the second GbE-Port the **NAT-MCH-PHYS** can be assembled with a second RJ45 connector usable as RJ45-Clock-Interface.

Note: The second GbE-Interface is not available with this assembly option. The pin assignment of the RJ45-Clock-Interface differs from the GbE-Interface. For detailed information, please refer to chapter 0 S6: RJ45 Clock Connector.

The signals are directly connected to LVDS compliant I/Os of the clock module FPGA.

Note: Do not apply signals to this interface, which are not compliant with the LVDS signal standard!

Other External Reference Clock Transceiver Modules:

Please contact N.A.T. GmbH, if the available Clock transceiver modules or any parameter does not satisfy the needs for your application.

4.7. Interface to Extension Modules

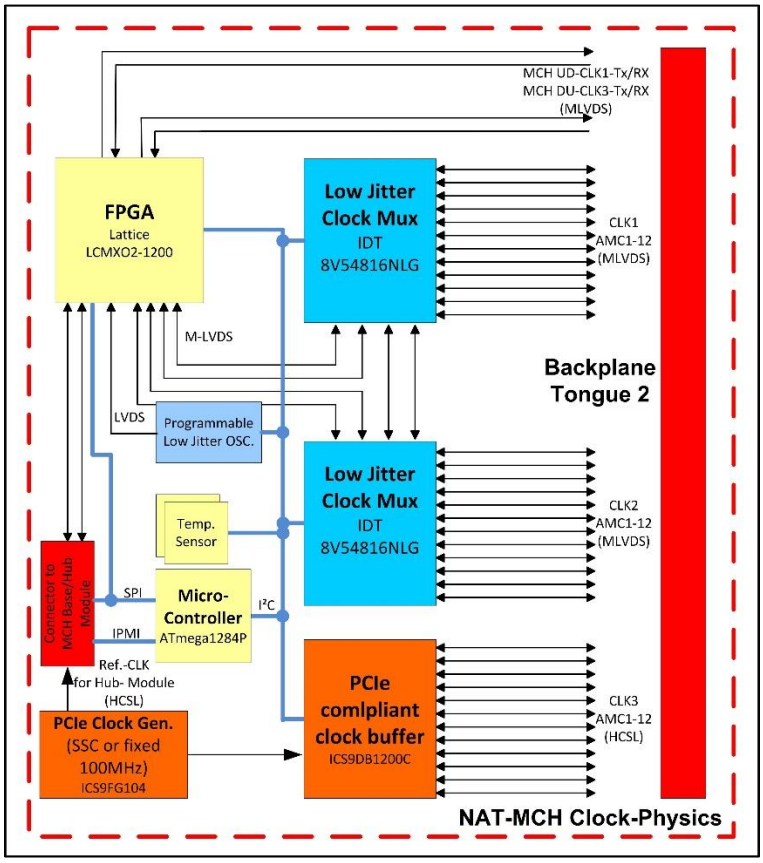
The ColdFire MCF54452 CPU interfaces the extension modules via I^2C bus or SPI interface.

4.7.1. NAT-MCH-CLK-PHYS

The **NAT-MCH-CLK-PHYS** has been developed to satisfy the demand of physics groups requiring very low jitter and low latency clock at CLK1 and CLK2, and a fixed mean 100MHZ PCIe clock. These features are realized by using a special Clock Multiplexer developed in cooperation with IDT (Integrated Device Technology Inc.).

The block diagram below illustrates the main functionality of the **NAT-MCH-CLK-PHYS**.

Figure 5 – NAT-MCH-CLK-PHYS: Block Diagram



The module is capable of sourcing an external clock from, or delivering an internal clock to two SMA inputs or outputs on the front panel. This allows installations of many MTCA systems to be synchronized to a central clock source in a very elegant and easy to use way.

Key features:

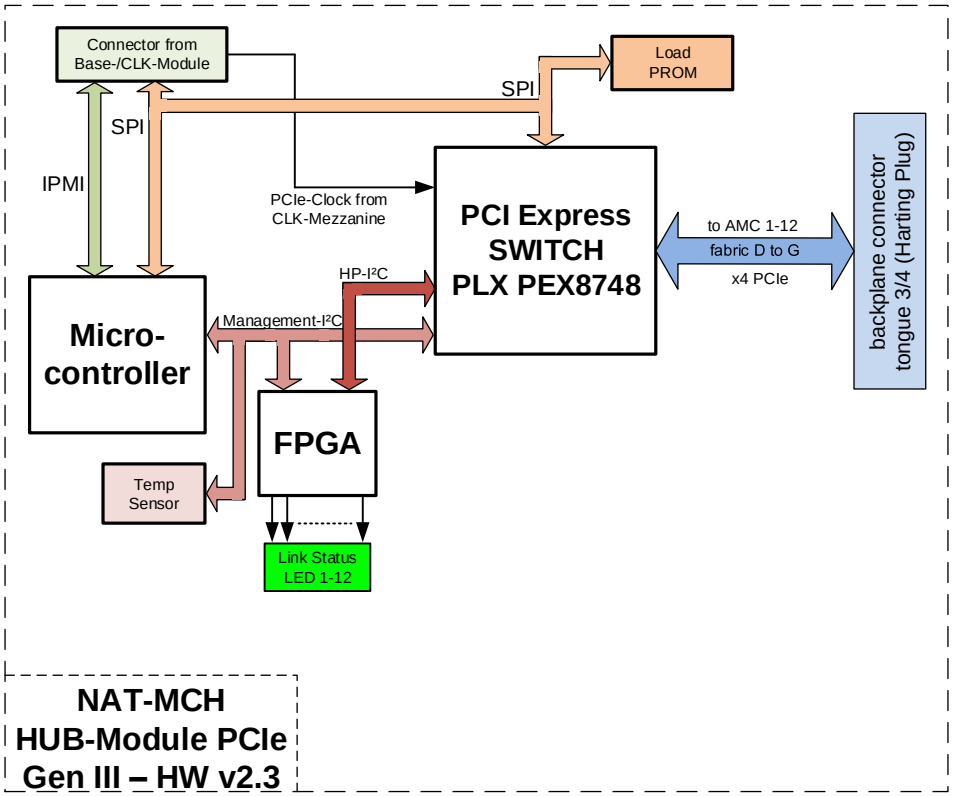
- CLK1 connections for all 12 AMC multiplexed by one device
- CLK2 connections for all 12 AMC multiplexed by one device
- Two direct multiplexer interconnections
- Fixed low jitter reference clock
- Connection to front panel clock interfaces
- PCIe reference clock distribution for 12 AMCs via CLK3 (AMC.0 R2.0 - FCLKA)

4.7.2. NAT-MCH-PCIex48 (NAT-MCH-PHYS only)

The **NAT-MCH-PCIex48** provides a 48-port PCIe Gen3 switch that allows each of the 12 AMCs in a MicroTCA.4 system to be connected by an x4 link. The PCIe switch also provides the ability to establish up to six virtual PCIe clusters and assign the AMC slots to these.

The following figure shows a block diagram of the **NAT-MCH-PCIex48**.

Figure 6 – NAT-MCH-PCIex48 – Block Diagram



The PCI Express Switching Mezzanine is an AMC.1 compliant module for the **NAT-MCH-PHYS,** that enables users to add scalable high bandwidth, non-blocking interconnection to a wide variety of applications including servers, storage, video streaming, blade servers, and embedded control products. It supports full non-transparent bridging functionality to allow implementation of multi-host systems and intelligent I/O modules.

Key Features:

- PCIe Gen 3
- Support for 12 AMC modules, Fabrics D-G
- Non-blocking switch fabric
- Upstream port configurable to any of the 12 AMC slots
- PCIe hot plug support for each AMC slot
- Secondary (failover) host possible
- Clustering support for 6 independent clusters with one configurable non-transparent upstream port; each cluster offers its own transparent upstream port
- Supports x1 and x4 width ports to any AMC
- Configuration option for Spread Spectrum Clock (SSC) or 100MHz fixed PCIe clock
- PCIe clock can be provided as Fabric Clock (FCLKA) to the AMC slots

4.7.3. NAT-MCH PCIex80-Module (NAT-MCH-PHYS80 only)

The PCIe hub module provides an 80-port PCIe Gen3 switch that allows each of the 12 AMCs in a MicroTCA.4.x system to be connected by an x4 link. An optional **NAT-MCH-RTM** is connected by an x16 link.

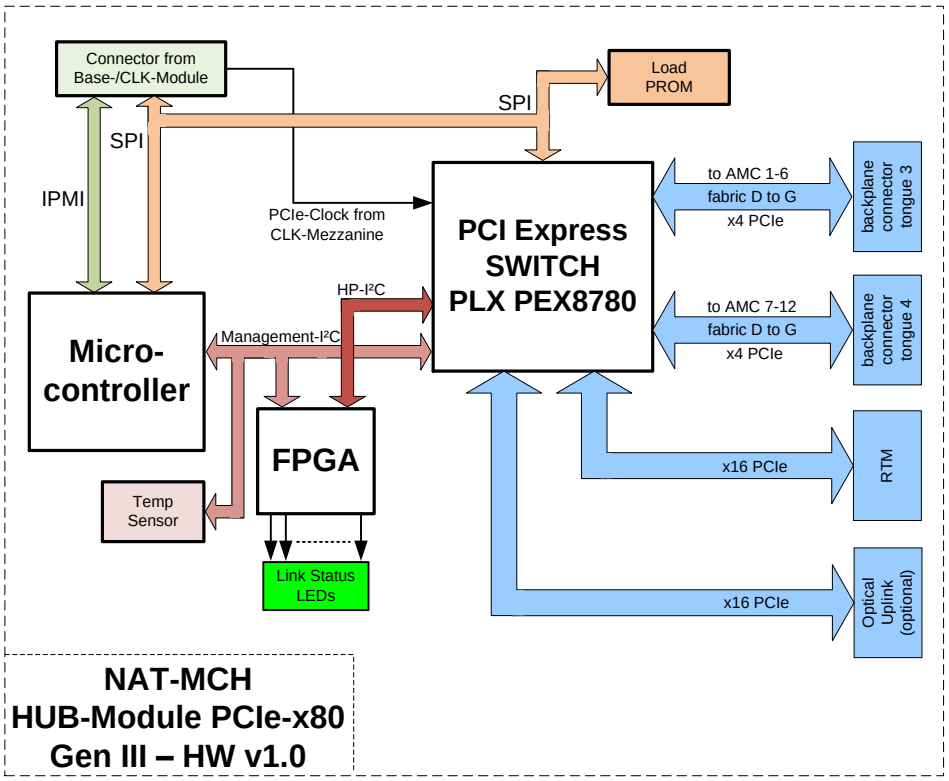
Furthermore, the **NAT-MCH-PHYS80** offers either two x8 or one x16 optional optical PCIe uplink(s) to external high performance servers or other MTCA.4 systems (product variant - **PHYS80-UPLNK**). For connecting to an external system via the front uplink ports, an optical cross-connection cable is needed. A recommendation can be found in chapter 6.3 Cable Recommendation.

The PCIe switch also accommodates higher bandwidths, i.e. x8 or x16 to a reduced number of AMC slots if the backplane provides appropriate connectivity.

Finally, the PCIe switch provides the ability to establish up to four virtual PCIe clusters and assign the AMC slots to these. The up to four PCIe Root Complexes can be any of the AMC-CPUs, the **NAT-MCH-RTM** CPU or an external PC.

The following block diagram shows the main functionality of the **NAT-MCH-PCIex80**.

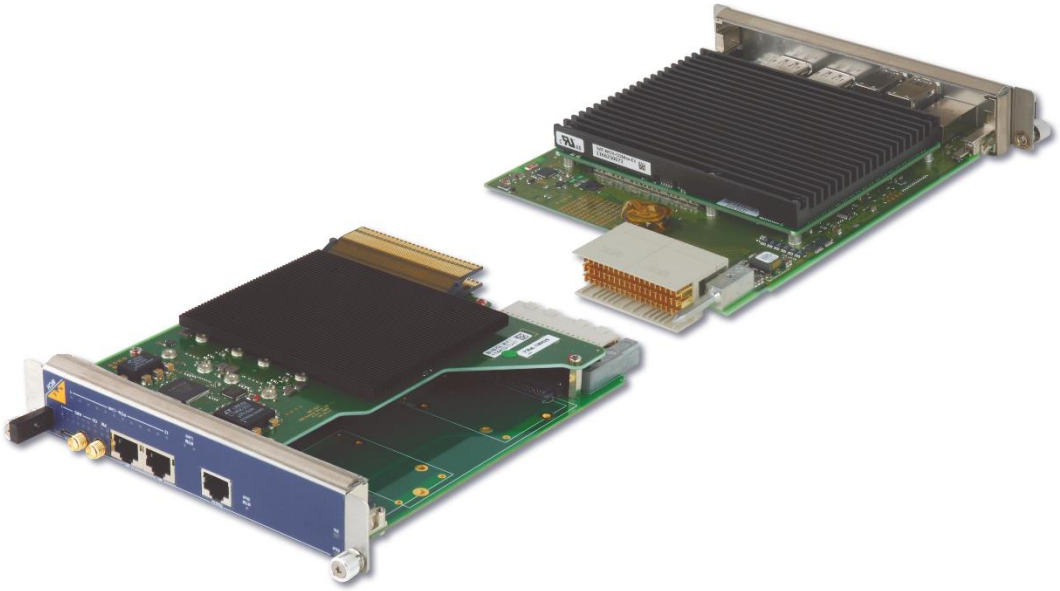
Figure 7 – NAT-MCH-PCIex80 – Block Diagram



4.8. NAT-MCH-RTM-Module (NAT-MCH-PHYS80 only)

Via its Zone3 connector, the **NAT-MCH-PHYS80** offers support for an optional RTM – for applicable variants, please check order codes listed in Table 1 – Technical Data or visit our homepage.

Figure 8 – NAT-MCH-PHYS80 with NAT-MCH-RTM



4.8.1. Power Supply and Management

The **NAT-MCH-PHYS80** provides a local generated 3.3V management power and a switched version of the MCH 12V payload power to the **NAT-MCH-RTM**. Both supplies are ramped and over-current controlled to support hot-swap. For management issues, an IPMB-L interface is supported.

4.8.2. NAT-MCH-RTM-Interfaces

The **NAT-MCH-PHYS80** features a PCIe Gen3 connection up to x16, a GbE interface, and two SATA interfaces towards the **NAT-MCH-RTM**.

If the attached **NAT-MCH-RTM** owns a Backplane Manager, the **NAT-MCH-PHYS80** can be connected to the µRTM-Backplane vie Zone2 connector and thus is able to control the µRTM-Backplane itself as well as any module connected to it, such as eRTM, RPM, or standard RTM.

For more information on the available RTMs and their features, please check the manuals and/or fact sheets available on our website.

5. HARDWARE

5.1. Front Panel and LEDs

The **NAT-MCH-PHYS** is equipped with various LEDs described in the following sections.

Figure 9 – NAT-MCH-PHYS: Front Panel

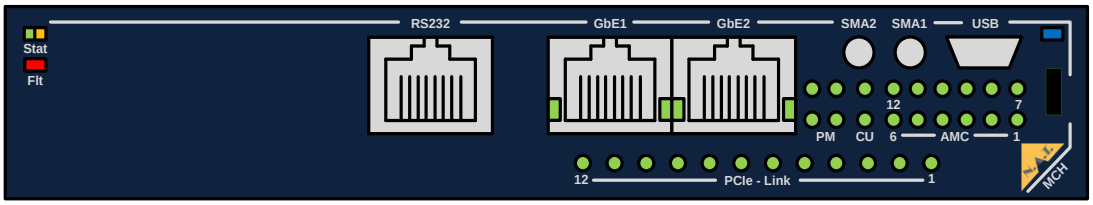


Figure 10 – NAT-MCH-PHYS80: Front Panel

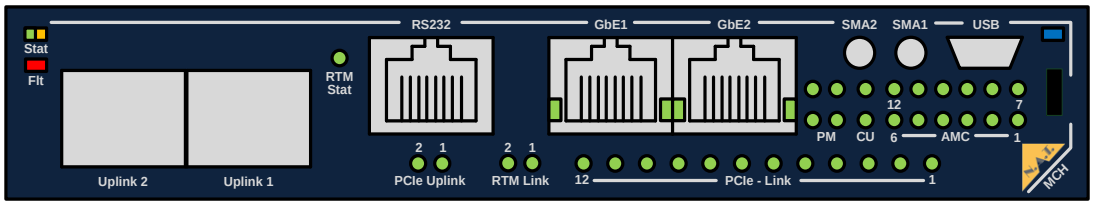


Table 4 – LED Functionality

LED	Color	Function
MCH-Status	Green	**NAT-MCH-PHYS** operates as ***primary*** MCH in the MTCA-System
	Orange	**NAT-MCH-PHYS** operates as ***secondary*** MCH in the MTCA-System
Fault	Red	Indicates MCH malfunction of the
Hot-Swap	Blue	Indicates MCH hot-swap status
RJ45	Green	Indicates GbE status
AMC / CU / PM	Green	Indicate status of 12 AMCs, 2 CUs, and 4 PMs
PCIe-Link / RTM-Link / Uplink*	Slow blink	PCIe-GEN1-Link established
	Fast flash	PCIe-GEN2-Link established
	Solid ON	PCIe-GEN3-Link established
RTM-Status	Off	No RTM present
	Green blink	Link established, no Payload Power
	Green solid ON	Link established, Payload Power ON
	Solid Red ON	No Link established / unknown RTM

Note: If the uplink is configured as one x16 connection, **LED1** represents the PCIe link status

5.2. Component-, Connector-, and Switch-Location

Figure 11 – Location Diagram – Top

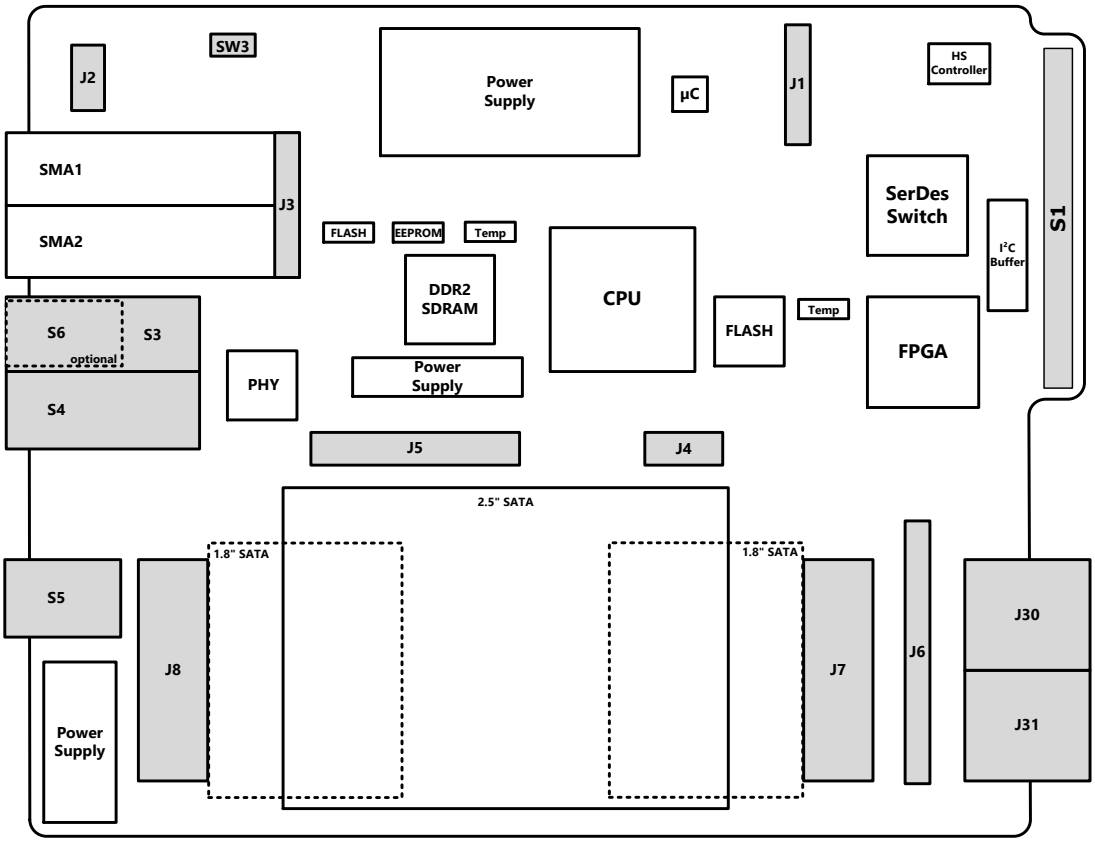
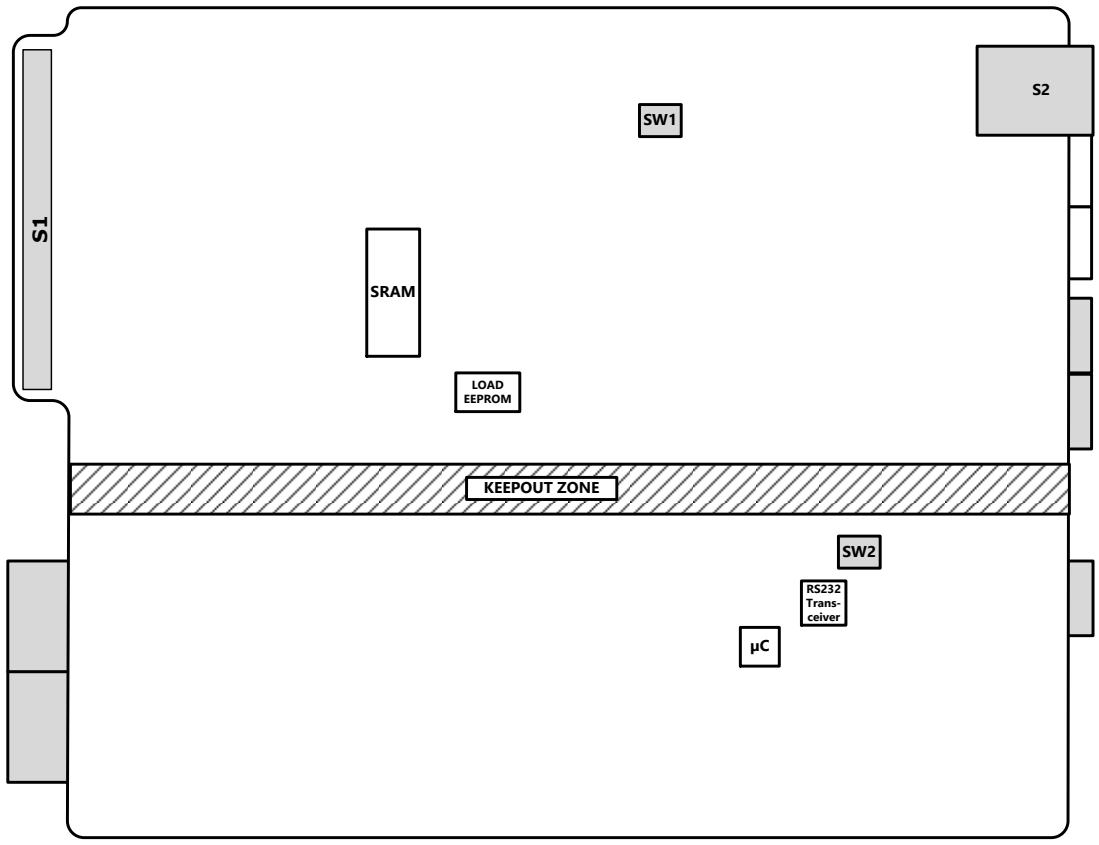


Figure 12 – Location Diagram – Bottom



Please refer to the following tables to look up the connector pin assignment of the **NAT-MCH-PHYS**.

All drawings in this chapter imply the board is orientated with the MCH Edge-Connector to the right side, or rather viewed from the front plate side. Either way, the top side of the PCB faces upwards.

5.2.1. J1: HUB-Module Connector

Connector J1 connects to the PCIex48-HUB Module (**NAT-MCH-PHYS** only) and the **NAT-MCH-CLK-PHYS**.

Figure 13 – J1: HUB-Module Connector

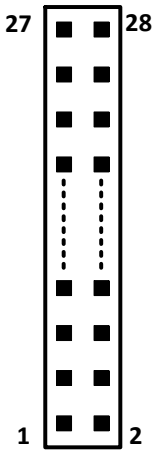


Table 5 – J1: HUB-Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	/SPISEL_CLKPCB	/INT_HUB	2
3	GND	GND	4
5	NC	NC	6
7	NC	NC	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_1_P	+3.3V MP	14
15	EXTREF_1_N	SPICLK	16
17	EXTREF_2_N	EXTREF_2_P	18
19	MOSI	MISO	20
21	GND	/SPISEL_HubPCB	22
23	HUB_SCL	/Reset_CLKPCB	24
25	HUB_SDA	/Reset_HubPCB	26
27	GND	GND	28

5.2.2. J2: LED-Module Connector

J2 connects the LED-Module via a ribbon cable.

Figure 14 – J2: LED-Module Connector

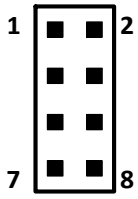


Table 6 – J2: LED-Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	/RESET_LED	2
3	+3.3V	MOSI	4
5	/SPISEL_LED	MISO	6
7	LED_MOC_PDI	SPICLK	8

5.2.3. J3: External Clock Transceiver Module Connector

J3 connects the external clock transceiver module to the **NAT-MCH-PHYS**.

Figure 15 – J2: LED-Module Connector

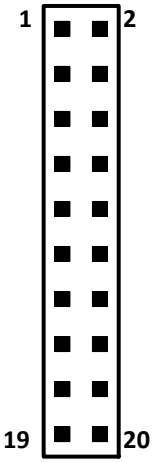


Table 7 – J3: External Clock Transceiver Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	+3.3V	2
3	EXTREF_C_P	EXTREF_CONF1	4
5	EXTREF_C_N	EXTREF_CONF2	6
7	EXTREF_A_P	EXTREF1_P	8
9	EXTREF_A_N	EXTREF1_N	10
11	EXTREF_B_P	EXTREF2_P	12
13	EXTREF_B_N	EXTREF2_N	14
15	EXTREF_D_P	EXTREF_CONF3	16
17	EXTREF_D_N	SGND	18
19	EXTREF_CONF4	GND	20

5.2.4. J4: FPGA Programming Header

J4 offers access to the programming interface of the Altera FPGA.

Figure 16 – J4: FPGA Programming Header

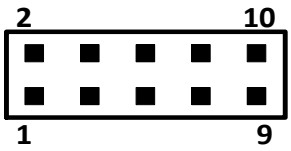


Table 8 – J4: FPGA Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	nCONFIG	/CECONF	6
7	DATA0	/CSO	8
9	ASDI	GND	10

5.2.5. J5: BDM Port / COP Header

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Figure 17 – J5: BDM Port / COP Header

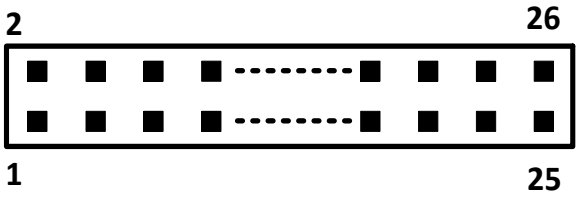


Table 9 – J5: BDM Port / COP Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	/CPU_RSTOUT	/BKPT	2
3	GND	/DSCLK	4
5	GND	SLV_TCK	6
7	/HRESET	SLV_TDI	8
9	+3.3V	CPU_TDO	10
11	GND	PST_D7	12
13	PST_D6	PST_D5	14
15	PST_D4	PST_D3	16
17	PST_D2	PST_D1	18
19	PST_D0	JTAG_EN	20
21	NC	NC	22
23	GND	PST_CLK	24
25	TMREQ	/TA	26

5.2.6. J6: PCIex80-Hub-Module Connector (NAT-MCH-PHYS80 only)

Connector J6 connects to the PCIex80-Hub-Module and is assembled on the **NAT-MCH-PHYS80** only.

Figure 18 – J6: PCIex80-Hub-Module Connector

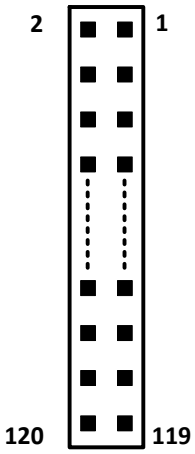


Table 10 – J6: PCIex80-Hub-Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	2
3	UpLNK_ETH0-Tx_P	UpLNK_ETH0-Rx_P	4
5	UpLNK_ETH0-Tx_N	UpLNK_ETH0-Rx_N	6
7	GND	GND	8
9	UpLNK_ETH1-Tx_P	UpLNK_ETH1-Rx_P	10
11	UpLNK_ETH1-Tx_N	UpLNK_ETH1-Rx_N	12
13	GND	GND	14
15	RTM_CON0	RTM_CON1	16
17	GND	GND	18
19	RTM-PCIe-CLK1_P	RTM-PCIe-CLK0_P	20
21	RTM-PCIe-CLK1_N	RTM-PCIe-CLK0_N	22
23	GND	GND	24
25	RTM-PCIe00_Tx_P	RTM-PCIe00_Rx_P	26
27	RTM-PCIe00_Tx_N	RTM-PCIe00_Rx_N	28
29	GND	GND	30
31	RTM-PCIe01_Tx_P	RTM-PCIe01_Rx_P	32
33	RTM-PCIe01_Tx_N	RTM-PCIe01_Rx_N	34
35	GND	GND	36
37	RTM-PCIe02_Tx_P	RTM-PCIe02_Rx_P	38
39	RTM-PCIe02_Tx_N	RTM-PCIe02_Rx_N	40
41	GND	GND	42
43	RTM-PCIe03_Tx_P	RTM-PCIe05_Rx_P	44
45	RTM-PCIe03_Tx_N	RTM-PCIe05_Rx_N	46
47	GND	GND	48

Pin #	Signal	Signal	Pin #
49	RTM-PCIe03_Rx_P	RTM-PCIe06_Rx_P	50
51	RTM-PCIe03_Rx_N	RTM-PCIe06_Rx_N	52
53	GND	GND	54
55	RTM-PCIe04_Rx_P	RTM-PCIe07_Rx_P	56
57	RTM-PCIe04_Rx_N	RTM-PCIe07_Rx_N	58
59	GND	GND	60
61	RTM-PCIe04_Tx_P	RTM-PCIe06_Tx_P	62
63	RTM-PCIe04_Tx_N	RTM-PCIe06_Tx_N	64
65	GND	GND	66
67	RTM-PCIe05_Tx_P	RTM-PCIe07_Tx_P	68
69	RTM-PCIe05_Tx_N	RTM-PCIe07_Tx_N	70
71	GND	GND	72
73	RTM-PCIe08_Rx_P	RTM-PCIe09_Rx_P	74
75	RTM-PCIe08_Rx_N	RTM-PCIe09_Rx_N	76
77	GND	GND	78
79	RTM-PCIe10_Rx_P	RTM-PCIe11_Rx_P	80
81	RTM-PCIe10_Rx_N	RTM-PCIe11_Rx_N	82
83	GND	GND	84
85	RTM-PCIe08_Tx_P	RTM-PCIe12_Rx_P	86
87	RTM-PCIe08_Tx_N	RTM-PCIe12_Rx_N	88
89	GND	GND	90
91	RTM-PCIe09_Tx_P	RTM-PCIe13_Rx_P	92
93	RTM-PCIe09_Tx_N	RTM-PCIe13_Rx_N	94
95	GND	GND	96
97	RTM-PCIe10_Tx_P	RTM-PCIe14_Rx_P	98
99	RTM-PCIe10_Tx_N	RTM-PCIe14_Rx_N	100
101	GND	GND	102
103	RTM-PCIe11_Tx_P	RTM-PCIe15_Rx_P	104
105	RTM-PCIe11_Tx_N	RTM-PCIe15_Rx_N	106
107	GND	GND	108
109	RTM-PCIe12_Tx_P	RTM-PCIe14_Tx_P	110
111	RTM-PCIe12_Tx_N	RTM-PCIe14_Tx_N	112
113	GND	GND	114
115	RTM-PCIe13_Tx_P	RTM-PCIe15_Tx_P	116
117	RTM-PCIe13_Tx_N	RTM-PCIe15_Tx_N	118
119	GND	GND	120

5.2.7. J7/J8: SATA Connectors (NAT-MCH-PHYS80 only)

Via J7 and J8, one 2.5" or two 1.8" SATA-SSDs can be installed on the **NAT-MCH-PHYS80**. As described in the tables below, J7 connects to SATA0, J8 links to SATA1.

Figure 19 – J7/J8: SATA Connectors

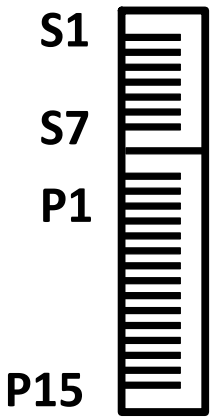


Table 11 – J7: SATA Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
S1	GND	+3.3V_SATA	P1
S2	RTM_SATA0-Rx_P	+3.3V_SATA	P2
S3	RTM_SATA0-Rx_N	+3.3V_SATA	P3
S4	GND	GND	P4
S5	RTM_SATA0-Tx_N	GND	P5
S6	RTM_SATA0-Tx_P	GND	P6
S7	GND	+5V_SATA	P7
		+5V_SATA	P8
		+5V_SATA	P9
		GND	P10
		SATA0_DSS	P11
		GND	P12
		+12V	P13
		+12V	P14
		+12V	P15

Table 12 – J8: SATA Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
S1	GND	+3.3V_SATA	P1
S2	RTM_SATA1-Rx_P	+3.3V_SATA	P2
S3	RTM_SATA1-Rx_N	+3.3V_SATA	P3
S4	GND	GND	P4
S5	RTM_SATA1-Tx_N	GND	P5
S6	RTM_SATA1-Tx_P	GND	P6
S7	GND	+5V_SATA	P7
		+5V_SATA	P8
		+5V_SATA	P9
		GND	P10
		SATA1_DSS	P11
		GND	P12
		+12V	P13
		+12V	P14
		+12V	P15

5.2.8. J30/J31: Zone3 Connectors (NAT-MCH-PHYS80 only)

J30 and J31 offer access to an optional available RTM-Module and are assembled on the **NAT-MCH-PHYS80** only.

Figure 20 – J30/J31: Zone3 Connectors

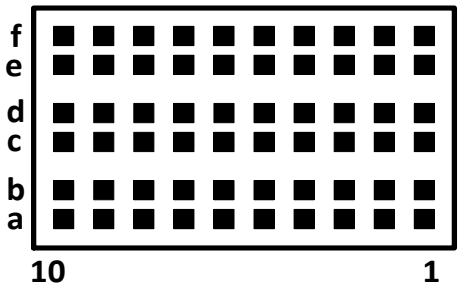


Table 13 – J30: Zone3 Connector – Pin Assignment

Col → / Row ↓	A	B	GND	C	D	GND	E	F	GND
1	RTM_PWR	RTM_PWR	GND	RTM_PS#	RTM_SDA	GND	RTM_TCK	RTM_TDO	GND
2	RTM_PWR	RTM_PWR	GND	RTM_MP	RTM_SCL	GND	RTM_TDI	RTM_TMS	GND
3	UpLNK_ ETH0-Tx_P	UpLNK_ ETH0-Tx_N	GND	RTM_ ETH0-Tx_P	RTM_ ETH0-Tx_N	GND	RTM_ PCIe00-Tx_P	RTM_ PCIe00-Tx_N	GND
4	UpLNK_ ETH0-Rx_P	UpLNK_ ETH0-Rx_N	GND	RTM_ ETH0-Rx_P	RTM_ ETH0-Rx_N	GND	RTM_ PCIe00-Rx_P	RTM_ PCIe00-Rx_N	GND
5	RTM_EN	RTM_SPICLK	GND	RTM_ SATA0-Tx_P	RTM_ SATA0-Tx_N	GND	RTM_ PCIe01-Tx_P	RTM_ PCIe01-Tx_N	GND
6	RTM_MISO	RTM_MOSI	GND	RTM_ SATA0-Rx_P	RTM_ SATA0-Rx_N	GND	RTM_ PCIe01-Rx_P	RTM_ PCIe01-Rx_N	GND
7	RTM_SPISEL0n	RTM_SIPSEL1n	GND	RTM_ SATA1-Tx_P	RTM_ SATA1-Tx_N	GND	RTM_ PCIe02-Tx_P	RTM_ PCIe02-Tx_N	GND
8	RTM_IO1_0	RTM_IO1_1	GND	RTM_ SATA1-Rx_P	RTM_ SATA1-Rx_N	GND	RTM_ PCIe02-Rx_P	RTM_ PCIe02-Rx_N	GND
9	RTM_IO1_2	RTM_IO1_3	GND	RTM_ UART-TxD	RTM_ UART-RxD	GND	RTM_ PCIe03-Tx_P	RTM_ PCIe03-Tx_N	GND
10	RTM_IO1_4	RTM_IO1_5	GND	RTM_ PCIe-CLK0_P	RTM_ PCIe-CLK0_N	GND	RTM_ PCIe03-Rx_P	RTM_ PCIe03-Rx_N	GND

Table 14 – J31: Zone3 Connector – Pin Assignment

Col → / Row ↓	A	B	GND	C	D	GND	E	F	GND
1	RTM_IO1_6	RTM_IO1_7	GND	RTM_ PCIe04-Rx_P	RTM_ PCIe04-Rx_N	GND	RTM_ PCIe05-Rx_P	RTM_ PCIe05-Rx_N	GND
2	RTM_IO2_0	RTM_IO2_1	GND	RTM_ PCIe06-Rx_P	RTM_ PCIe06-Rx_N	GND	RTM_ PCIe07-Rx_P	RTM_ PCIe07-Rx_N	GND
3	RTM_IO2_2	RTM_IO2_3	GND	RTM_ PCIe04-Tx_P	RTM_ PCIe04-Tx_N	GND	RTM_ PCIe05-Tx_P	RTM_ PCIe05-Tx_N	GND
4	RTM_IO2_4	RTM_IO2_5	GND	RTM_ PCIe06-Tx_P	RTM_ PCIe06-Tx_N	GND	RTM_ PCIe07-Tx_P	RTM_ PCIe07-Tx_N	GND
5	RTM_IO2_6	RTM_IO2_7	GND	RTM_ PCIe08-Rx_P	RTM_ PCIe08-Rx_N	GND	RTM_ PCIe09-Rx_P	RTM_ PCIe09-Rx_N	GND
6	RTM_ PCIe08-Tx_P	RTM_ PCIe08-Tx_N	GND	RTM_ PCIe10-Rx_P	RTM_ PCIe10-Rx_N	GND	RTM_ PCIe11-Rx_P	RTM_ PCIe11-Rx_N	GND
7	RTM_ PCIe09-Tx_P	RTM_ PCIe09-Tx_N	GND	RTM_ PCIe12-Rx_P	RTM_ PCIe12-Rx_N	GND	RTM_ PCIe13-Rx_P	RTM_ PCIe13-Rx_N	GND
8	RTM_ PCIe10-Tx_P	RTM_ PCIe10-Tx_N	GND	RTM_ PCIe14-Rx_P	RTM_ PCIe14-Rx_N	GND	RTM_ PCIe15-Rx_P	RTM_ PCIe15-Rx_N	GND
9	RTM_ PCIe-CLK1_P	RTM_ PCIe-CLK1_N	GND	RTM_ PCIe11-Tx_P	RTM_ PCIe11-Tx_N	GND	RTM_ PCIe12-Tx_P	RTM_ PCIe12-Tx_N	GND
10	RTM_ PCIe15-Tx_P	RTM_ PCIe15-Tx_N	GND	RTM_ PCIe14-Tx_P	RTM_ PCIe14-Tx_N	GND	RTM_ PCIe13-Tx_P	RTM_ PCIe13-Tx_N	GND

5.2.9. S1: MCH Connector (Zone1)

Figure 21 – S1: MCH-Connector (top view)

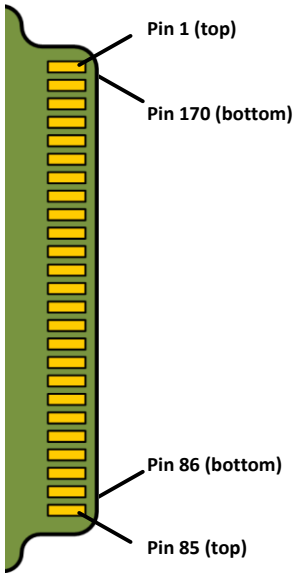


Table 15 – S1: MCH-Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	GND	PWR_ON	170
2	PWR	NC	169
3	/PS1	NC	168
4	MP	NC	167
5	GA0	NC	166
6	RESVD	NC	165
7	GND	GND	164
8	RESVD	TxFA-1+	163
9	PWR	TxFA-1-	162
10	GND	GND	161
11	TxFUA+	RxFA-1+	160
12	TxFUA-	RxFA-1-	159
13	GND	GND	158
14	RxFUA+	TxFA-2+	157
15	RxFUA-	TxFA-2-	156
16	GND	GND	155
17	GA1	RxFA-2+	154
18	PWR	RxFA-2-	153
19	GND	GND	152
20	TxFA-3+	TxFA-4+	151
21	TxFA-3-	TxFA-4-	150
22	GND	GND	149

Pin #	Signal	Signal	Pin #
23	RxFA-3+	RxFA-4+	148
24	RxFA-3-	RxFA-4-	147
25	GND	GND	146
26	GA2	TxFA-6+	145
27	PWR	TxFA-6-	144
28	GND	GND	143
29	TxFA-5+	RxFA-6+	142
30	TxFA-5-	RxFA-6-	141
31	GND	GND	140
32	RxFA-5+	TxFA-8+	139
33	RxFA-5-	TxFA-8-	138
34	GND	GND	137
35	TxFA-7+	RxFA-8+	136
36	TxFA-7-	RxFA-8-	135
37	GND	GND	134
38	RxFA-7+	/TMREQ	133
39	RxFA-7-	RSVD	132
40	GND	GND	131
41	/ENABLE	I2C_SCL	130
42	PWR	I2C_SDA	129
43	GND	GND	128
44	TxFA-9+	IPMB0-SCL-A	127
45	TxFA-9-	IPMB0-SDA-A	126
46	GND	GND	125
47	RxFA-9+	IPMB0-SCL-B	124
48	RxFA-9-	IPMB0-SDA-B	123
49	GND	GND	122
50	TxFA-10+	IPMBL-SCL-1	121
51	TxFA-10-	IPMBL-SDA-1	120
52	GND	GND	119
53	RxFA-10+	IPMBL-SCL-2	118
54	RxFA-10-	IPMBL-SDA-2	117
55	GND	GND	116
56	SCL_L	IPMBL-SCL-3	115
57	PWR	IPMBL-SDA-3	114
58	GND	GND	113
59	TxFA-11+	IPMBL-SCL-4	112
60	TxFA-11-	IPMBL-SDA-4	111
61	GND	GND	110
62	RxFA-11+	IPMBL-SCL-5	109
63	RxFA-11-	IPMBL-SDA-5	108
64	GND	GND	107
65	TxFA-12+	IPMBL-SCL-6	106
66	TxFA-12-	IPMBL-SDA-6	105
67	GND	GND	104
68	RxFA-12+	IPMBL-SCL-7	103
69	RxFA-12-	IPMBL-SDA-7	102
70	GND	GND	101
71	SDA_L	IPMBL-SCL-8	100

Pin #	Signal	Signal	Pin #
72	PWR	IPMBL-SDA-8	99
73	GND	GND	98
74	XOVER0+	IPMBL-SCL-9	97
75	XOVER0-	IPMBL-SDA-9	96
76	GND	GND	95
77	XOVER1+	IPMBL-SCL-10	94
78	XOVER1-	IPMBL-SDA-10	93
79	GND	GND	92
80	XOVER2+	IPMBL-SCL-11	91
81	XOVER2-	IPMBL-SDA-11	90
82	GND	GND	89
83	/PS0	IPMBL-SCL-12	88
84	PWR	IPMBL-SDA-12	87
85	GND	GND	86

5.2.10. S2: USB Debug Connector

S2 features a Micro-USB Debug Interface towards the Coldfire-CPU of the **NAT-MCH-PHYS**.

Figure 22 – S2: USB Debug Connector

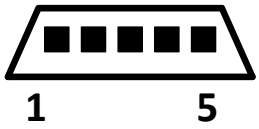


Table 16 – S2: USB Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	USB_VBUS	USB_D_N	2
3	USB_D_P	USB_ID_1	4
5	USB_GND	SGND	6
7	nc	SGND	8
9	SGND	SGND	10
11	SGND		

5.2.11. S3/S4: RJ45 Ethernet Connectors

S3 and S4 provide Gigabit Ethernet towards the front plate.

Figure 23 – S3/S4: RJ45 Ethernet Connectors

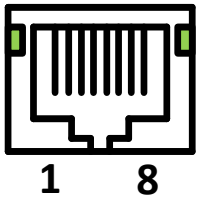


Table 17 – S3/S4: RJ45 Ethernet Connectors – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MX0+	MX0-	2
3	MX1+	MX2+	4
5	MX2-	MX1-	6
7	MX3+	MX3-	8

5.2.12. S5: RJ45 Debug Connector

The **NAT-MCH-PHYS** features an RS232 Debug interface via an RJ45 connector.

Figure 24 – S5: RJ45 Debug Connector

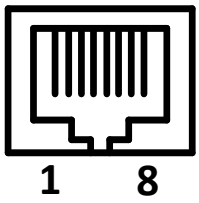


Table 18 – S5: RJ45 Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	nc	nc	2
3	nc	RS232_GND	4
5	RS232_Rx	RS232_Tx	6
7	nc	nc	8

5.2.13. S6: RJ45 Clock Connector

As an assembly option, the **NAT-MCH-PHYS** offers a clock interface via an RJ45 connector.

Note: With this assembly option, the second GbE port is ***not available!***

Figure 25 – S6: RJ45 Clock Connector

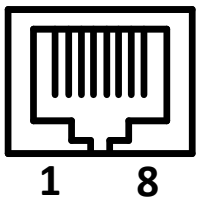


Table 19 – S6: RJ45 Clock Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	EXTREF_C_P	EXTREF_C_N	2
3	EXTREF_B_P	EXTREF_A_P	4
5	EXTREF_A_N	EXTREF_B_N	6
7	EXTREF_D_P	EXTREF_D_N	8

5.2.14. SW1: General Settings

SW1-1 offers the option to deactivate USB console support.

SW1-2 can be used to prevent the **NAT-MCH-PHYS** from loading the firmware and to force the board to stop in the bootloader. This feature can be useful e.g. if the firmware is corrupt.

The tables below provide information on the operating parameters and configuration options of SW1.

Figure 26 – SW1: General Settings

Table 20 – SW1 – Operating Parameters

Switch #	Function
SW1-1	On: USB console deactivate ***OFF: USB console active***
SW1-2	On: force bootloader ***OFF: normal booting***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.2.15. SW2: SATA Active (NAT-MCH-PHYS80 only)

SW2 is used to inform the **NAT-MCH-PHYS80**, if a SATA device is present or not; there is no other (auto-) detecting mechanism. Basically the MCMC will request more power, if a SATA device is present.

The tables below provide information on the operating parameters and configuration options of SW2.

Figure 27 – SW2: SATA

Table 21 – SW2 – Operating Parameters

Switch #	Function
SW2-1	ON: SATA0 present ***OFF: SATA not present***
SW2-2	ON: SATA1 present ***OFF: SATA1 not present***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.2.16. SW3: Hot Swap Switch

Switch SW3 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

- **NAT-MCH** User's Manual:
  https://www.nateurope.com/manuals/nat_mch_man_usr.pdf
- **NAT-MCH** Ethernet Switch:
  https://www.nateurope.com/manuals/nat_mch_ethx_man_usr.pdf
- **NAT-MCH-CLK-PHYS**:
  https://www.nateurope.com/manuals/nat_mch_clk_phys_man_hw.pdf
- **NAT-MCH-PCIex48:**
  https://www.nateurope.com/manuals/nat_mch_pciex48_v2x_man_hw.pdf
- **NAT-MCH-PCIex80:**
  https://www.nateurope.com/manuals/nat_mch_pciex80_v1x_man_hw.pdf
- **NAT-MCH-RTM**:
  https://www.nateurope.com/manuals/nat_mch_rtm_ComEx_HWv22_23.pdf
- Application:
  https://www.nateurope.com/documents/SS_High_Energy_Physics.pdf

6.2. External Reference Documentation

- Freescale MCF5445x ColdFire Microprocessor Data Sheet, Rev. 8, 02/2012
- Intel/Altera Cyclone Device Handbook Volume 1, V1.3, 05/2008
- Broadcom BCM5461S 10/100/1000Base-T Gigabit Ethernet Transceiver, 5461-PB05-R, 04/2006

6.3. Cable Recommendation

NAT recommends the use of the following optical uplink cable:

Sylex 1x24f MTP(F) to 1x24f MTP(F) 24-fiber OM3 ruggedized trunk cable, Polarity X (Order Code: 1-610-610-248-6GB/B0/XXXX)

Datasheet:
https://www.sylex.sk/wp-content/uploads/2018/11/1x24f-MTP-to-1x24f-MTP-24-fiber-trunk-cable.pdf

Drawing/Polarity:
https://www.sylex.sk/wp-content/uploads/2018/09/Polarities_for_24-fiber_MTP_assemblies.pdf

6.4. Standards Compliance

- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- PICMG AMC.2 Rev. 1.0
- PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)
- IPMI Specification v1.5 Rev. 1.0
- PICMG µTCA.0 Rev. 1.0
- PICMG MicroTCA.4 Rev. 1.0

6.5. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.6. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the

supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.7. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.8. Product Safety

The board complies with EN60950 and UL1950.

6.9. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7. ABBREVIATION LIST

Table 22 – Abbreviation List

Abbreviation	Description
AC	Alternating Current
AMC	Advanced Mezzanine Card
API	Application Programming Interface
BDM	Background Debug Mode
CMOS	Complementary Metal-Oxide-Semiconductor
COM Express	Computer-On-Module Express
CPU	Central Processing Unit
CU	Cooling Unit
DC	Direct Current
DDR3 SDRAM	Double Data Rate Synchronous Dynamic RAM
DESY	Deutsches Elektronen-Synchrotron
DMA	Direct Memory Access
DSPI	SPI with DMA capability
ECC	Error Correcting Code
EEPROM	Electrically Erasable PROM
EMAC	Enhanced Multiply-Accumulate
eRTM	extended RTM
FCLK	Fabric Clock
FEC	Forward Error Correction
FLASH	Non-Volatile Memory
FLASH	Free Electron LASer - DESY facility
FPGA	Field Programmable Gate Array
FPU	Floating-Point Unit
GbE	Gigabit Ethernet
GBIC	Gigabit Interface Converter
GUI	Graphical User Interface
HCSL	High Speed Current Steering Logic
HPI	Hardware Platform Interface
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
LLRF	Low Latency Radio Frequency
LVDS	Low Voltage Differential Signaling
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MCMC	MicroTCA Carrier Management Controller
MCH	µTCA/MTCA Carrier Hub
MII	Media Independent Interface
MIPS	Microprocessor without interlocked pipeline stages
MMU	Module Management Unit
PCI(e)	Peripheral Component Interconnect (Express)

Abbreviation	Description
PM	Power Module
(P)ROM	(Programmable) Read Only Memory
RAM	Random Access Memory
RMCP	Remote Management Control Protocol
RPM	Rear Power Module
RTM	Rear Transition Module
SATA	Serial Advanced Technology Attachment
SerDes	Serializer/Deserializer
SMA	SubMiniature version A
SNMP	Simple Network Management Protocol
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SRAM	Static RAM
SSC	Spread Spectrum Clock
SSD	Solid State Drive
TTL	Transistor–Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPN	Virtual Private Network
XFEL	X-Ray Free Electron Laser - DESY facility

8. DOCUMENT'S HISTORY

Table 23 – Document's History

Rev	Date	Description	Author
1.0	11.12.2018	initial release	Se
	19.02.2019	Photos updated	se
	26.03.2019	Added cable recommendation information	se
	19.02.2020	Updated Block Diagrams Minor Changes	se
1.1	24.03.2020	Updated SSD-Information	Se
	15.09.2020	Updated Figure 6 – NAT-MCH-PCIex48 – Block Diagram Minor changes	se