NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.3
HUB-Module PCIe HW Revision 2.3-2.5

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x.
The following table gives a list of the abbreviations used in this document:

Table 1: **List of used Abbreviations**

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Introduction

The **NAT-MCH** consists of a **BASE-Module**, which can be expanded with additional PCBs. The **BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB-Modules** are available. With the **CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

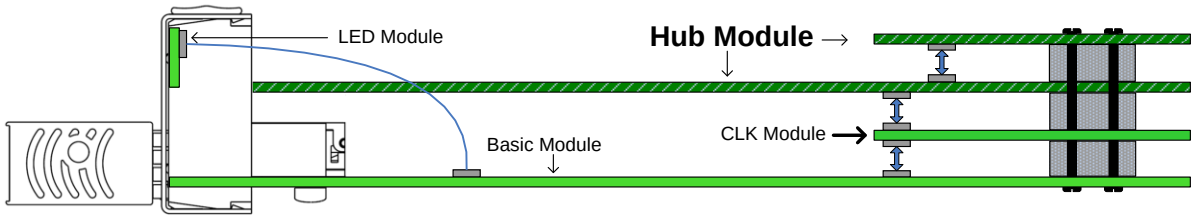
Through the extension of the **NAT-MCH** with a **HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in the following figure

Figure 1: **Arrangement of different NAT-MCH Modules**



This Technical Reference Manual describes the **NAT-MCH HUB-Module PCIe**. In addition to the **CLK-Module** it can be mounted on the **NAT-MCH BASE-Module**. With the **NAT-MCH HUB-Module PCIe** the 3rd tongue and 4th tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed.

2 Overview

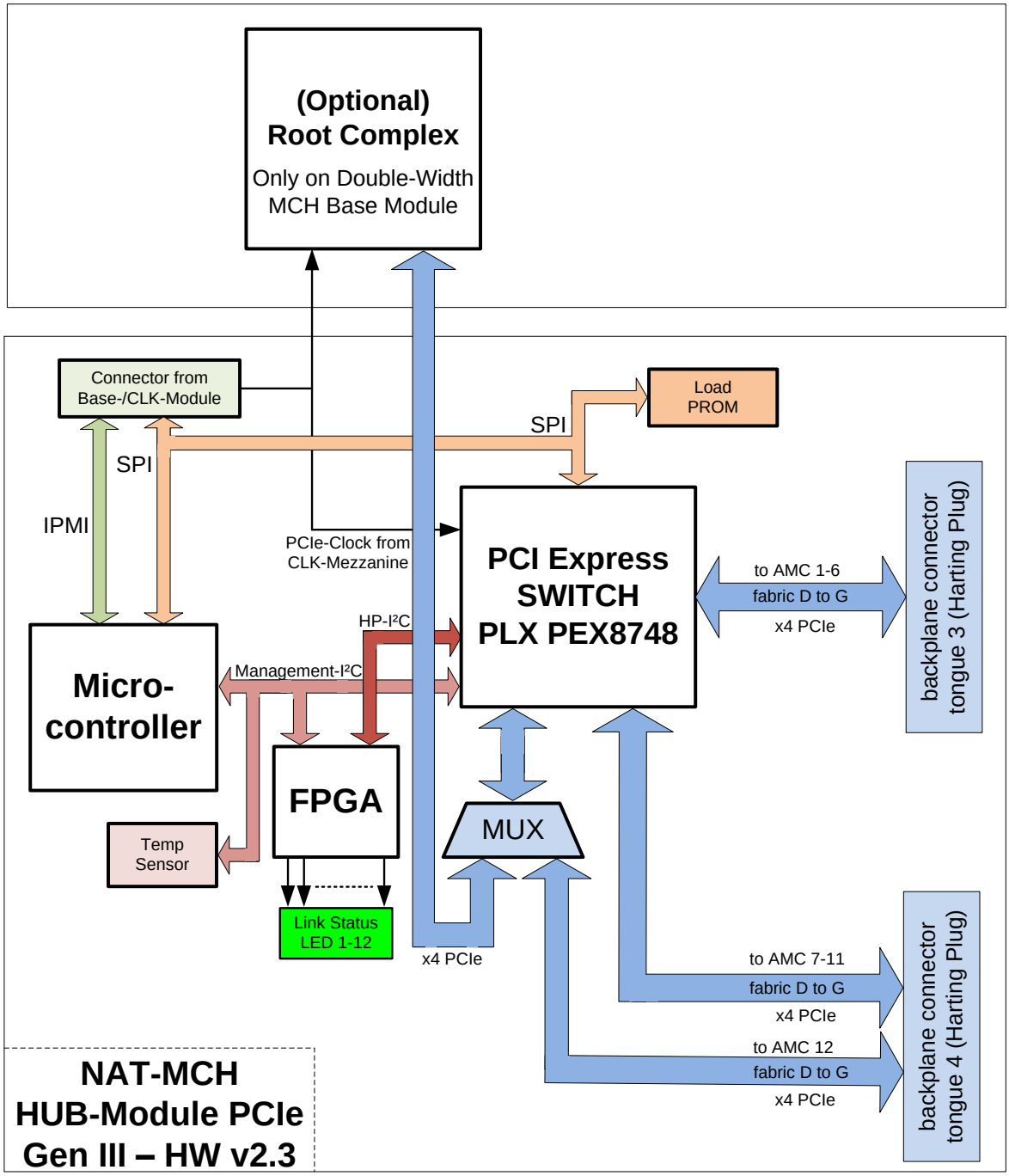
2.1 Major Features

- PLX PEX8748 PCI Express switch
  - connection to AMC 1-6 (via 3rd tongue) and to AMC 7-12 (via 4th tongue)
  - non-blocking switching at full line rate
  - Quality of Service (QoS)
  - 2 virtual cannels and 8 traffic classes per port supported
  - Configuration of one of all 12 AMC ports as transparent and non-transparent upstream port each
- Atmel ATmega1284 microcontroller
  - Configuration of PCIe switch
  - Support of Hot-Swap functionality
- Lattice MachXO2 FPGA
  - Support of Hot-Plug functionality for each AMC-Slot
- Two PI3PCIE3412 multiplexing units
  - Connection to AMC 12 (via 4th tongue)
  - Switching between AMC 12 and optional Root Complex (double-width **NAT-MCH BASE-Module** only)
- PCIe x1 and x4 switching function
  - Connection of fabrics D to G of up to 6 AMCs (**NAT-MCH HUB-Module PCIe x24)**
  - Connection of fabrics D to G of up to 12 AMCs (**NAT-MCH HUB-Module PCIe x48)**
  - Connection to optional Root Complex (double-width **NAT-MCH BASE-Module** only)
- Clustering support – up too six clusters can be operated individually, each having its own Root Complex
- PCIe compliant Spread Spectrum Clocking

2.2 Block Diagram

The following figure shows a block diagram of the **NAT-MCH HUB-Module PCIe**.

Figure 2: **Figure 1: NAT-MCH HUB-Module PCIe – Block Diagram**



2.3 Location Diagram

The following location diagram of the **NAT-MCH HUB-Module PCIe** shows the position of important components.

Figure 3: **NAT-MCH HUB-Module PCIe – Location Diagram (top)**

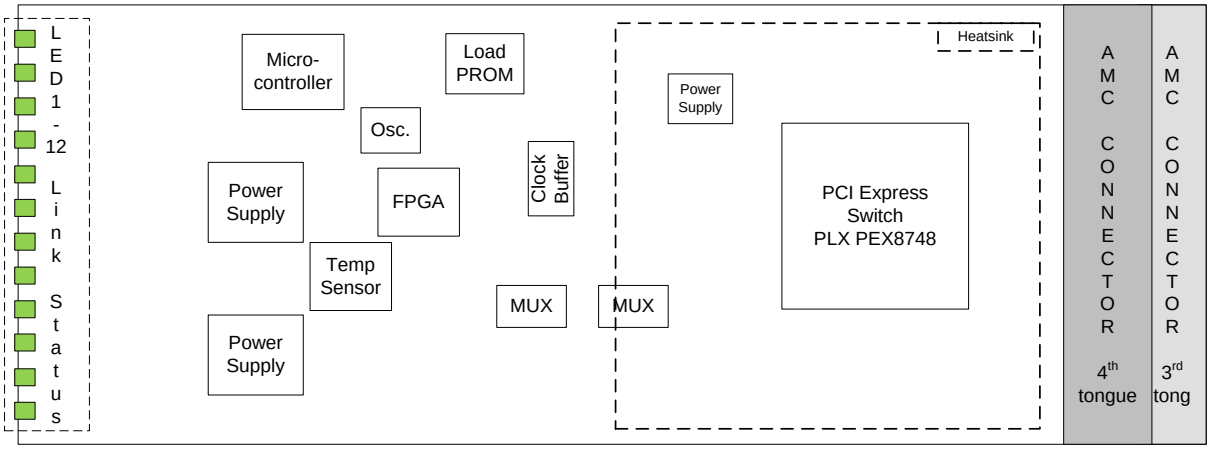
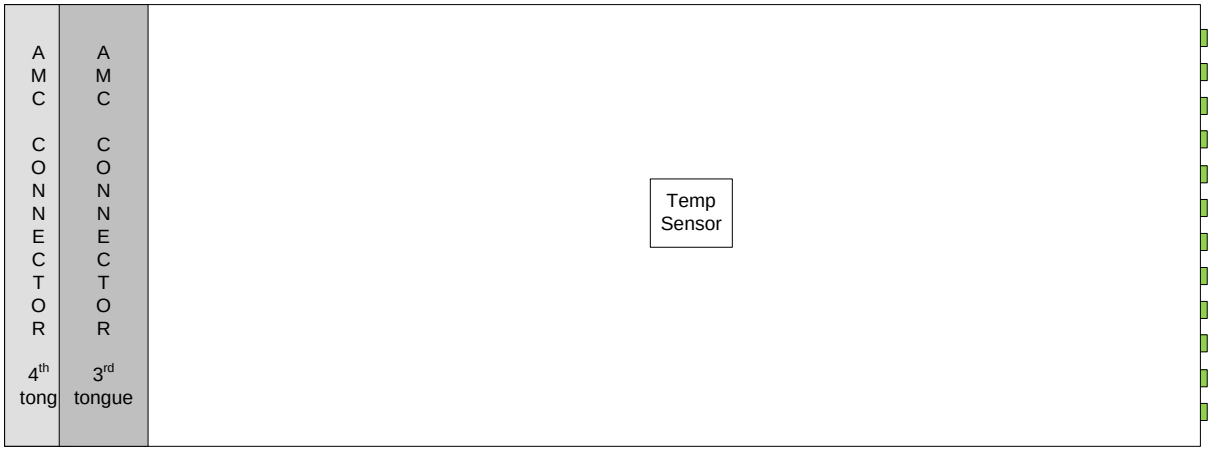


Figure 4: **NAT-MCH HUB-Module PCIe – Location Diagram (bottom)**



3 Board Features

The **NAT-MCH HUB-Module PCIe** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 PCI Express Switch PLX PEX8748

The **NAT-MCH HUB-Module PCIe** is equipped with a PLX PEX8748 PCI Express switch, which provides non-blocking switching at full line rate. Quality of Service (QoS) is provided by the PEX8748, supporting 2 virtual cannels and 8 traffic classes per port. One of all ports can be configured as transparent upstream port, and one of all ports can be configured as non-transparent upstream port.

The PCI Express Switch PEX8748 can be configured by strapping pins, by loading an EEPROM, or by PCI Express messages from a host. A standard configuration is done by the microprocessor and resistors by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.
These standard settings can be changed by reading the EEPROM after a reset, or by receiving PCI Express messages from a host.
The EEPROM contains basic configuration information for the PCIe switch as well as user settings, e.g. upstream port settings. The user settings can be changed by the CPU on the **NAT-MCH BASE-Module**.

The /PERST pin is also connected to the microcontroller. The value of this pin can also be controlled by programming a register in the microcontroller.

The PLX PEX8748 supports 12 ports, per default with 4 lanes (PCIe x4). As shown in the following tables a certain switch port is not constrained to the according AMC port or MCH fabric.

Table 2: **PCIe Switch Lane to MCH Fabric Port Mapping**

Switch Lanes	MCH Fabric
0	G-4
1	F-4
2	E-4
3	D-4
4	G-3
5	F-3
6	E-3
7	D-3
8	G-2
9	F-2
10	E-2
11	D-2
12	G-1
13	F-1
14	E-1
15	D-1

Switch Lanes	MCH Fabric
16	D-5
17	E-5
18	F-5
19	G-5
20	D-6
21	E-6
22	F-6
23	G-6
24	D-11
25	E-11
26	F-11
27	G-11
28	D-12 / Root Complex (opt.)
29	E-12 / Root Complex (opt.)
30	F-12 / Root Complex (opt.)
31	G-12 / Root Complex (opt.)
32	G-10
33	F-10
34	E-10
35	D-10
36	G-9
37	F-9
38	E-9
39	D-9
40	G-8
41	F-8
42	E-8
43	D-8
44	G-7
45	F-7
46	E-7
47	D-7

Table 3: **Switch Lanes to AMC port mapping for X4-Link on a standard MicroTCA-Backplane**

Switch Port (Lanes)	AMC Slot #
0 (0 – 3)	4
1 (4 – 7)	3
2 (8 – 11)	2
3 (12 – 15)	1
8 (16 – 19)	5
9 (20 – 23)	6
10 (24 – 27)	11
11 (28 – 31)	12 / Root Complex (opt.)
16 (32 – 35)	10
17 (36 – 39)	9
18 (40 – 43)	8
19 (44 – 47)	7

3.2 Microcontroller

For configuration of the PCIe switch and for providing hot-swap functionality, an 8-bit Atmel microcontroller resides on the **NAT-MCH HUB-Module PCIe**. The microcontroller can be updated by the CPU on the **NAT-MCH BASE-Module** via SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages over the I²C interface.

The strapping options and the reset signal of the switch can be controlled by programming registers in the microcontroller. Also the PCIe Hot-Plug signals can be served by the microcontroller.

Furthermore, three temperature sensors are connected to a second I²C bus of the microcontroller. The microcontroller makes these sensors accessible to the CPU on the **NAT-MCH BASE-Module** via IPMI.

3.3 FPGA

The Lattice MachXO2 FPGA is used to emulate a set of I^2C port expanders that the PLX switch normally uses to extend its pins for PCIe Hotplug support on all ports. The FPGA implements an I^2C interface towards the PLX switch and behaves as if there were 12 I^2C port expenders connected.
Further it implements a second interface towards the Atmel µC, so that the Hotplug signals finally can be exchanged with the MCH main firmware.

3.4 Multiplexing Units

There are two PCIe Gen3 compliant multiplexing chips (each can switch two lanes) used to switch the four lanes going towards AMC12 to the double-width **NAT-MCH BASE-Module.** From the **BASE-Module** these lanes connect to an optional PCIe-capable module connected as RTM to the double-width **BASE-Module**.

3.5 PCIe Interfaces

The **NAT-MCH HUB-Module PCIe** implements interfaces to connect fabrics D to G of up to 12 AMCs or an optional Root Complex, which is only available on a double-width **NAT-MCH BASE-Module**, instead of the 12th AMC.

3.6 Interface to NAT-MCH BASE-Module

The Microcontroller on the **NAT-MCH HUB-Module PCIe** can be updated by the CPU on the **NAT-MCH BASE-Module** via SPI interface. Normal communication between Microprocessor and CPU is done by IPMI messages via I²C interface.
A configuration EEPROM for the PCIe Switch resides on the **NAT-MCH HUB-Module PCIe**. This EEPROM can be programmed / updated by the CPU of the **NAT-MCH BASE-Module** via SPI interface.

3.7 Interface to NAT-MCH CLK-Module

The **NAT-MCH CLK-Module** can provide the 100 MHz PCI Express compliant clock signal to the **NAT-MCH HUB-Module PCIe**.

4 Hardware

4.1 LEDs

The **NAT-MCH HUB-Module PCIe** features 12 green LEDs which reflect the PCIe Link Status. They can take the following states:

Table 4: **LED State – Link Status**

LED(1-12) State	Link Status
OFF	No PCIe link established
SLOW BLINK (1 blink/second)	PCIe GEN1 Link (2.5 GBaud)
FAST BLINK (2 blinks/second)	PCIe GEN2 Link (5 GBaud)
SOLID ON	PCIe GEN3 (8 GBaud)

4.2 Connectors

Figure 5: **NAT-MCH HUB-Module PCIe – Connectors (top)**

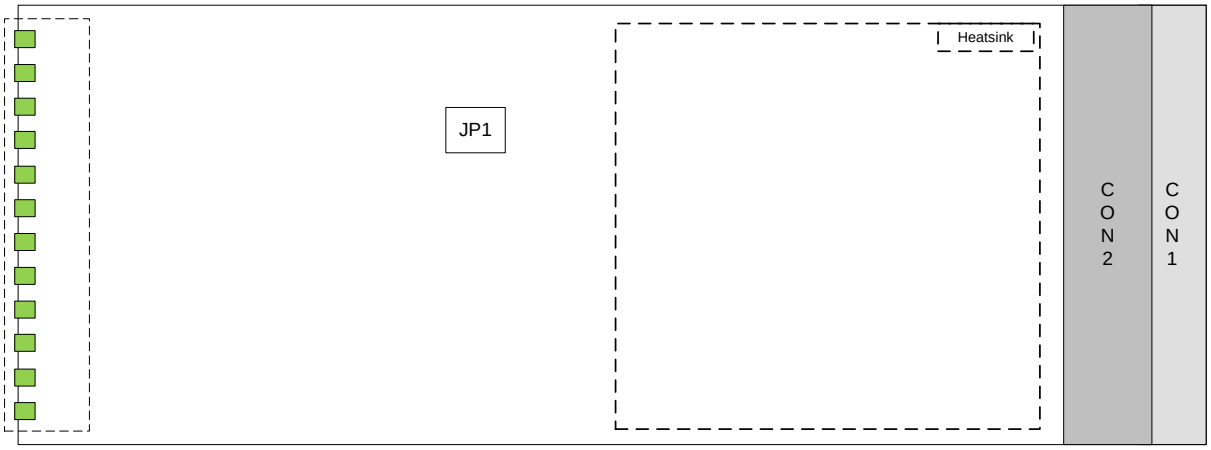
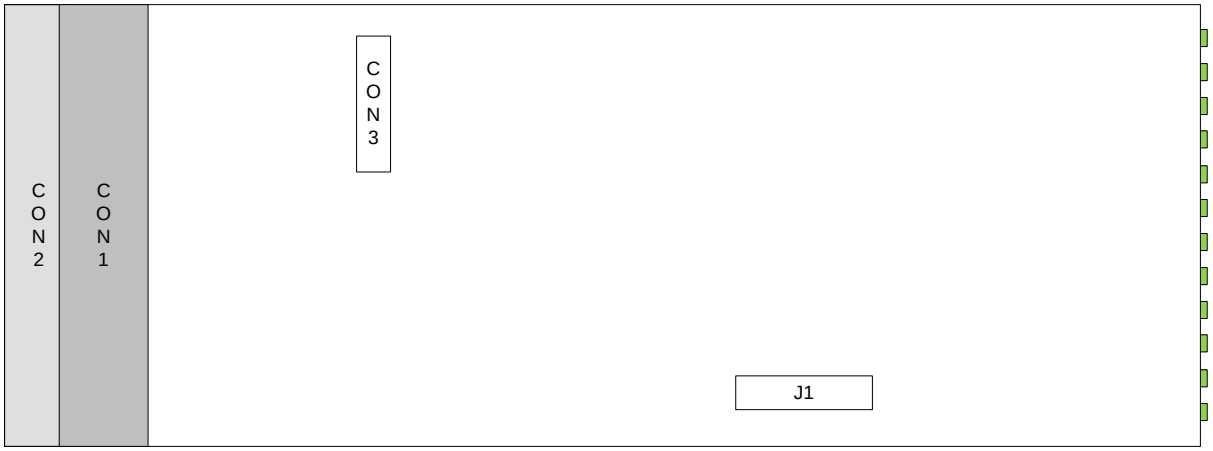


Figure 6: **NAT-MCH HUB-Module PCIe – Connectors (bottom)**



Please refer to the following tables to look up the pin assignment of the **NAT-MCH HUB-Module PCIe**.

4.2.1 CON1: AMC Connector to 3rd tongue

Table 5: **CON1: AMC Connector to 3rd tongue – Pin Assignment**

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

4.2.2 CON2: AMC Connector to 4th tongue

Table 6: **CON2: AMC Connector to 4th tongue – Pin Assignment**

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

4.2.3 CON3: Connector to NAT-MCH CLK/BASE-Module

Table 7: **CON3: Connector to NAT-MCH CLK/BASE-Module – Pin Assignment**

Pin #	Signal	Signal	Pin #
1	INT1	INT2	2
3	GND	GND	4
5	NC	NC	6
7	NC	NC	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK HUB_P	NC	14
15	PCIeCLK HUB_N	SPICLK	16
17	GND	NC	18
19	MOSI	MISO	20
21	GND	/SPISEL HUBPCB	22
23	SCL	NC	24
25	SDA	/RESET HUBPCB	26
27	GND	GND	28

CON3 connects to the **NAT-MCH CLK-Module**; on the **CLK-Module** these signals are routed via another connector to the **NAT-MCH BASE-Module**.

4.2.4 JP1: JTAG programming interface

The JTAG programming interface is for development use only and not intended to be used by the customer.

4.2.5 J1: Connector to optional Root-Complex

Table 8: **J1: Connector to optional Root-Complex – Pin Assignment**

Pin #	Signal	Signal	Pin #
1	UP-LNK CON	GND	2
3	GND	RxFD-UP_LNK_P	4
5	GND	RxFD-UP_LNK_N	6
7	TxFD-UP_LNK_P	GND	8
9	TxFD-UP_LNK_N	GND	10
11	GND	RxFE-UP_LNK_P	12
13	GND	RxFE-UP_LNK_N	14
15	TxFE-UP_LNK_P	GND	16
17	TxFE-UP_LNK_N	GND	18
19	GND	RxFF-UP_LNK_P	20
21	GND	RxFF-UP_LNK_N	22
23	TxFF-UP_LNK_P	GND	24
25	TxFF-UP_LNK_N	GND	26
27	GND	RxFG-UP_LNK_P	28
29	GND	RxFG-UP_LNK_N	30
31	TxFG-UP_LNK_P	GND	32
33	TxFG-UP_LNK_N	GND	34
35	GND	RxCLK-UP_LNK_P	36
37	TxCLK-UP_LNK_P	RxCLK-UP_LNK_N	38
39	TxCLK-UP_LNK_N	GND	40

Please note that the Root-Complex is optional and only available with the double-width **NAT-MCH BASE-Modules**.

5 Programming Notes

5.1 SPI Interface

The SPI interface on the **NAT-MCH HUB-Module PCIe** can be connected in two different ways.

5.1.1 SPI-Interface – Default mode

In Default mode the SPI interface establishes a connection between the CPU on the **BASE-Module** and the Atmel microcontroller for maintenance purposes, e.g. microcontroller firmware update.
At the same time the PCIe Switch PEX8748 is connected to the load PROM.

5.1.2 SPI-Interface – Update mode

In Update mode the SPI Bus connects the CPU on the **BASE-Module** with the load PROM. In this case data is read from or written to the PROM.

5.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **NAT-MCH BASE-Module**. All communication is based on IPMI messages.

5.3 Register

A register interface is implemented in the Atmel microcontroller. With the help of this interface different functions can be controlled and various identification values can be read.

5.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH HUB-Module PCIe**.

Table 9: **Board Identifier Register**

Board Identifier - Address 0x00								
Default value 0xb7								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**BOARD_ID**							

5.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH HUB-Module PCIe**.

Table 10: **PCB Revision Register**

PCB Revision - Address 0x01								
Default value 0x23								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**PCB_REV**							

5.3.3 Atmel Version

The Atmel Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH HUB-Module PCIe**.

Table 11: **Atmel Revision Register**

Atmel Version - Address 0x02								
Default value 0x12								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**Atmel_vers**							

6 Board Specification

Table 12: **NAT-MCH HUB-Module PCIe Features**

Power Consumption	12V / 1.6A max. (only **NAT-MCH HUB-Module PCIe x48**)
Operating Temperature	0°C – +50°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PCI Express Base Specification Rev. 1.1 PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification v2.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH HUB-Module PCIe** during its usual life-time take refer to the safety note section of the **NAT-MCH BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires a **NAT-MCH BASE-Module** and a **NAT-MCH CLK-Module** where the **NAT-MCH HUB-Module PCIe** can be mechanically fixed on to. The **NAT-MCH HUB-Module PCIe** must be completely connected and joined to the complete PCB stack (**BASE-Module** and **CLK-Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH HUB-Module PCIe** must meet the following specifications:

- +12 V / 1.6 A max. (**NAT-MCH HUB-Module PCIe x48** only – in addition to other PCBs of the **NAT-MCH**).

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] ExpressLane PEX_8748-BA 48-Lane, 12-Port PCI Express Gen 3 Multi-Root Switch Data Book v0.85 02Mar11

Appendix B: Document's History

Revision	Date	Description	Author
1.0	27.07.2011	initial revision	SE
1.1	23.05.2013	Adapted to HW 2.3 Adapted to new layout	SE
1.2	24.09.2013	Adaption to new layout completed Typo correction Update Pin Assignment J1	se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	SE
1.3	23.04.2015	Updated chapter 7.3 WEEE-Directive	ks