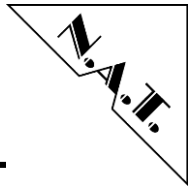
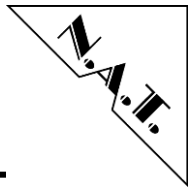


NAT-MCH
Clock-Module
Technical Reference Manual V 1.3
CLK-Module HW Version 4.1



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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1: gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
B	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Introduction

The **NAT-MCH** consists of a **NAT-MCH BASE-Module**, which can be expanded with additional PCBs. The **NAT-MCH BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **NAT-MCH BASE-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **NAT-MCH CLK-Module** and different **NAT-MCH HUB-Modules** are available. With the **NAT-MCH CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs and a second MCH
- reception of clock signals from either of 12 AMCs, a second MCH or from the front panel input and redistribution

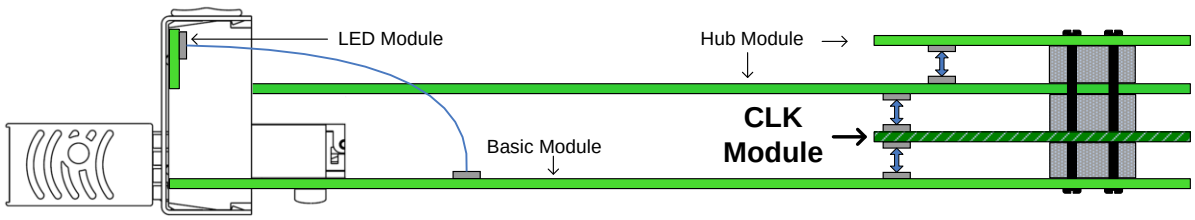
Through the extension of the **NAT-MCH** with a **NAT-MCH HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **NAT-MCH HUB-Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown below.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **NAT-MCH CLK-Module**. With the **NAT-MCH CLK-Module**, the 2nd tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed.

2 Overview

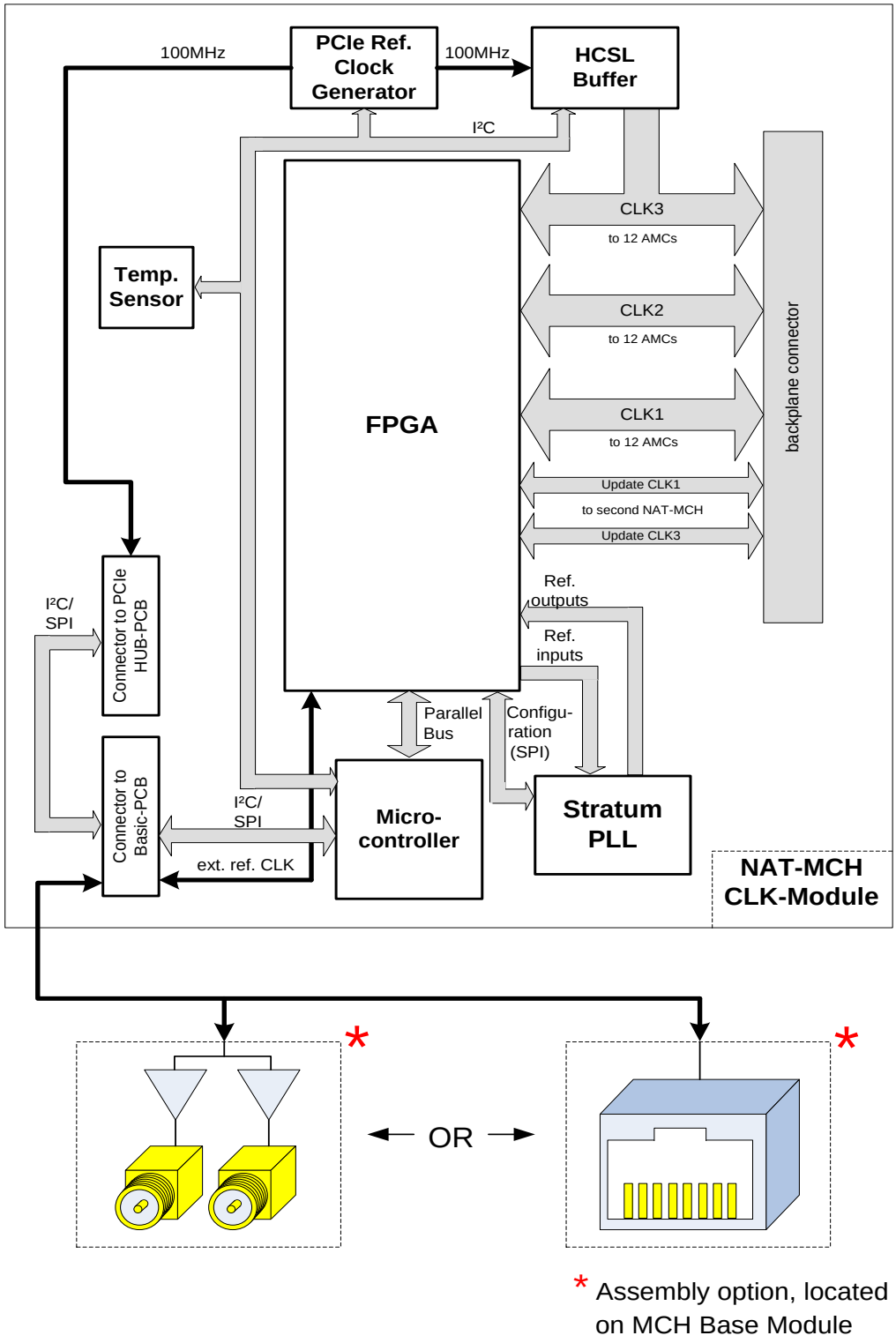
2.1 Major Features

- support of AMC clocks CLK1* CLK2* and CLK3* for up to 12 AMCs
- support of update CLK1 and CLK3 for a second **NAT-MCH** in a redundant system
- support of two front panel reference clock In/Outputs
- Stratum 3 or 3E (depending on assembly option) type PLL clock source for telecom applications with various output frequencies
- Telecom CLK signals can be distributed over all backplane clock connections and the front panel interface
- CLK1, CLK2 and CLK3 from all 12 AMCs, the update clocks from a second **NAT-MCH**, or a signal from the front panel interface can be used as reference for the PLL
- a PCI Express compliant clock signal can be distributed via CLK3 to all 12 AMCs Support of M-LVDS **or** HCSL compliant driver and termination for CLK3 (assembly option)

* Please refer to **Appendix A**: Correlation between MicroTCA and AMC Clock Naming for a brief description of the correlation between the MicroTCA and AMC clock interface naming

2.2 Block Diagram

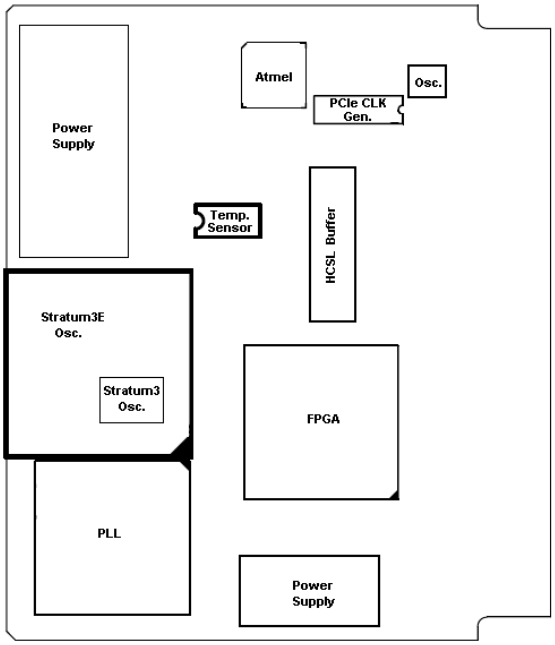
Figure 2: NAT-MCH CLK-Module – Block Diagram



2.3 Location Diagram

The following location diagram of the **NAT-MCH CLK-Module** shows the position of important components. Depending on the chosen options it may be that the board does not include all components named in the location diagram.

Figure 3: NAT-MCH CLK-Module – Location Diagram



3 Board Features

The **NAT-MCH CLOCK-Module** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 Stratum PLL

The board is equipped with a Maxim DS31400 Stratum 2/3E/3 PLL, which provides various typical telecom frequencies in the range from 1Hz to 725 MHz. Especially 8 kHz and 19.44 MHz, which are recommended for telecom applications by the MicroTCA Specification, are supported. Also 10MHz and 30.72MHz that are often needed for GPS applications are in the supported range.

The DS31400 supports the requirements of Stratum 2, 3E, 3, 4E and 4, G.812 Types I-IV, G.813 and G.8262. Although the PLL supports the requirements of Stratum2 this mode is not available on the **CLK-Module** due to assembly restrictions. The standard assembly variant is to have an oscillator fulfilling Stratum 3 requirements onboard; on demand an oscillator fulfilling Stratum 3E could be assembled.
Note: The component height of this Stratum 3E oscillator would prevent the usage of any **HUB-Module** on the **NAT-MCH**!

The eight reference clock inputs and the tree frame-sync inputs of the DS31400 are connected to the FPGA. Via multiplexers in the FPGA it can be decided which source shall be routed to those inputs. By setting up the PLL it can be chosen which of the two integrated high performance DPLLs shall synchronize on which reference input. The two DPLLs can independently lock on any frequency from 2kHz up to 725MHz and on a frame-sync of 2kHz, 4kHz, 8kHz.
In addition to that a special mode for synchronization to 1Hz (1pps) signals is supported.

By programming the FPGA multiplexers, any clock signal from any AMC (either CLK1, CLK2 or CLK3), from the other **NAT-MCH** (CLK1 or CLK3 update) or from the face plate interface can be connected to these reference inputs of the PLL.
If no reference signal is available or if the reference fails the DS31400 uses a 12.8 MHz master clock for frequency generation in a free running/holdover mode. The 12.8 MHz clock is generated by an oscillator.

The DS31400 has seven clock and two frame sync outputs. These outputs are routed to the FPGA and can there be selected as source by any multiplexer.
A digital frequency synthesizer (DFS) is available for every clock output. Each DFS can be slave to either DPLL and generate any 2kHz multiple up to 77,76MHz.

Furthermore the DS31400 supports three APLLs that can be used in addition to the DFS. With the help of the APLL nearly every frequency between 1Hz and 725MHz can be generated. As another advantage the APLLs produce a very low output jitter.

The frame pulse outputs can generate a 2kHz and/or a 8kHz frame pulse with programmable polarity and pulse-width. The frame pulses can be disciplined by the frame sync inputs.

Note: The DS31400 PLL is only assembled if the TC-Option is chosen.

Please refer to the manual of the DS31400 PLL [1] for a more detailed description.

3.2 Microprocessor

For configuration purposes an Atmel 8-bit microprocessor resides on the **NAT-MCH CLK-Module**. With the help of this microprocessor, the main CPU of the base board can configure all multiplexers implemented in the FPGA and enable the transceivers for the connection to each AMC. The firmware can be updated by the CPU of the **NAT-MCH BASE-Module** via the SPI interface. The base board CPU communicates with the **NAT-MCH CLK-Module** via IPMI (using the I²C interface).

3.3 CLOCK-Multiplex Function

Flexible multiplexing of the various clock signals is achieved by a Lattice FPGA. Multiplexing of source clock signals to destination clock signals is performed by programming a register interface provided by the microcontroller.

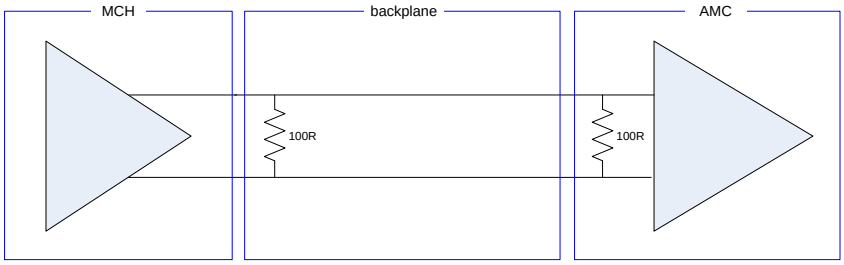
Note: The FPGA with these multiplexers is only assembled with the TC-option.

3.4 M-LVDS / HCSL Transceiver

The MicroTCA R1.0 Specification recommends that all clock interfaces are equipped with M-LVDS compliant driver/receiver and termination. Contrary to that the AMC.0 R2.0 allows for FCLKA (formerly CLK3) also HCSL compliant driver/receiver and termination.

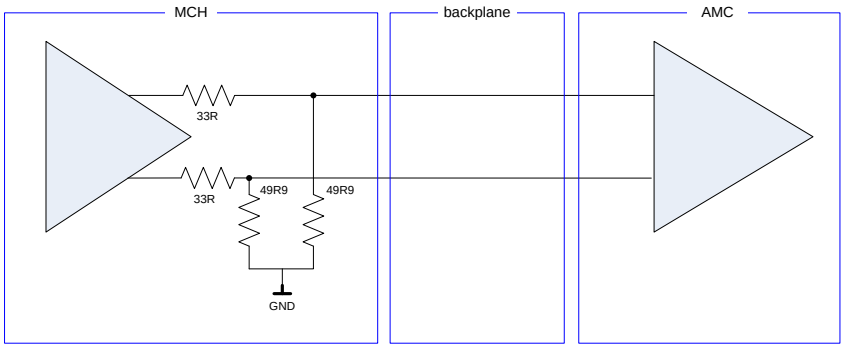
The main difference between the two signal specifications is the different termination which makes it difficult to realize both with the same hardware: M-LVDS uses a dual differential termination between the two complimentary clock lines at both ends of the bus. This termination is shown in Figure 4.

Figure 4: M-LVDS Termination



HCSL uses a source-only termination with two series and term-to-ground resistors. This termination is depicted in Figure 5.

Figure 5: HCSL termination



Because of this differences N.A.T. decided to offer two different assembly/ordering options, SSCM (Spread Spectrum Clock M-LVDS) and SSCH (Spread Spectrum Clock HCSL). The SSCM option implements M-LVDS compliant transmitter and termination for CLK3, the SSCH option implements HCSL compliant transmitter and termination.

Either the SSCM or the SSCH option can be chosen. Beside these two options always the TC option can additionally be chosen. The TC option implements always M-LVDS compliant transceiver and termination for CLK1, CLK2 and Update CLK1/3.

Note: It is important that not only the **CLK-Module** and the AMC modules fit together regarding the termination, also the backplane needs to be selected adequate.
The backplane shall have a 100Ohm termination if M-LVDS is chosen for CLK3 (refer to Figure 4). If HCSL is chosen for CLK3 the backplane shall have no termination (refer to Figure 5).

3.5 PCIe compliant reference clock generation

If the **NAT-MCH** is equipped with a **HUB-Module PCIe** the 100MHz PCIe reference clock will be generated by that module. In that case the **NAT-MCH CLK-Module** will only distribute that clock.

If the **NAT-MCH** is not equipped with a **HUB-Module PCIe** it might be nevertheless necessary to distribute a PCIe compliant 100MHz reference clock. For those cases the **NAT-MCH CLK-Module** can be equipped with a clock generator (ICS9FG104) that is compliant to the PCIe Gen I and Gen II requirements. This clock generator supports also the PCIe compliant spread spectrum clock (SSC) mode.

(In systems that follow the scope approach, the PCIe endpoints are connected directly via the backplane without using the switch on the **NAT-MCH**. In those systems often a PCIe reference clock is missing.)

3.6 Clock Interfaces

3.6.1 CLK Interfaces

The **NAT-MCH CLK-Module** implements clock interfaces to 12 AMCs.

3.6.1.1 CLK1 and CLK2

These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any of the 12 AMCs.

3.6.1.2 CLK3

Depending on the assembly option different signal standards are supported:

- The M-LVDS option supports M-LVDS compliant in- or outputs.
- The HCSL option supports HCSL compliant outputs, as recommended for a PCIe reference clock.

3.6.2 Update CLK

The **NAT-MCH CLK-Module** implements 2 update channels (update CLK1 and CLK3). These channels are full-duplex connections to a second **NAT-MCH**. They can only be used to send and receive telecom clock signals (not the PCI Express clock signal).

3.6.3 External Reference CLK

Reference clock signals can be received or transmitted by a dual external reference clock in- or output, accessible via connectors on the **NAT-MCH** face plate. The required signals are routed to the **NAT-MCH BASE-Module** where different clock transceiver modules can be assembled.
The available transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL) and the supported connector. At the moment the following external clock transceiver modules are available:

3.6.3.1 Coax-IO

The Coax-IO transceiver module supports two SMA connectors at the face plate. Each connector is connected to its independent amplifier circuit. Each amplifier circuit can be configured as receiver or transmitter.

Configured as transmitter the output pin of the Clock Module FPGA is connected to the SMA connector via AC-coupling without additional amplifier.

The amplifier circuit first comes really into operation if configured as receiver. The receiver part is designed to be able to work with a wide range of input voltages, as well as signal forms (e.g. sine wave, rectangle...). To be independent of any DC-offset the receiver part is also connected via AC-coupling.
The main part of the amplifier is a comparator that transfers the input signal from the SMA connector into a rectangle signal with a peak to peak voltage of 3.3V. Refer to the following table Table 2: for the electrical characteristics.

Table 2: Coax-IO Electrical characteristics

Parameter	Min.	Typ.	Max.	Unit
Input Voltage peak to peak	0.3		5	V
Output Current		16		mA
Input Frequency	1		50M	Hz
Termination Resistance		50		Ω

3.6.3.2 RJ45-Clock

The RJ45 Clock uses the second RJ45 connector at the **NAT-MCH** face plate for the clock interface instead of the Ethernet uplink.

The following table Table 3: shows how the pins of the second RJ45 connector are assigned if the RJ45-Clock is used.

Table 3: 2nd Face Plate RJ45 for RJ45 Clock – Pin Assignment

Pin #	Signal	Signal	Pin #
1	N.C.	N.C.	2
3	Extref2_p	Extref1_p	4
5	Extref1_n	Extref2_n	6
7	N.C.	N.C.	8

The signals are directly connected to LVDS compliant IOs of the **NAT-MCH CLK-Module** FPGA. To prevent damage, do not apply signals to this interface that are not compliant with the MLVDS signal standard!

3.6.3.3 Other External Reference Clock Transceiver Modules

Please contact N.A.T. GmbH if the available Clock transceiver modules do not satisfy the needs for your application.

3.7 Interfaces to other NAT-MCH Modules

3.7.1 NAT-MCH BASE-Module

The Microprocessor on the **NAT-MCH CLK-Module** can be programmed by the CPU on the **NAT-MCH BASE-Module** via a SPI interface. Normal communication between the Microprocessor and the CPU is done by IPMI messages via the I²C interface.
The external clock interface on the front panel is connected to the **NAT-MCH CLK-Module** via the interface to the **NAT-MCH BASE-Module** (via connector CON2).

3.7.2 NAT-MCH-HUB-Module PCIe

Depending on the **HUB-Module** version the **NAT-MCH CLK-Module** can receive a PCI Express compliant clock signal from the **NAT-MCH HUB-Module** or transmit that clock signal to the **NAT-MCH HUB-Module**.

4 Hardware

4.1 Connectors

The following figures show the position of the different connectors of the **NAT-MCH CLK-Module**.

Figure 6: NAT-MCH CLK-Module – Connectors (top)

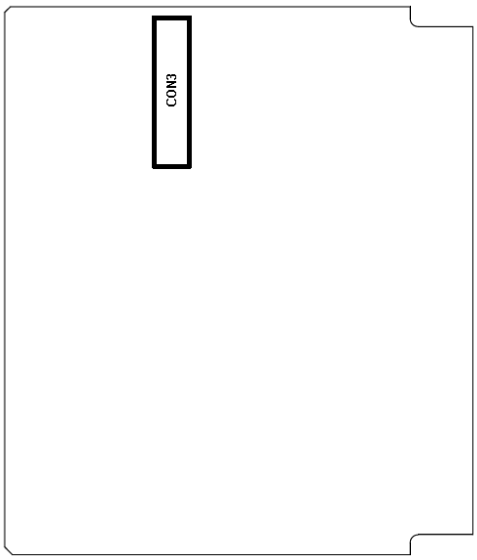
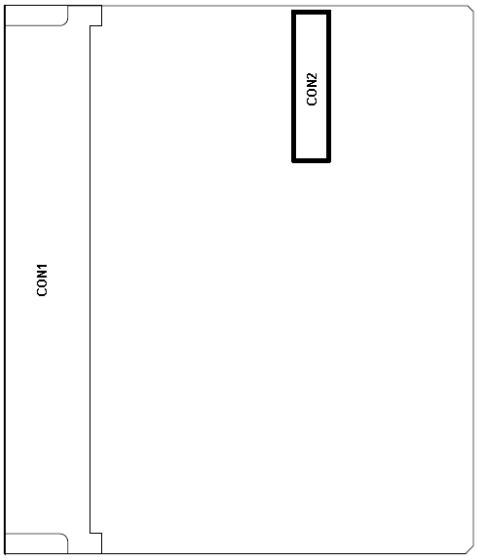


Figure 7: NAT-MCH CLK-Module – Connectors (bottom)



Please refer to the following tables for the pin assignment of the **NAT-MCH CLK - Module**.

4.1.1 CON1: NAT-MCH Connector

Table 4: CON1: MCH Connector – Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	CLK3_Tx+	CLK3_Rx+	163
9	CLK3_Tx-	CLK3_Rx-	162
10	GND	GND	161
11	CLK1_Tx+	CLK1_Rx+	160
12	CLK1_Tx-	CLK1_Rx-	159
13	GND	GND	158
14	TxFB-1+	RxFB-1+	157
15	TxFB-1-	RxFB-1-	156
16	GND	GND	155
17	TxFB-2+	RxFB-2+	154
18	TxFB-2-	RxFB-2-	153
19	GND	GND	152
20	TxFB-3+	RxFB-3+	151
21	TxFB-3-	RxFB-3-	150
22	GND	GND	149
23	TxFB-4+	RxFB-4+	148
24	TxFB-4-	RxFB-4-	147
25	GND	GND	146
26	TxFB-5+	RxFB-5+	145
27	TxFB-5-	RxFB-5-	144
28	GND	GND	143
29	TxFB-6+	RxFB-6+	142
30	TxFB-6-	RxFB-6-	141
31	GND	GND	140
32	CLK3-1+	CLK3-7+	139
33	CLK3-1-	CLK3-7-	138
34	GND	GND	137
35	CLK3-2+	CLK3-8+	136
36	CLK3-2-	CLK3-8-	135
37	GND	GND	134
38	CLK3-3+	CLK3-9+	133
39	CLK3-3-	CLK3-9-	132
40	GND	GND	131
41	CLK3-4+	CLK3-10+	130
42	CLK3-4-	CLK3-10-	129
43	GND	GND	128
44	CLK3-5+	CLK3-11+	127
45	CLK3-5-	CLK3-11-	126
46	GND	GND	125
47	CLK3-6+	CLK3-12+	124

Pin #	MCH-Signal	MCH-Signal	Pin No.
48	CLK3-6-	CLK3-12-	123
49	GND	GND	122
50	CLK1-1+	CLK2-1+	121
51	CLK1-1-	CLK2-1-	120
52	GND	GND	119
53	CLK1-2+	CLK2-2+	118
54	CLK1-2-	CLK2-2-	117
55	GND	GND	116
56	CLK1-3+	CLK2-3+	115
57	CLK1-3-	CLK2-3-	114
58	GND	GND	113
59	CLK1-4+	CLK2-4+	112
60	CLK1-4-	CLK2-4-	111
61	GND	GND	110
62	CLK1-5+	CLK2-5+	109
63	CLK1-5-	CLK2-5-	108
64	GND	GND	107
65	CLK1-6+	CLK2-6+	106
66	CLK1-6-	CLK2-6-	105
67	GND	GND	104
68	CLK1-7+	CLK2-7+	103
69	CLK1-7-	CLK2-7-	102
70	GND	GND	101
71	CLK1-8+	CLK2-8+	100
72	CLK1-8-	CLK2-8-	99
73	GND	GND	98
74	CLK1-9+	CLK2-9+	97
75	CLK1-9-	CLK2-9-	96
76	GND	GND	95
77	CLK1-10+	CLK2-10+	94
78	CLK1-10-	CLK2-10-	93
79	GND	GND	92
80	CLK1-11+	CLK2-11+	91
81	CLK1-11-	CLK2-11-	90
82	GND	GND	89
83	CLK1-12+	CLK2-12+	88
84	CLK1-12-	CLK2-12-	87
85	GND	GND	86

4.1.2 CON2: Interface to NAT-MCH BASE-Module

Connector CON2 connects the **NAT-MCH CLK-Module** with the **BASE-Module.**

Table 5: CON2: Connector to NAT-MCH BASE-Module – Pin Assignment

Pin #	Signal	Signal	Pin #
1	/SPISEL_CLKPCB	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_OUT_P	+3.3V MP	14
15	EXTREF_OUT_N	SPICLK	16
17	GND	EXTREF_IN	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

4.1.3 CON3: Interface to NAT-MCH HUB-Module

Connector CON3 connects the **NAT-MCH CLK-Module** with a **NAT-MCH HUB-Module**.

Table 6: CON3: Connector to NAT-MCH HUB-Module – Pin Assigment

Pin #	Signal	Signal	Pin #
1	N.C.	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_P	+3.3V MP	14
15	PCIeCLK_N	SPICLK	16
17	GND	expansion3	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

5 Programming Notes

5.1 SPI Interface

The SPI interface on the **NAT-MCH CLK-Module** is used only for maintenance purposes, e.g. updating the microcontroller firmware or the FPGA image.

5.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **NAT-MCH BASE-Module**. All communication is based on IPMI Messages.

5.3 Register

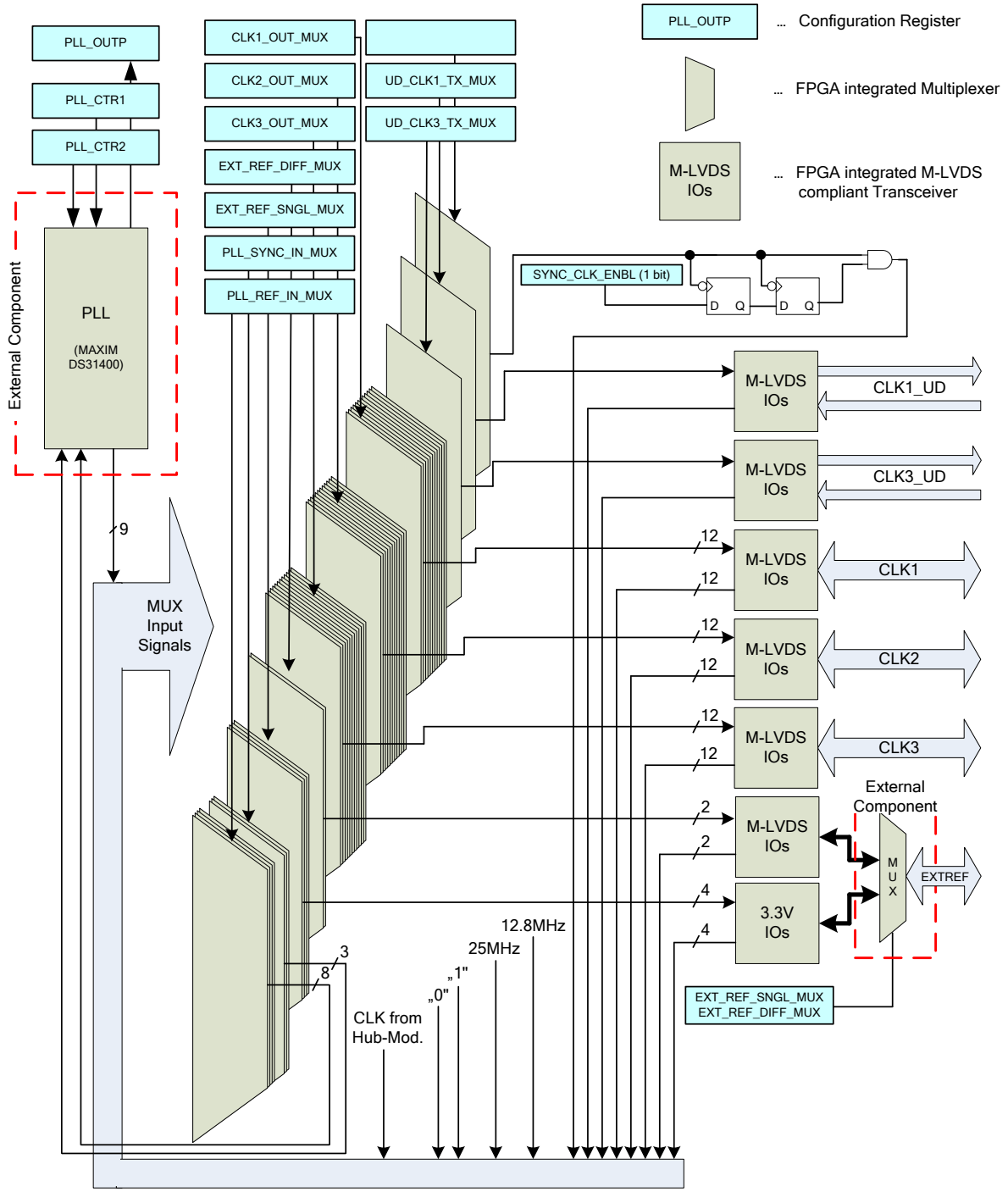
Different clock signals can be received by the **NAT-MCH CLK-Module** via interfaces at the **NAT-MCH BASE-Module's** face plate or the backplane interfaces, e.g. CLK1/2/3 connected to AMCs as well as CLK1/3_UD connected to a redundant MCH.

Additionally the **NAT-MCH CLK-Module** can generate clock signals on its own. Therefore a stratum 3/3E PLL resides on the **CLK-Module**. This PLL can generate various frequencies on different outputs either in free run mode or locked onto a reference clock. Clock signals coming from one of these interfaces can serve as reference for the PLL.

The **NAT-MCH CLK-Module** can also transmit clock signals. This can also be done by the backplane interfaces (CLK1/2/3 and CLK1/3_UD). The clock signals generated by the PLL can serve as source for the transceiver or received signals can directly be routed to other interfaces to be transmitted again.

To allow a maximum flexibility to choose at runtime which clock shall be routed between which interfaces several multiplexers are implemented into the **NAT-MCH CLK-Module's** FPGA. To get a better understanding of these (multiplexer-) functions the following figure shows a detailed overview.

Figure 8: CLK-Signal multiplexing – Detailed Functional Overview



The multiplexer and further functions implemented on the **NAT-MCH CLK-Module** can be controlled by a register interface. The following tables are showing a detailed description of the registers that are available. These registers are not intended to be used by the customer. N.A.T. offers a script based configuration interface that simplifies the complex configuration options. Please refer to chapter "**CLK-Module** Configuration" of the **NAT-MCH** User Manual for a more detailed description of this interface.

Table 7: NAT-MCH CLK-Module – Register overview

	7	6	5	4	3	2	1	0
0x00	BOARD_ID							
0x01	PCB_VERS							
0x02	FW_VERS							
0x03	FPGA_VERS							
0x0A	CLK1_OUT_MUX							
0x16	CLK2_OUT_MUX							
0x22	CLK3_OUT_MUX							
0x2E	UD_CLK1_TX_MUX							
0x2F	UD_CLK3_TX_MUX							
0x30	EXT_REF_SNGL_MUX							
0x34	EXT_REF_DIFF_MUX							
0x36	PLL_REF_IN_MUX							
0x3E	PLL_SYNC_IN_MUX							
0x41	SYNC_CLK_IN_MUX							
0x60	SYNC_CLK_ENBL							
0x61	PLL_FB							
0x62	EXT_CLK_TERM							

5.3.1 BOARD_ID – 0x00

Bit	Name	Description	Default	Access
7..0	BOARD_ID	The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH CLK-Module.**	0xB4	Read Only

5.3.2 PCB_VERS – 0x01

Bit	Name	Description	Default	Access
7..4	PCB_VERS_MAJ	The PCB Version Register contains the version code of the **NAT-MCH CLK-Module.** Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the PCB version is e.g. v3.1 the PCB Version Register contains the value 0x31.	0xXX	Read Only
3..0	PCB_VERS_MIN		0xXX	Read Only

5.3.3 FW_VERS – 0x02

Bit	Name	Description	Default	Access
7..4	FW_VERS_MAJ	The Atmel Version Register contains the version of the Atmel firmware. Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the firmware running on the Atmel is v1.3 the Firmware Version Register contains the value 0x13.	0xXX	Read Only
3..0	FW_VERS_MIN		0xXX	Read Only

5.3.4 FPGA_VERS – 0x03

Bit	Name	Description	Default	Access
7..4	FW_VERS_MAJ	The FPGA Version Register contains the version code of the Altera FPGA. Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the FPGA is running with the image v1.3 the FPGA Version Register contains the value 0x13.	0xXX	Read Only
3..0	FW_VERS_MIN		0xXX	Read Only

5.3.5 CLK1_OUT_MUX – 0x0A

The value of the output selection multiplexer registers selects which source is connected to CLK1 of AMC slot 1 to 12.

Register	AMC Slot
0x0A	CLK1-1_OUT_MUX
0x0B	CLK1-2_OUT_MUX
0x0C	CLK1-3_OUT_MUX
0x0D	CLK1-4_OUT_MUX
0x0E	CLK1-5_OUT_MUX
0x0F	CLK1-6_OUT_MUX
0x10	CLK1-7_OUT_MUX
0x11	CLK1-8_OUT_MUX
0x12	CLK1-9_OUT_MUX
0x13	CLK1-10_OUT_MUX
0x14	CLK1-11_OUT_MUX
0x15	CLK1-12_OUT_MUX

Bit	Name	Description	Default	Access
7..0	CLK1-1..12_OUT_MUX	**Reference Select for REF0 input of the PLL** **0x00** – High impedance (recommended value for receive functionality) **0x01** – CLK1 of AMC1 **0x02** – CLK1 of AMC2 … **0x0C** – CLK1 of AMC12 **0x0D** – CLK2 of AMC1 … **0x18** – CLK2 of AMC12 **0x19** – CLK3 of AMC1 … **0x24** – CLK3 of AMC12 **0x25** – Update CLK1 Rx (from 2nd MCH) **0x26** – Update CLK3 Rx (from 2nd MCH) **0x27** – Extref_single1 (External reference from face plate, single ended) **0x28** – Extref_single2 **0x29** – Extref_single3 **0x2A** – Extref_single4 **0x2B** – Extref_diff1 (External reference from face plate, differential) **0x2C** – Extref_diff2 **0x2D** – PLL_OC1 (clock output of the Maxim PLL) **0x2E** – PLL_OC2 (clock output of the Maxim PLL) **0x2F** – PLL_OC3 (clock output of the Maxim PLL) **0x30** – PLL_OC4 (clock output of the Maxim PLL) **0x31** – PLL_OC5 (clock output of the Maxim PLL) **0x32** – PLL_OC6 (clock output of the Maxim PLL) **0x33** – PLL_OC7 (clock output of the Maxim PLL) **0x34** – PLL_fsync (frame sync output of the Maxim PLL) **0x35** – PLL_mfsync (frame sync output of the Maxim PLL) **0x36** – 12.8 MHz (Stratum3E/3 reference clock) **0x37** – 25 MHz (only with HCSL option) **0x38** – "0" **0x39** – "1" **0x3A** – Sync_clk (refer to chapter 5.3.14 for a description) **0x3B** – Clock from Hub Module All other values result in undefined output values	0x00	Read/ Write

The following multiplexers CLK2-1..12_OUT_MUX and CLK3-1..12_OUT_MUX are offering exactly the same reference signals. Therefore this table is also true for these multiplexers.

5.3.6 CLK2_OUT_MUX – 0x16

The value of the output selection multiplexer registers selects which source is connected to CLK2 of AMC slot 1 to 12.

Register	AMC Slot
0x16	CLK2-1_OUT_MUX
0x17	CLK2-2_OUT_MUX
0x18	CLK2-3_OUT_MUX
0x19	CLK2-4_OUT_MUX
0x1A	CLK2-5_OUT_MUX
0x1B	CLK2-6_OUT_MUX
0x1C	CLK2-7_OUT_MUX
0x1D	CLK2-8_OUT_MUX
0x1E	CLK2-9_OUT_MUX
0x1F	CLK2-10_OUT_MUX
0x20	CLK2-11_OUT_MUX
0x21	CLK2-12_OUT_MUX

For further information refer to the reference table in chapter 5.3.5

5.3.7 CLK3_OUT_MUX – 0x22

The value of the output selection multiplexer registers selects which source is connected to CLK3 of AMC slot 1 to 12.

Register	AMC Slot
0x22	CLK3-1_OUT_MUX
0x23	CLK3-2_OUT_MUX
0x24	CLK3-3_OUT_MUX
0x25	CLK3-4_OUT_MUX
0x26	CLK3-5_OUT_MUX
0x27	CLK3-6_OUT_MUX
0x28	CLK3-7_OUT_MUX
0x29	CLK3-8_OUT_MUX
0x2A	CLK3-9_OUT_MUX
0x2B	CLK3-10_OUT_MUX
0x2C	CLK3-11_OUT_MUX
0x2D	CLK3-12_OUT_MUX

For further information refer to the reference table in chapter 5.3.5

5.3.8 UD_CLK1_TX_MUX - 0x2E

Bit	Name	Description	Default	Access
7..0	CLK1_TX	The value of the update CLK1_Tx output selection multiplexer registers selects which source is connected to update CLK1-Tx.	0x00	Read/Write

5.3.9 UD_CLK3_TX_MUX - 0x2F

Bit	Name	Description	Default	Access
7..0	CLK3_TX	The value of the update CLK3_Tx output selection multiplexer registers selects which source is connected to update CLK3-Tx.	0x00	Read/Write

5.3.10EXT_REF_SNGL_MUX – 0x30

Register	Source
0x30	Extref_single_1 _MUX
0x31	Extref_single_2 _MUX
0x32	Extref_single_3 _MUX
0x33	Extref_single_4 _MUX

Bit	Name	Description	Default	Access
7..0	EXT_REF_SNGL_1..4_MUX	The value of the Clock 1..4 Single Ended Output Selection Multiplexer Registers selects which source is connected to the single ended external reference clock at the face plate.	0x00	Read/Write

5.3.11EXT_REF_DIFF_MUX – 0x34

Register	Source
0x34	Extref_diff_1 _MUX
0x35	Extref_diff_2 _MUX

Bit	Name	Description	Default	Access
7..0	EXT_REF_DIFF_1..2_MUX	The value of the Clock 1..2 Differential Output Selection Multiplexer Registers selects which source is connected to the differential external reference clock at the face plate.	0x00	Read/Write

5.3.12PLL_REF_IN_MUX – 0x36

Register	Source
0x36	PLL_REF_IC1_MUX
0x37	PLL_REF_IC2_MUX
0x38	PLL_REF_IC3_MUX
0x39	PLL_REF_IC4_MUX
0x3A	PLL_REF_IC5_MUX
0x3B	PLL_REF_IC6_MUX
0x3C	PLL_REF_IC7_MUX
0x3D	PLL_REF_IC8_MUX

Bit	Name	Description	Default	Access
7..0	PLL_REF_IC1..8_MUX	The value of the Maxim PLL Reference Input IC1..8 Selection Multiplexer Registers selects which source is connected to the reference input IC1 to IC8 of the Maxim PLL.	0x00	Read/Write

5.3.13PLL_SYNC_IN_MUX - 0x3E

Register	Source
0x3E	PLL_SYNC_IN_1_MUX
0x3F	PLL_SYNC_IN_2_MUX
0x40	PLL_SYNC_IN_3_MUX

Bit	Name	Description	Default	Access
7..0	PLL_SYNC_IN_1..3_MUX	The value of the Maxim PLL Sync Input 1..3 Selection Multiplexer Registers selects which source is connected to the sync input 1 to 3 of the Maxim PLL.	0x00	Read/Write

5.3.14SYNC_CLK_IN_MUX – 0x41

To enable the clock signals for all AMCs in a complete system the multiplexer for each AMC need to be set up one after the other. That causes that the AMCs do not get their clocks enabled at the same time. If the system application requires enabling the clock to all AMCs at the same time the synchronous clock function can be used.

The synchronous clock function includes a multiplexer with the same input as the other multiplexers. The difference is that the output of this multiplexer is connected to an enable gate instead of driving directly the output buffer. The output of that enable gate ("sync_clk") can then be chosen as an input for the clock output multiplexer (e.g. CLK1-1_OUT_MUX, CLK1-2_OUT_MUX, …).

With that solution the clock output multiplexer for all AMCs can be set up one after the other and when configuration is finished the SYNC_CLK_ENBL bit in the SYNC_CLK_ENBL register can be asserted.

The synchronous clock function is controlled by the SYNC_CLK_IN_MUX register in combination with the SYNC_CLK_ENBL register.

Bit	Name	Description	Default	Access
7..0	SYNC_CLK_IN_MUX	The value of the Synchronous Clock Input Selection Multiplexer Registers selects which source is connected to the Synchronous Clock function. This multiplexer has the same input signals as all the other multiplexers, described in chapter 5.3.5.	0x00	Read/Write

5.3.15SYNC_CLK_ENBL - 0x60

The value of the synchronous clock enable registers starts or stops the synchronous clock output. Refer to 5.3.14 for a description of the synchronous clock function.

Bit	Name	Description	Default	Access
7..1		**no function** write as 0 and ignore when read	0x0	Read/Write
0	SYNC_CLK_ENBL	**Enables the Synchronous Clock** If this bit is set the signal that is selected by the SYNC_CLK_IN_MUX Register is glitch free enabled. If the bit is cleared again the signal is glitch free disabled and a "0" is driven out on the Sync clock.	0x0	Read/Write

5.3.16PLL_FB – 0x61

The value of the Maxim PLL feedback registers shows the status of different feedback pins of the Maxim PLL.

Bit	Name	Description	Default	Access
7..3		**no function** write as 0 and ignore when read		
2	PLL_INTREQ	**This bit shows the status of the INTREQ pin of the PLL.** By default the function of that pin is disabled into the PLL.	0x0	Read Only
1	PLL_SRFAIL	**This bit shows the status of the SRFAIL pin of the PLL.** This bit is set to 1 when the selected reference to the DS31400 T0 DPLL fails, (i.e., no clock edges in two UI). SRFAIL is not set in free-run mode or holdover mode.	0x0	Read Only
0	PLL_LOCK	**This bit shows the status of the LOCK pin of the PLL.** The PLL_LOCK bit is set to high when the T0 DPLL is in the lock state.	0x0	Read Only

5.3.17EXT_CLK_TERM – 0x62

The value of the external clock termination select registers chooses which termination is used for the external reference clock from the face plate.

Bit	Name	Description	Default	Access
7..1		**no function** write as 0 and ignore when read	0x0	Read/Write
0	EXT_REF_CLK_TERM	**Selects the termination for the extref lines** If this bit is set a differential termination is chosen and the clock is transmitted via the Extref_diff1..2 lines. If the bit is cleared a single ended termination is chosen and the clock is transmitted via the Extref_single1..4 lines.	0x0	Read/Write

5.3.18HCSL Buffer Register

Register 0-8 of the HCSL buffer are mirrored to the **NAT-MCH CLK-Module** registers 0x64 – 0x6C (100 – 108). Writes on these registers do directly affect the HCSL buffer register. Please refer to the manual [2] of the HCSL buffer for a register description. Table 8: shows a mapping between the buffer ports and the AMC slots.

Table 8: HCSL Buffer Port to AMC Slot Mapping

# AMC Slot CLK3	# HCSL Buffer Port
AMC1	0
AMC2	1
AMC3	2
AMC4	3
AMC5	4
AMC6	5
AMC7	11
AMC8	10
AMC9	9
AMC10	8
AMC11	7
AMC12	6

5.3.19PCIe Reference Clock Generator Register

Register 0x00 – 0x0E of the PCIe reference clock generator are mirrored to the **NAT-MCH CLK-Module** registers 0x6E – 0x7C (110 – 124). Writes on these registers do directly affect the clock generator register. Please refer to the manual of the clock generator for a register description [3].

5.3.20DS31400 PLL Register

The register space of the DS31400 PLL can be accessed through indirect addressing. The **NAT-MCH CLK-Module** registers 0x80 - 81 are used for addressing and register 0x82 for the data value.

To change the value of a PLL register first the address registers must be written (while 0x80 is the lower address byte and 0x81 is the upper address byte). Afterwards the date register (0x82) needs to be filled with the value that should be written to the PLL. Writing to this register does directly affect the PLL register with the address that is set in the address registers.
Reading the data register shows the value of the PLL register with the address that was set in the address register.
Please refer to the manual of the DS31400 PLL for a detailed register description of the PLL [1].

6 Board Specification

Table 9: NAT-MCH CLK-Module Features

Power Consumption	12V / 0.5A max. (only **NAT-MCH CLK-Module**)
PLL Input Frequencies ***(To be sourced from external Reference via Face Plate Connector, CLK1, CLK2 or CLK3)***	• Any multiple of 2 kHz up to 725 MHz. *(clocks via backplane are restricted to a maximum frequency of 100MHz by the MicroTCA specification)* • Special mode for input of 1Hz (1pps) signals
PLL Output Frequencies ***(To be distributed via Face Plate Connector, CLK1, CLK2 or CLK3)***	• Nearly any frequency from 1Hz up to 750MHz. • Frame sync. of 8 kHz and 2 kHz *(clocks via backplane are restricted to a maximum frequency of 100MHz by the MicroTCA specification)*
Cycle to Cycle Output Jitter	~50ps
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 2.0 IPMI Specification v2.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH CLK-Module** during its usual lifetime take refer to the safety note section of the **NAT-MCH BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up, check this section for installation prerequisites and requirements!

7.2.1 Requirements

The **NAT-MCH CLK-Module** is always mounted on a **NAT-MCH BASE-Module**. Therefore please refer to the requirements section of the **NAT-MCH BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH CLK-Module** must meet the following specifications:

- +12 V / 0.5 A max. (only **NAT-MCH CLK-Module**, in addition to other PCBs of the **NAT-MCH**).

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

[1] The M-LVDS Specification recommends a signal rise time of at least 1ns. The output of the used FPGA has a rise time of 0.3 ns.

Appendix A: Correlation between MicroTCA and AMC Clock Naming

The AMC.0 Rev.1.0 as well as the MicroTCA Rev.1.0 have defined three clock interfaces that can be used to for clock distribution purposes. These interfaces are named CLK1, CLK2 and CLK3. With the new AMC.0 V2.0 specification the clocks have been renamed as well as additional clocks were defined.

Which clock of an AMC is connected to which clock of the MCH depends on the connections that are made by the backplane. That means it must not necessarily be that TCLKA of an AMC is always connected to CLK1 of the MCH. Even though, this is the standard way for a non-redundant MicroTCA Backplane.

The following table shows the correlation between the MicroTCA/AMC.0 Rev. 1.0 and the AMC.0 Rev. 2.0 naming.

Table 10: Correlation between MicroTCA and AMC Clock Naming

MicroTCA/AMC.0 Rev. 1.0	AMC.0 Rev. 2.0	Description
CLK1	TCLKA	Telecom Clock A
CLK2	TCLKB	Telecom Clock B
CLK3	**FCLKA**	**Fabric Clock**
X	TCLKC	Telecom Clock C
X	TCLKD	Telecom Clock D

Please refer to the AMC.0 Rev. 2.0 specification for a more detailed description of the single clock signals and their intended purpose.

Since the MicroTCA specification defines the MCH this manual is using the names that are defined by the MicroTCA.

Appendix B: Jitter measurement setup

This appendix describes the measurement setup that was used to measure the maximum cycle to cycle jitter.

There are a lot of different options available to measure the jitter of a signal. Most customers that require a very low jitter are referring to the cycle to cycle jitter.

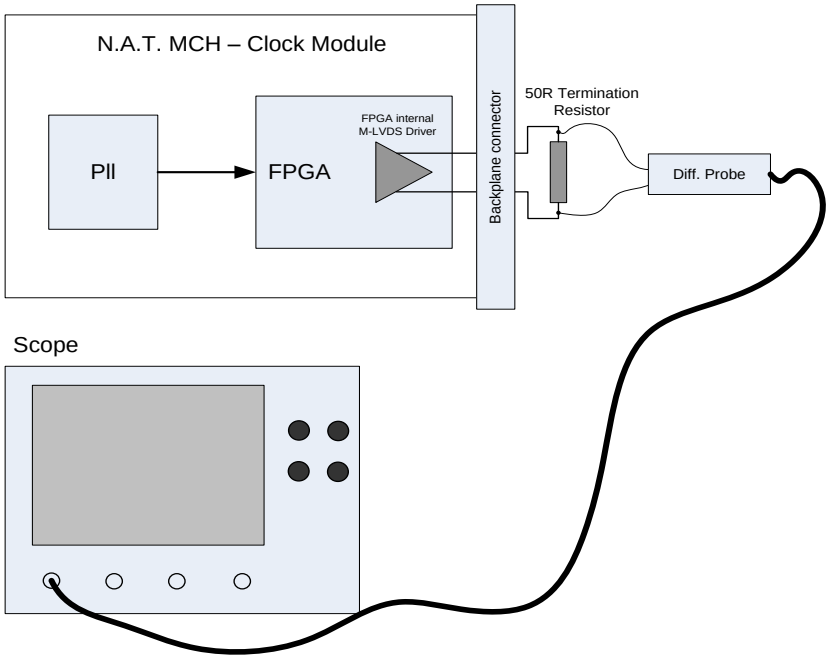
Still there are a lot of different definitions or options available to measure the cycle to cycle jitter. The different measurement options or setups deliver differences in the results that should not be disregarded. Therefore this appendix shows the details of the setup.

Description of the measurement system:

To have no dependencies on a special backplane the clock signal was directly measured after the backplane connector at the termination resistor.

In a normal MicroTCA system there are two 100 Ohm termination resistors in parallel on each clock connection. One is located on the backplane, near the MCH, and one is located on the AMC. Since this is a simplified system there is only one 50 Ohm termination resistor instead of the 2 parallel 100 Ohm. Figure 9 shows the setup.

Figure 9: Jitter measurement setup



Description of the Measurement setup:

To measure the maximum cycle to cycle jitter the TIE (Time Interval Error) function of the oscilloscope was used. The TIE function calculates the difference between the measured times of crossing a given slope and level and the ideal expected time.

That means the scope calculates the optimal or average period time for the whole trace. The result is taken as the reference clock. The output of the function is the deviation between the calculated and the measured edges.

Of course the result of this measurement is the more meaningful the more clock cycles are captured. To have a reasonable ratio between data value that must be captured and calculated and accuracy of the result a minimum of 500 captured cycles was chosen.

The following table shows the jitter results for different typical frequencies measured at CLK1 (or TCLKA) for AMC slot 1.

Table 11: Cycle to Cycle Jitter for typical output Frequencies

Frequency [MHz]	Captured cycles [#]	Max. Jitter $_{\text{Cycle-to-Cycle}}$ [ps]
2.048	1023	51.3
5	500	47.2
10	500	46.1
19.44	971	49.8
30.72	614	36.4
122.88	614	37.8

Summing up, the resulting jitter for the measured frequencies is located in the range of 50ps.

This table shows by far not all possible frequencies that the PLL can generate. Therefore it is only intended to give an idea of an output cycle to cycle jitter that can be estimated.

The jitter values may differ if other frequencies are needed. Furthermore it must be taken into account that the backplane and other AMCs in a real MicroTCA environment may add noise and crosstalk. That increases the jitter.

Hence it is required that the clock signals in a target system are measured at the receiver of the AMCs to verify if the resulting jitter fulfills the system requirements.

Appendix C: Reference Documentation

[1] Maxim DS31400 Stratum 2/3E/3 Timing Card IC, 05/09
http://datasheets.maxim-ic.com/en/ds/DS31400.pdf
[2] IDT ICS9DB1200CTwelve Output Differential Buffer for PCIe Gen1/Gen2, 09/08
http://www.idt.com/products/getDoc.cfm?docID=18459714
[3] IDT ICS9FG104 programmable FTG for differential P4™ CPU, PCIe Clocks, 02/07
http://timing.idt.com/datasheets/ics9FG104.pdf

Appendix D: Document's History

Revision	Date	Description	Author
1.0	10.09.2010	initial revision	ks
1.1	28.04.2011	Document structure chapter "NAT-MCH CLK Module Programming Notes" updated	se
1.2	14.03.2013 15.05.2013	Adapted to pcb version 4.1, minor changes, formatting updated	te/se
1.3	19.05.2013 1.10.2013	Phone and fax updated Adaption to new layout Typo correction	Fh se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	se