NAMC-TCK7
Data Processing AMC Module
Technical Reference Manual V1.2
HW Revision 1.x

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x. The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
ADC	Analog-Digital-Converter
AMC	Advanced Mezzanine Card
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DESY	Deutsches Elektronen-Synchrotron
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GTX	Gigabit Transceiver
JTAG	Joint Test Action Group
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
LLL	Low Latency Links
LLRF	Low Latency Radio Frequency
(M)-LVDS	(Multipoint) Low Voltage Differential Signaling
MMC	Module Management Controller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
PCIe	Peripheral Component Interconnect Express
PLL	Phase-Locked Loop
RAM	Random Access Memory
RTM	Rear Transition Module
SFP(+)	Small Form-Factor Pluggable
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SMB	SubMiniature version B
UART	Universal Asynchronous Receiver/Transmitter
(Micro)-USB	(Micro) Universal Serial Bus

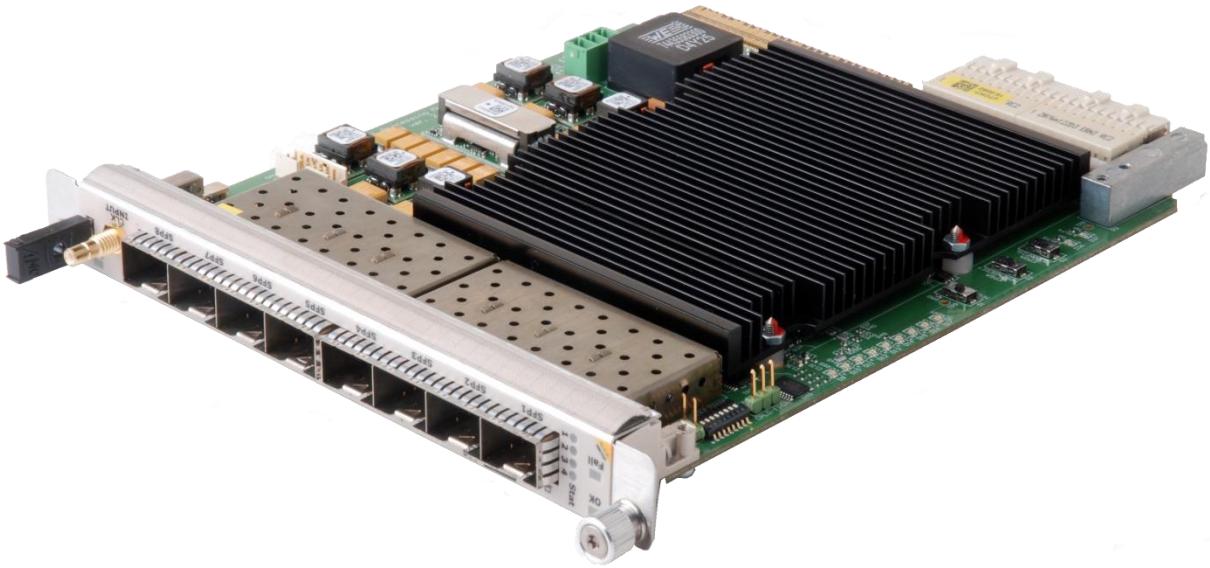
1 Introduction

The **NAMC-TCK7** is a general purpose high-performance low-latency data processing AMC module providing processing power, data memory, communication links, and reference clock signals. Originally designed as a LLRF (Low Level Radio Frequency) cavity field stabilizing controller, the application field is much wider.

The XILINX Kintex-7 FPGA (XC7K355T or XC7420T) delivers computing power and memory for low-latency digital signal processing. It supports a number of LLLs (Low Latency Links) available on the front plate, at the backplane, and via a RTM (Rear Transition Module), working with several Gbps throughput. In-System firmware upgrade via IPMI and fast serial link is supported.

The following figure shows a photo of the **NAMC-TCK7.**

Figure 1: NAMC-TCK7



2 Overview

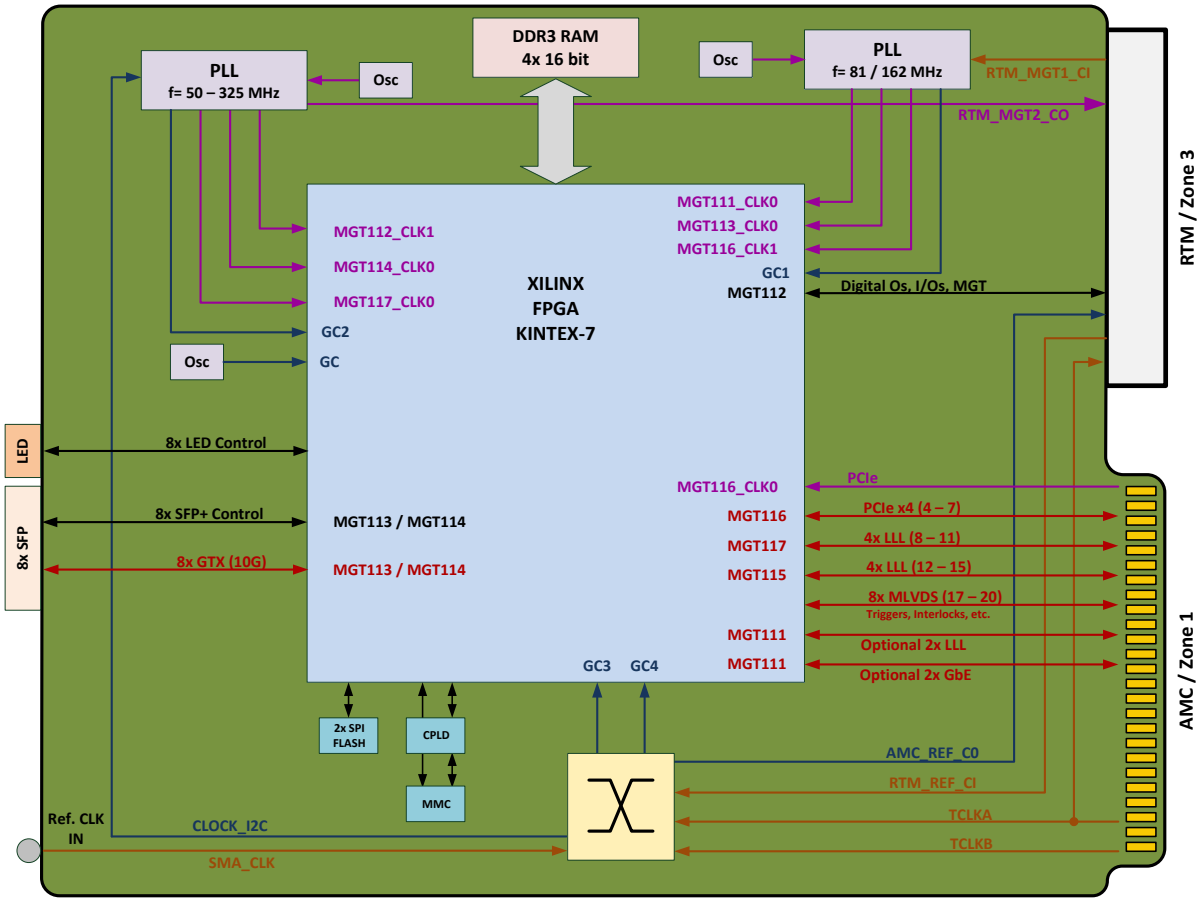
2.1 Major Features

- XILINX XILINX-7 FPGA
- DDR3 Memory
- CPLD
- Quad SPI FLASH memory
- Clock
- Connectivity
  - Front Panel
  - Backplane (Zone 1) AMC
  - Backplane (Zone 3) RTM

2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-TCK7**.

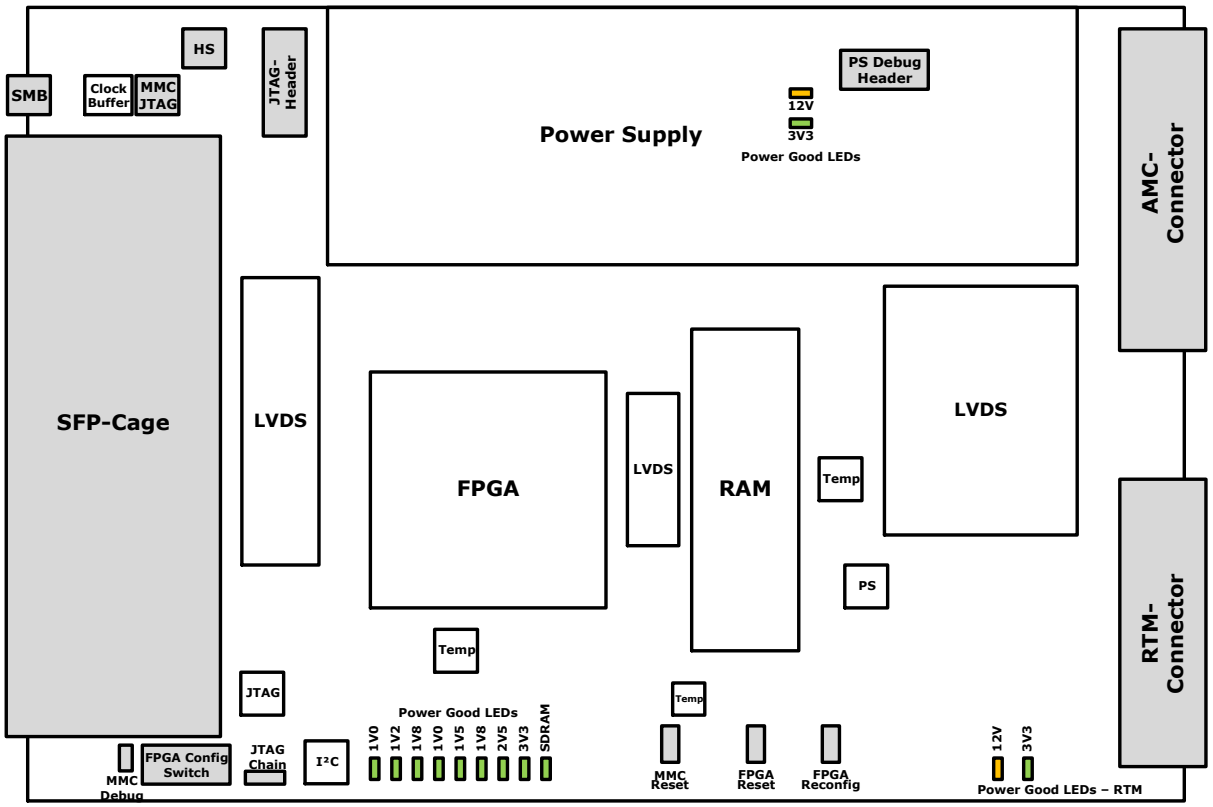
Figure 2: NAMC-TCK7 – Block Diagram

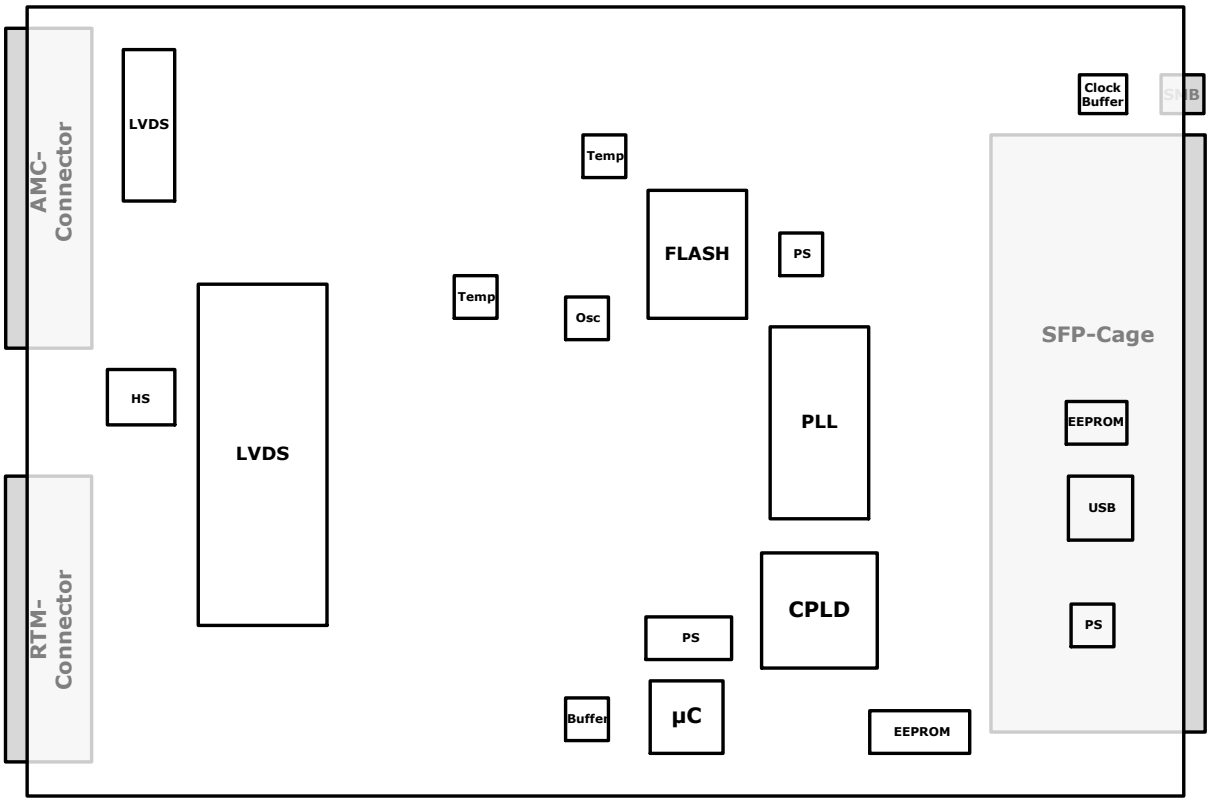


2.3 Location Diagram

The following figure shows a location diagram of the **NAMC-TCK7**.

Figure 3: NAMC-TCK7 – Location Diagram




AMC-Connector
LVDS
Temp
FLASH
PS
Clock Buffer
SMB
Temp
Osc
SFP-Cage
HS
LVDS
PLL
EEPROM
USB
RTM-Connector
CPLD
PS
PS
Buffer
µC
EEPROM

3 Board Features

The **NAMC-TCK7** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 FPGA

The **NAMC-TCK7** hosts a XILINX Kintex-7 FPGA; XC7K355T (default) or XC7K420T (option). In default assembly option the FPGA offers 24 multi-gigabit transceivers, which support bit-rates up to 12.5 Gb/s. Hardware support for PCIe Gen2 communication is contained as well, hence the implemented x4 link can reach throughput of 20 Gb/s.

3.2 DDR3 Memory

For temporary data storage the **NAMC-TCK7** features four SDRAM DDR3 memory chips, each with a capacity of 4Gb (16 Gb in total), operating with a data rate of 1066 Mbit/s and a width of 64 bit. The memory circuits share the address and control buses.

3.3 CPLD

The **NAMC-TCK7** features a XILINX XC2C256 CoolRunner-II CPLD. This device is used for support functions like multiplexing and switching of SPI and JTAG lines, as well as for driving status LED.

For further information on the XILINX CPLD, please refer to Appendix A.

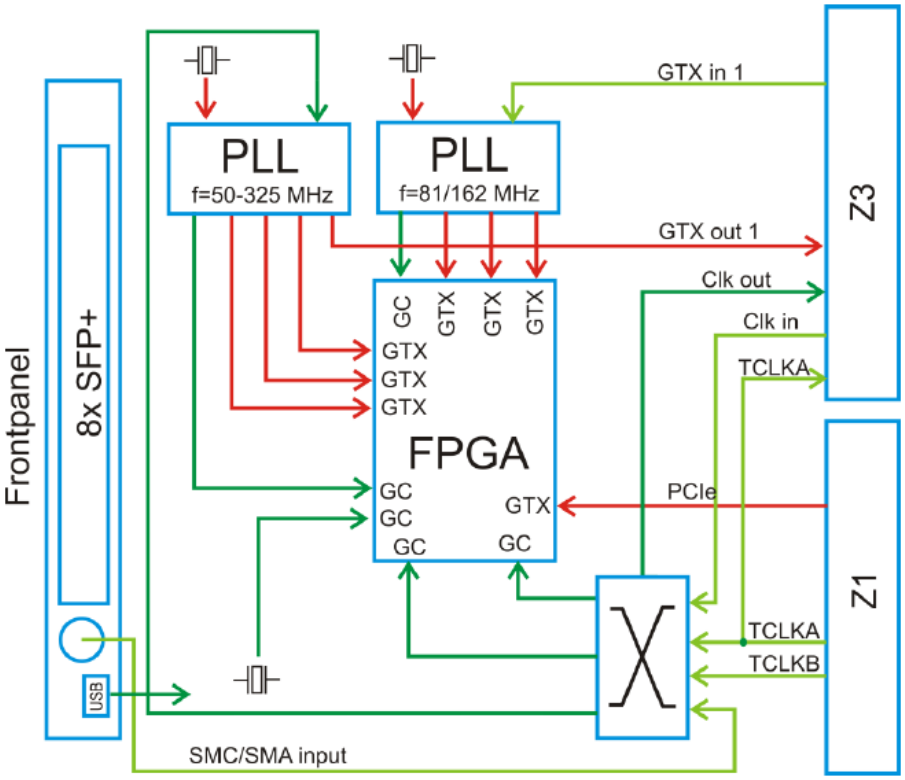
3.4 SPI FLASH Memory

For permanent data storage, the **NAMC-TCK7** is equipped with a Quad SPI FLASH containing the FPGA bit stream; the memory space beyond the bit stream is available for user application.

3.5 Clock

The XILINX Kintex-7 FPGA requires external signals for GTX transceivers, PCIe, GbE interface, and digital logic (Global Clock FPGA Signals). The clock distribution of the **NAMC-TCK7** is shown below.

Figure 4: NAMC-TCK7 – Clock Distribution



The clock distribution circuit provides a broad range of reference frequencies for high-speed serial interfaces. The following table shows an example of reference frequencies that can be generated by the on-board PLL circuits.

Table 2: Reference Frequencies for selected high-speed serial interfaces

Interface Type	Frequency [MHz]
DESY LLRF	81.25 or 160.5
PCI Express	100
Fibre Channel	106.25
Infiniband	125
GigE	125
10 GigE	156.25
10-G Fibre Channel	159.375
12 GigE	187.5
10GBASE-R, 10GBASE-X, XGMII	312.5

The PCIe clock is delivered from the AMC backplane (f = 100 MHz). The reference clock for the GTX transceivers can be provided by the RTM (e.g. f = 81.25 MHz). A programmable PLL allows multiplying the frequency (e.g. x1, x2, etc.) and then the signal is connected to the GTX transceivers and the FPGA logic.

3.6 Connectivity

3.6.1 Front Panel

The front panel provides MTCA.4 standard compliant retention devices, handle, and three IPMI LEDs as well as four LEDs for FPGA application free use. Please see chapter 4.5 Front Panel & LEDs for details.

For low-latency connections towards various LLRF components via optical fibre eight SFP+-Bays can be used.

A reference clock signal can be received via a SMB connector. Please see chapter 3.5 Clock for details.

The **NAMC-TCK7** features a MicroUSB connector which provides access to diagnostic UARTs (RS232-via-USB). The debug interface allows for performing low-speed data transmissions to the MMC and FPGA circuits.

3.6.2 Backplane (Zone 1) AMC

The Zone 1 connector provides eight low-latency communication links to the ADC boards, a PCIe interface to the controlling CPU, M-LVDS bus signals, and other signal required by the AMC standard. The two 1 GbE-channels and LLL on ports 2 and 3 are available for the XC7K420T-FPGA only.

The connector is compatible with the double-row B+-Connector specified in the AMC base specification with extensions required by PICMG MTCA.4.

3.6.3 Backplane (Zone 3) RTM

The Zone 3 connection provides low-latency links to the RTM (in case of a LLRF-System it is a vector modulator), general purpose parallel bus (LVDS levels), output signals (interlocks), reference clock inputs and outputs for GTX, and digital logic and other signals required by MTCA.4. The **NAMC-TCK7** can be connected to a RTM using two 30-pair ADF connectors.

4 Hardware

4.1 AMC Port Definition

Table 3: AMC Port Definition

Port	Signal	Characteristic	Description
0	1GbE 1000Base-X	Single lane	AMC.2
1	1GbE 1000Base-X	Single lane	AMC.2
2	LLL (Xilinx)	P2P connection, single lane	Custom
3	LLL (Xilinx)	P2P connection, single lane	Custom
4	PCIe x4 (lane 0)	1 or 4 lanes	AMC.1
5	PCIe x4 (lane 1)		
6	PCIe x4 (lane 2)		
7	PCIe x4 (lane 3)		
8	LLL (Xilinx)	P2P connection, single lane	Custom
9	LLL (Xilinx)	P2P connection, single lane	Custom
10	LLL (Xilinx)	P2P connection, single lane	Custom
11	LLL (Xilinx)	P2P connection, single lane	Custom
12	LLL (Xilinx)	P2P connection, single lane	Custom
13	LLL (Xilinx)	P2P connection, single lane	Custom
14	LLL (Xilinx)	P2P connection, single lane	Custom
15	LLL (Xilinx)	P2P connection, single lane	Custom
17_RxD	BusDClock	Bidirectional	Custom
17_TxD	BusData	Bidirectional	Custom
18_RxD	StartTrigger	Bidirectional	Custom
18_TxD	PreTrigger	Bidirectional	Custom
19_RxD	RESET (AppTrigger)	Bidirectional	Custom
19_TxD	INTERLOCK0 Receiver/Transmitter	Input / Bidirectional	Custom
20_RxD	INTERLOCK1 Receiver/Transmitter	Input / Bidirectional	Custom
20_TxD	INTERLOCK2 Receiver/Transmitter	Bidirectional	Custom
TCLKA	f = 108 MHz	Input	General purpose Fast clock
TCLKB	f = 4.514 MHz	Input	General purpose Slow clock
FCLKA	f = 100 MHz	Input	Synchronization clock for PCIe
N/A	JTAG	Voltage levels translated to 3.3V (output)	JTAG chain for programmable devices
N/A	IPMI	With pull-up	IPMI for MMC (SCL/SDA)
N/A	PS0, PS1	With pull-up and low-pass-filter	Presence detection

Port	Signal	Characteristic	Description
N/A	GA0 / GA1 / GA2	With pull-up controlled by MMC	Geographical address
N/A	Enable_n	With pull-up	Enable
N/A	MP +3V3	0.15A / 150µF max.	Management power
N/A	PP +12V	7.4A / 800µF max.	Payload Power

4.2 FPGA GTX-Transceiver-Assignment

Each GTX-Quad is allocated to a dedicated FPGA-Bank. The following tables show the assignment for the different FPGA-types.

Table 4: Assignment GTX-Transceiver to FPGA-Bank on XC7K355T

# GTX-Transceiver	# FPGA Bank
X0Y0 – X0Y3	112
X0Y4 – X0Y7	113
X0Y8 – X0Y11	114
X0Y12 – X0Y15	115
X0Y16 – X0Y19	116
X0Y20 – X0Y23	117

Table 5: Assignment GTX-Transceiver to FPGA-Bank on XC7K420T

# GTX-Transceiver	# FPGA Bank
X0Y0 – X0Y3	111
X0Y4 – X0Y7	112
X0Y8 – X0Y11	113
X0Y12 – X0Y15	114
X0Y16 – X0Y19	115
X0Y20 – X0Y23	116
X0Y24 – X0Y27	117

For further information on the XILINX Kintex-7, please refer to Appendix A.

4.3 FPGA Pin-Assignment

The following tables show the FPGA I/O pin assignment. Pin functions are fixed and cannot be changed by the user.

Table 6: Bank 0 – JTAG-/FPGA-Configuration

Pin Name	Pin Location	Function
M1_0	AC12	GND
M0_0	AC13	VCC+3V3
M2_0	AB12	GND
DONE_0	AC10	FPGA_DONE
CFGBVS_0	AC11	VCC+3V3
PROGRAM_B_0	AB11	FPGA_PROG_N
INIT_B_0	H10	FPGA_INIT_N
TDI_0	H11	FPGA_JTAG_TDI
TDO_0	J13	FPGA_JTAG_TDO
TMS_0	J11	FPGA_JTAG_TMS
TCK_0	H12	FPGA_JTAG_TCK
CCLK_0	H13	CCLK
VCCBATT_0	G13	GND
VN_0	T12	GND
VP_0	R13	GND
VREFP_0	T13	GND
VREFN_0	R12	GND
DXP_0	U13	FPGA_TEMP_DX_P
GNDADC_0	P12	GND
VCCADC_0	P13	VCC+1V8
DXN_0	U12	FPGA_TEMP_DX_N

Table 7: Bank 12 – Zone3-1 I/O

Pin Name	Pin Location	Function
IO_25_12	AE20	INTR_PLL_70
IO_L24N_T3_12	AK26	J31A.IO7_N
IO_L24P_T3_12	AJ26	J31A.IO7_P
IO_L23N_T3_12	AK25	J31B.IO17_N
IO_L23P_T3_12	AK24	J31B.IO17_P
IO_L22N_T3_12	AJ24	J31C.IO6_N
IO_L22P_T3_12	AJ23	J31C.IO6_P
IO_L21N_T3_DQS_12	AK23	J31A.IO13_N
IO_L21P_T3_DQS_12	AJ22	J31A.IO13_P
IO_L20N_T3_12	AK21	J31A.IO16_N
IO_L20P_T3_12	AJ21	J31A.IO16_P
IO_L19N_T3_VREF_12	AH22	J31C.IO12_N
IO_L19P_T3_12	AH21	J31C.IO12_P
IO_L18N_T2_12	AG20	J31C.IO18_N
IO_L18P_T2_12	AF20	J31C.IO18_P
IO_L17N_T2_12	AF21	J31C.IO15_N
IO_L17P_T2_12	AE21	J31C.IO15_P
IO_L16N_T2_12	AD22	J31C.IO9_N
IO_L16P_T2_12	AD21	J31C.IO9_P
IO_L15N_T2_DQS_12	AE23	CLOCK_I2C.SDA
IO_L15P_T2_DQS_12	AD23	CLOCK_I2C_SCL
IO_L14N_T2_SRCC_12	AF23	J31A.IO20_CC_N
IO_L14P_T2_SRCC_12	AF22	J31A.IO20_CC_P
IO_L13N_T2_MRCC_12	AG23	GC2_CLK_N
IO_L13P_T2_MRCC_12	AG22	GC2_CLK_P
IO_L12N_T1_MRCC_12	AH24	GC1_CLK_N
IO_L12P_T1_MRCC_12	AG24	GC1_CLK_P
IO_L11N_T1_SRCC_12	AG25	J31A.IO19_CC_N
IO_L11P_T1_SRCC_12	AF25	J31A.IO19_CC_P
IO_L10N_T1_12	AE24	J31A.IO10_N
IO_L10P_T1_12	AD24	J31A.IO10_P
IO_L9N_T1_DQS_12	AF26	J30C.IO18_N
IO_L9P_T1_DQS_12	AE25	J30C.IO18_P
IO_L8N_T1_12	AH26	J31B.IO14_N
IO_L8P_T1_12	AH25	J31B.IO14_P
IO_L7N_T1_12	AE26	nc
IO_L7P_T1_12	AD26	RTM_CLK_SEL_2V5
IO_L6N_T0_VREF_12	AC22	INTERLOCK2_DIR_2V5
IO_L6P_T0_12	AC21	INTERLOCK1_DIR_2V5
IO_L5N_T0_12	AB23	INTERLOCK0_DIR_2V5
IO_L5P_T0_12	AB22	INTR_PLL_71
IO_L4N_T0_12	AC20	FPGA_UART_USB_TXD
IO_L4P_T0_12	AB20	FPGA_UART_USB_RXD
IO_L3N_T0_DQS_12	AA23	FPGA_LEDS.LED3
IO_L3P_T0_DQS_12	AA22	MMC_FPGA_SQUARE
IO_L2N_T0_12	AA21	nc
IO_L2P_T0_12	AA20	nc
IO_L1N_T0_12	Y21	FPGA_LEDS.LED1

Pin Name	Pin Location	Function
IO_L1P_T0_12	Y20	FPGA_LEDS.LED2
IO_0_12	Y23	FPGA_LEDS.LED4

Table 8: Bank 13 – Zone3-2 I/O

Pin Name	Pin Location	Function
IO_25_13	Y24	nc
IO_L24N_T3_13	AK29	J30C.IO12_N
IO_L24P_T3_13	AK28	J30C.IO12_P
IO_L23N_T3_13	AK30	J31A.IO4_N
IO_L23P_T3_13	AJ29	J31A.IO4_P
IO_L22N_T3_13	AH30	J31B.IO2_N
IO_L22P_T3_13	AG30	J31B.IO2_P
IO_L21N_T3_DQS_13	AJ28	J31B.IO8_N
IO_L21P_T3_DQS_13	AJ27	J31B.IO8_P
IO_L20N_T3_13	AH29	J31B.IO5_N
IO_L20P_T3_13	AG29	J31B.IO5_P
IO_L19N_T3_VREF_13	AH27	J31B.IO11_N
IO_L19P_T3_13	AG27	J31B.IO11_P
IO_L18N_T2_13	AG28	J31A.IO1_N
IO_L18P_T2_13	AF27	J31A.IO1_P
IO_L17N_T2_13	AF30	J30B.IO11_N
IO_L17P_T2_13	AE30	J30B.IO11_P
IO_L16N_T2_13	AE29	J30B.IO17_N
IO_L16P_T2_13	AD29	J30B.IO17_P
IO_L15N_T2_DQS_13	AC30	J30B.IO14_N
IO_L15P_T2_DQS_13	AC29	J30B.IO14_P
IO_L14N_T2_SRCC_13	AF28	J30A.IO16_CC_N
IO_L14P_T2_SRCC_13	AE28	J30A.IO16_CC_P
IO_L13N_T2_MRCC_13	AD28	J30A.IO13_CC_N
IO_L13P_T2_MRCC_13	AC27	J30A.IO13_CC_P
IO_L12N_T1_MRCC_13	AB27	J30A.IO4_CC_N
IO_L12P_T1_MRCC_13	AA27	J30A.IO4_CC_P
IO_L11N_T1_SRCC_13	AA26	J30A.IO1_CC_N
IO_L11P_T1_SRCC_13	Y26	J30A.IO1_CC_P
IO_L10N_T1_13	AC24	J31C.IO3_N
IO_L10P_T1_13	AB24	J31C.IO3_P
IO_L9N_T1_DQS_13	AC25	J30B.IO8_N
IO_L9P_T1_DQS_13	AB25	J30B.IO8_P
IO_L8N_T1_13	AA25	J30C.IO6_N
IO_L8P_T1_13	Y25	J30C.IO6_P
IO_L7N_T1_13	AD27	J30C.IO15_N
IO_L7P_T1_13	AC26	J30C.IO15_P
IO_L6N_T0_VREF_13	W27	J30C.IO3_N
IO_L6P_T0_13	W26	J30C.IO3_P
IO_L5N_T0_13	W29	J30B.IO2_N
IO_L5P_T0_13	W28	J30B.IO2_P
IO_L4N_T0_13	Y29	J30B.IO5_N
IO_L4P_T0_13	Y28	J30B.IO5_P

Pin Name	Pin Location	Function
IO_L3N_T0_DQS_13	AA30	J30A.IO7_N
IO_L3P_T0_DQS_13	Y30	J30A.IO7_P
IO_L2N_T0_13	AB30	J30C.IO9_N
IO_L2P_T0_13	AB29	J30C.IO9_P
IO_L1N_T0_13	AB28	J30A.IO10_N
IO_L1P_T0_13	AA28	J30A.IO10_P
IO_0_13	W24	nc

Table 9: Bank 14 – Zone1 I/O

Pin Name	Pin Location	Function
IO_25_14	W21	8XI2C.LANE3.SCL
IO_L24N_T3_A00_D16_14	W19	8XI2C.LANE3.SDA
IO_L24P_T3_A01_D17_14	W18	8XI2C.LANE2.SDA
IO_L23N_T3_A02_D18_14	W17	8XI2C.LANE2.SCL
IO_L23P_T3_A03_D19_14	V17	8XI2C.LANE1.SCL
IO_L22N_T3_A04_D20_14	U18	8XI2C.LANE8.SDA
IO_L22P_T3_A05_D21_14	U17	8XI2C.LANE8.SCL
IO_L21N_T3_DQS_A06_D22_14	T18	8XI2C.LANE7.SDA
IO_L21P_T3_DQS_14	T17	8XI2C.LANE7.SCL
IO_L20N_T3_A07_D23_14	V19	8XI2C.LANE1.SDA
IO_L20P_T3_A08_D24_14	U19	8XI2C.LANE6.SCL
IO_L19N_T3_A09_D25_VREF_14	R19	8XI2C.LANE5.SDA
IO_L19P_T3_A10_D26_14	R18	8XI2C.LANE5.SCL
IO_L18N_T2_A11_D27_14	W23	8XI2C.LANE5.SCL
IO_L18P_T2_A12_D28_14	W22	8XI2C.LANE4.SDA
IO_L17N_T2_A13_D29_14	V20	8XI2C.LANE6.SDA
IO_L17P_T2_A14_D30_14	U20	FPGA_SPI.MOSI
IO_L16N_T2_A15_D31_14	T21	FPGA_SPI.CS
IO_L16P_T2_CSI_B_14	T20	FPGA_SPI.MISO
IO_L15N_T2_DQS_DOUT_CSO_B_14	R21	SPI_MMC_SCK
IO_L15P_T2_DQS_RDWR_B_14	R20	M-LVDS-FPGA.TRGSTART_DATA
IO_L14N_T2_SRCC_14	U23	M-LVDS-FPGA.CLK_AUX_DATA
IO_L14P_T2_SRCC_14	U22	FPGA_SPI.SCK
IO_L13N_T2_MRCC_14	V22	SPI_MMC_MISO
IO_L13P_T2_MRCC_14	V21	CLK_50MHz
IO_L12N_T1_MRCC_14	U25	M-LVDS-FPGA.INTERLOCK0_DATA
IO_L12P_T1_MRCC_14	U24	GC3
IO_L11N_T1_SRCC_14	T26	M-LVDS-FPGA.AMC_CRYO_OK_DATA
IO_L11P_T1_SRCC_14	T25	GC4
IO_L10N_T1_D15_14	T27	SPI_MMC_MOSI
IO_L10P_T1_D14_14	R26	M-LVDS-FPGA.AMC_CRYO_OK_DIR
IO_L9N_T1_DQS_D13_14	V25	M-LVDS-FPGA.TRGSTART_DIR
IO_L9P_T1_DQS_14	V24	M-LVDS-FPGA.TRGEND_DIR
IO_L8N_T1_D12_14	T23	FPGA_SPI_AS_JTAG

Pin Name	Pin Location	Function
IO_L8P_T1_D11_14	R23	M-LVDS-FPGA.INTERLOCK2_DATA
IO_L7N_T1_D10_14	R25	FPGA_INT_Interlock3
IO_L7P_T1_D09_14	R24	M-LVDS-FPGA.INTERLOCK1_DATA
IO_L6N_T0_D08_VREF_14	V27	M-LVDS-FPGA.TRGEND_DATA
IO_L6P_T0_FCS_B_14	V26	CS_IN
IO_L5N_T0_D07_14	U28	M-LVDS-FPGA.TRGREADOUT_DIR
IO_L5P_T0_D06_14	U27	FPGA_INT_Interlock1
IO_L4N_T0_D05_14	U30	M-LVDS-FPGA.CLK_AUX_DIR
IO_L4P_T0_D04_14	U29	FPGA_INT_Interlock0
IO_L3N_T0_DQS_EMCCLK_14	V30	M-LVDS-FPGA.TRGREADOUT_DATA
IO_L3P_T0_DQS_PUDC_B_14	V29	GND
IO_L2N_T0_D03_14	T28	FLASH_D3
IO_L2P_T0_D02_14	R28	FLASH_D2
IO_L1N_T0_D01_DIN_14	T30	FLASH_D1
IO_L1P_T0_D00_MOSI_14	R30	FLASH_D0
IO_0_14	T22	SPI_MMC_CS_FPGA

Table 10: Bank 15 – DDR3-RAM Data 1/2 I/O

Pin Name	Pin Location	Function
IO_25_15	P22	nc
IO_L24N_T3_RS0_15	P18	DDR3_DQ18
IO_L24P_T3_RS1_15	P17	DDR3_DQ22
2IO_L23N_T3_FWE_B_15	M17	DDR3_DQ21
IO_L23P_T3_FOE_B_15	N17	DDR3_DQ19
IO_L22N_T3_A16_15	N19	DDR3_DQ20
IO_L22P_T3_A17_15	P19	DDR3_DQ16
IO_L21N_T3_DQS_A18_15	M19	DQS_N2
IO_L21P_T3_DQS_15	M18	DQS_P2
IO_L20N_T3_A19_15	N21	DDR3_DQ23
IO_L20P_T3_A20_15	P21	DDR3_DM3
IO_L19N_T3_A21_VREF_15	M20	VREF+0V75
IO_L19P_T3_A22_15	N20	DDR3_DQ17
IO_L18N_T2_A23_15	L21	DDR3_DQ14
IO_L18P_T2_A24_15	L20	DDR3_DQ13
IO_L17N_T2_A25_15	P24	DDR3_DM1
IO_L17P_T2_A26_15	P23	DDR3_DQ11
IO_L16N_T2_A27_15	M22	DDR3_DQ12
IO_L16P_T2_A28_15	N22	DDR3_DQ9
IO_L15N_T2_DQS_ADV_B_15	K24	DQS_N1
IO_L15P_T2_DQS_15	L23	DQS_P1
IO_L14N_T2_SRCC_15	N25	DDR3_DQ15
IO_L14P_T2_SRCC_15	N24	DDR3_DQ8
IO_L13N_T2_MRCC_15	M24	nc

Pin Name	Pin Location	Function
IO_L13P_T2_MRCC_15	M23	DDR3_DQ10
IO_L12N_T1_MRCC_AD5N_15	L27	DDR3_DQ5
IO_L12P_T1_MRCC_AD5P_15	L26	DDR3_DQ2
IO_L11N_T1_SRCC_AD12N_15	L25	DDR3_DQ6
IO_L11P_T1_SRCC_AD12P_15	M25	DDR3_DQ4
IO_L10N_T1_AD4N_15	P28	DDR3_DQ1
IO_L10P_T1_AD4P_15	P27	DDR3_DM0
IO_L9N_T1_DQS_AD11N_15	M27	DQS_N0
IO_L9P_T1_DQS_AD11P_15	N27	DQS_P0
IO_L8N_T1_AD3N_15	N26	DDR3_DQ7
IO_L8P_T1_AD3P_15	P26	DDR3_DQ0
IO_L7N_T1_AD10N_15	K26	nc
IO_L7P_T1_AD10P_15	K25	DDR3_DQ3
IO_L6N_T0_VREF_15	L28	VREF+0V75
IO_L6P_T0_15	M28	DDR3_DQ24
IO_L5N_T0_AD2N_15	P29	DDR3_DQ27
IO_L5P_T0_AD2P_15	R29	DDR3_DM3
IO_L4N_T0_AD9N_15	M29	DDR3_DQ25
IO_L4P_T0_AD9P_15	N29	DDR3_DQ29
IO_L3N_T0_DQS_AD1N_15	M30	DQS_N3
IO_L3P_T0_DQS_AD1P_15	N30	DQS_P3
IO_L2N_T0_AD8N_15	K30	DDR3_DQ30
IO_L2P_T0_AD8P_15	L30	DDR3_DQ31
IO_L1N_T0_AD0N_15	K29	DDR3_DQ28
IO_L1P_T0_AD0P_15	K28	DDR3_DQ26
IO_0_15	L22	nc

Table 11: Bank 16 – DDR3-RAM Data 4 I/O and DDR3-RAM Control

Pin Name	Pin Location	Function
IO_25_16	J24	DDR3_VRP
IO_L24N_T3_16	A28	DDR3_CK_N
IO_L24P_T3_16	A27	DDR3_CK_P
IO_L23N_T3_16	A30	DDR3_A10
IO_L23P_T3_16	B30	DDR3_WE_N
IO_L22N_T3_16	B29	DDR3_A12
IO_L22P_T3_16	B28	DDR3_BA1
IO_L21N_T3_DQS_16	C30	DDR3_RAS_N
IO_L21P_T3_DQS_16	C29	DDR3_A4
IO_L20N_T3_16	D29	DDR3_CAS_N
IO_L20P_T3_16	E29	DDR3_A0
IO_L19N_T3_VREF_16	D28	VREF+0V75
IO_L19P_T3_16	E28	DDR3_CS_N
IO_L18N_T2_16	J29	DDR3_A13
IO_L18P_T2_16	J28	DDR3_RESET_N
IO_L17N_T2_16	G30	DDR3_A5
IO_L17P_T2_16	H30	DDR3_A11
IO_L16N_T2_16	E30	DDR3_BA2
IO_L16P_T2_16	F30	DDR3_A2

Pin Name	Pin Location	Function
IO_L15N_T2_DQS_16	G29	DDR3_A8
IO_L15P_T2_DQS_16	H29	DDR3_A14
IO_L14N_T2_SRCC_16	F28	DDR3_A3
IO_L14P_T2_SRCC_16	G28	DDR3_A1
IO_L13N_T2_MRCC_16	F27	DDR3_ODT
IO_L13P_T2_MRCC_16	G27	DDR3_A7
IO_L12N_T1_MRCC_16	E26	DDR3_A6
IO_L12P_T1_MRCC_16	E25	DDR3_CKE
IO_L11N_T1_SRCC_16	F26	DDR3_A15
IO_L11P_T1_SRCC_16	F25	DDR3_BA0
IO_L10N_T1_16	H27	DDR3_A9
IO_L10P_T1_16	H26	nc
IO_L9N_T1_DQS_16	J27	nc
IO_L9P_T1_DQS_16	J26	nc
IO_L8N_T1_16	G25	nc
IO_L8P_T1_16	H25	nc
IO_L7N_T1_16	G24	nc
IO_L7P_T1_16	H24	nc
IO_L6N_T0_VREF_16	D27	VREF+0V75
IO_L6P_T0_16	D26	DDR3_DQ50
IO_L5N_T0_16	B27	DDR3_DQ54
IO_L5P_T0_16	C27	DDR3_DQ52
IO_L4N_T0_16	A26	DDR3_DQ48
IO_L4P_T0_16	A25	DDR3_DQ55
IO_L3N_T0_DQS_16	C26	DQS_N6
IO_L3P_T0_DQS_16	C25	DQS_P6
IO_L2N_T0_16	B25	DDR3_DQ53
IO_L2P_T0_16	B24	DDR3_DQ49
IO_L1N_T0_16	C24	DDR3_DQ51
IO_L1P_T0_16	D24	DDR3_DM6
IO_0_16	E24	VCC+1V5

Table 12: Bank 17 – DDR3-RAM Data 3/4 I/O and DIPSWITCH

Pin Name	Pin Location	Function
IO_25_17	L17	nc
IO_L24N_T3_17	A23	DDR3_DQ59
IO_L24P_T3_17	A22	DDR3_DQ63
IO_L23N_T3_17	B23	DDR3_DQ61
IO_L23P_T3_17	B22	DDR3_DQ57
IO_L22N_T3_17	A21	DDR3_DM7
IO_L22P_T3_17	A20	DDR3_DQ60
IO_L21N_T3_DQS_17	A18	DQS_N7
IO_L21P_T3_DQS_17	B18	DWS_P7
IO_L20N_T3_17	B20	DDR3_DQ56
IO_L20P_T3_17	B19	DDR3_DQ62
IO_L19N_T3_VREF_17	C20	VREF+0V75
IO_L19P_T3_17	C19	DDR3_DQ58
IO_L18N_T2_17	D19	DDR3_DQ35

Pin Name	Pin Location	Function
IO_L18P_T2_17	D18	DDR3_DM4
IO_L17N_T2_17	E19	DDR3_DQ38
IO_L17P_T2_17	E18	DDR3_DQ34
IO_L16N_T2_17	C22	DDR3_DQ33
IO_L16P_T2_17	C21	DDR3_DQ37
IO_L15N_T2_DQS_17	D23	DQS_N4
IO_L15P_T2_DQS_17	E23	DQS_P4
IO_L14N_T2_SRCC_17	D22	DDR3_DQ36
IO_L14P_T2_SRCC_17	D21	DDR3_DQ39
IO_L13N_T2_MRCC_17	E21	nc
IO_L13P_T2_MRCC_17	E20	DDR3_DQ32
IO_L12N_T1_MRCC_17	F21	nc
IO_L12P_T1_MRCC_17	F20	DDR3_DQ42
IO_L11N_T1_SRCC_17	F22	DDR3_DQ44
IO_L11P_T1_SRCC_17	G22	DDR3_DM5
IO_L10N_T1_17	F18	DDR3_DQ46
IO_L10P_T1_17	G18	DDR3_DQ45
IO_L9N_T1_DQS_17	G19	DQS_N5
IO_L9P_T1_DQS_17	H19	DQS_P5
IO_L8N_T1_17	G20	DDR3_DQ40
IO_L8P_T1_17	H20	DDR3_DQ43
IO_L7N_T1_17	F23	DDR3_DQ47
IO_L7P_T1_17	G23	DDR3_DQ41
IO_L6N_T0_VREF_17	K18	VREF+0V75
IO_L6P_T0_17	L18	nc
IO_L5N_T0_17	J19	nc
IO_L5P_T0_17	J18	nc
IO_L4N_T0_17	K20	DIPSW3
IO_L4P_T0_17	K19	DIPSW4
IO_L3N_T0_DQS_17	J21	DIPSW7
IO_L3P_T0_DQS_17	K21	DIPSW2
IO_L2N_T0_17	H22	DIPSW8
IO_L2P_T0_17	J22	DIPSW6
IO_L1N_T0_17	J23	DIPSW5
IO_L1P_T0_17	K23	DIPSW1
IO_0_17	H21	FPGA_RESET_N

Table 13: Bank 111 – LLRF I/O – LLL0-3

Pin Name	Pin Location	Function
MGTXRXN0_111	AH9	CH0_RX_N
MGTXRXP0_111	AH10	CH0_RX_P
MGTXTXN0_111	AJ11	CH0_TX_N
MGTXTXP0_111	AJ12	CH0_TX_P
MGTXRXN1_111	AG11	CH1_RX_N
MGTXRXP1_111	AG12	CH1_RX_P
MGTXTXN1_111	AK9	CH1_TX_N
MGTXTXP1_111	AK10	CH1_TX_P
MGTREFCLK1N_111	AE7	nc

Pin Name	Pin Location	Function
MGTREFCLK1P_111	AE8	nc
MGTREFCLK0N_111	AC7	nc
MGTREFCLK0P_111	AC8	nc
MGTXRXN2_111	AF9	CH2_RX_N
MGTXRXP2_111	AF10	CH2_RX_P
MGTXTXN2_111	AJ7	CH2_TX_N
MGTXTXP2_111	AJ8	CH2_TX_P
MGTXRXN3_111	AE11	CH3_RX_N
MGTXRXP3_111	AE12	CH3_RX_P
MGTXTXN3_111	AG7	CH3_TX_N
MGTXTXP3_111	AG8	CH3_TX_P

Note: This bank is available with the XC7K420T only.

Table 14: Bank 112 – Zone3 Management

Pin Name	Pin Location	Function
MGTXRXN0_112	AH5	J31_MGT3_RX_N
MGTXRXP0_112	AH6	J31_MGT3_RX_P
MGTXTXN0_112	AK5	J31_MGT3_TX_N
MGTXTXP0_112	AK6	J31_MGT3_TX_P
MGTXRXN1_112	AG3	J31_MGT2_RX_N
MGTXRXP1_112	AG4	J31_MGT2_RX_P
MGTXTXN1_112	AJ3	J31_MGT2_TX_N
MGTXTXP1_112	AJ4	J31_MGT2_TX_P
MGTREFCLK1N_112	AF5	MGT112_CLK1_N
MGTREFCLK1P_112	AF6	MGT112_CLK1_P
MGTREFCLK0N_112	AD5	nc
MGTREFCLK0P_112	AD6	nc
MGTXRXN2_112	AE3	J31_MGT1_RX_N
MGTXRXP2_112	AE4	J31_MGT1_RX_P
MGTXTXN2_112	AK1	J31_MGT1_TX_N
MGTXTXP2_112	AK2	J31_MGT1_TX_P
MGTXRXN3_112	AC3	J31_MGT0_RX_N
MGTXRXP3_112	AC4	J31_MGT0_RX_P
MGTXTXN3_112	AH1	J31_MGT0_TX_N
MGTXTXP3_112	AH2	J31_MGT0_TX_P

Table 15: Bank 113 – Optical Data Transmission I/O – Lower Connector

Pin Name	Pin Location	Function
MGTXRXN0_113	AB5	LCage1_RX_N
MGTXRXP0_113	AB6	LCage1_RX_P
MGTXTXN0_113	AF1	LCage1_TX_N
MGTXTXP0_113	AF2	LCage1_TX_P
MGTXRXN1_113	AA3	LCage2_RX_N
MGTXRXP1_113	AA4	LCage2_RX_P
MGTXTXN1_113	AD1	LCage2_TX_N
MGTXTXP1_113	AD2	LCage2_TX_P
MGTREFCLK1N_113	W7	nc
MGTREFCLK1P_113	W8	nc
MGTREFCLK0N_113	U7	MGT113_CLK0_N
MGTREFCLK0P_113	U8	MGT113_CLK0_P
MGTXRXN2_113	Y5	LCage3_RX_N
MGTXRXP2_113	Y6	LCage3_RX_P
MGTXTXN2_113	AB1	LCage3_TX_N
MGTXTXP2_113	AB2	LCage3_TX_P
MGTXRXN3_113	W3	LCage4_RX_N
MGTXRXP3_113	W4	LCage4_RX_P
MGTXTXN3_113	Y1	LCage4_TX_N
MGTXTXP3_113	Y2	LCage4_TX_P

Table 16: Bank 114 – Optical Data Transmission I/O – Upper Connector

Pin Name	Pin Location	Function
MGTXRXN0_114	V5	UCage1_RX_N
MGTXRXP0_114	V6	UCage1_RX_P
MGTXTXN0_114	V1	UCage1_TX_N
MGTXTXP0_114	V2	UCage1_TX_P
MGTXRXN1_114	U3	UCage2_RX_N
MGTXRXP1_114	U4	UCage2_RX_P
MGTXTXN1_114	T1	UCage2_TX_N
MGTXTXP1_114	T2	UCage2_TX_P
MGTREFCLK1N_114	T5	nc
MGTREFCLK1P_114	T6	nc
MGTREFCLK0N_114	R7	MGT114_CLK0_N
MGTREFCLK0P_114	R8	MGT114_CLK0_P
MGTXRXN2_114	R3	UCage3_RX_N
MGTXRXP2_114	R4	UCage3_RX_P
MGTXTXN2_114	P1	UCage3_TX_N
MGTXTXP2_114	P2	UCage3_TX_P
MGTXRXN3_114	P5	UCage4_RX_N
MGTXRXP3_114	P6	UCage4_RX_P
MGTXTXN3_114	N3	UCage4_TX_N
MGTXTXP3_114	N4	UCage4_TX_P

Table 17: Bank 115 – LLRF I/O – LLL12-15

Pin Name	Pin Location	Function
MGTXRXN0_115	M5	CH0_RX_N
MGTXRXP0_115	M6	CH0_RX_P
MGTXTXN0_115	M1	CH0_TX_N
MGTXTXP0_115	M2	CH0_TX_P
MGTXRXN1_115	L3	CH1_RX_N
MGTXRXP1_115	L4	CH1_RX_P
MGTXTXN1_115	K1	CH1_TX_N
MGTXTXP1_115	K2	CH1_TX_P
MGTREFCLK1N_115	L7	nc
MGTREFCLK1P_115	L8	nc
MGTREFCLK0N_115	J7	nc
MGTREFCLK0P_115	J8	nc
MGTXRXN2_115	K5	CH2_RX_N
MGTXRXP2_115	K6	CH2_RX_P
MGTXTXN2_115	H1	CH2_TX_N
MGTXTXP2_115	H2	CH2_TX_P
MGTXRXN3_115	J3	CH3_RX_N
MGTXRXP3_115	J4	CH3_RX_P
MGTXTXN3_115	F1	CH3_TX_N
MGTXTXP3_115	F2	CH3_TX_P

Table 18: Bank 116 – PCIe I/O

Pin Name	Pin Location	Function
MGTXRXN0_116	G3	PCIE1_RX_N
MGTXRXP0_116	G4	PCIE1_RX_P
MGTXTXN0_116	D1	PCIE1_TX_N
MGTXTXP0_116	D2	PCIE1_TX_P
MGTXRXN1_116	E3	PCIE2_RX_N
MGTXRXP1_116	E4	PCIE2_RX_P
MGTXTXN1_116	B1	PCIE2_TX_N
MGTXTXP1_116	B2	PCIE2_TX_P
MGTREFCLK1N_116	H5	MGT116_CLK1_N
MGTREFCLK1P_116	H6	MGT116_CLK1_P
MGTREFCLK0N_116	F5	MGT116_CLK0_N
MGTREFCLK0P_116	F6	MGT116_CLK0_P
MGTXRXN2_116	D5	PCIE3_RX_N
MGTXRXP2_116	D6	PCIE3_RX_P
MGTXTXN2_116	A3	PCIE3_TX_N
MGTXTXP2_116	A4	PCIE3_TX_P
MGTXRXN3_116	C3	PCIE4_RX_N
MGTXRXP3_116	C4	PCIE4_RX_P
MGTXTXN3_116	B5	PCIE4_TX_N
MGTXTXP3_116	B6	PCIE4_TX_P

Table 19: Bank 117 – LLRF I/O – LLL8-11

Pin Name	Pin Location	Function
MGTXRXN0_117	F9	CH0_RX_N
MGTXRXP0_117	F10	CH0_RX_P
MGTXTXN0_117	C7	CH0_TX_N
MGTXTXP0_117	C8	CH0_TX_P
MGTXRXN1_117	D9	CH1_RX_N
MGTXRXP1_117	D10	CH1_RX_P
MGTXTXN1_117	A7	CH1_TX_N
MGTXTXP1_117	A8	CH1_TX_P
MGTREFCLK1N_117	G7	nc
MGTREFCLK1P_117	G8	nc
MGTREFCLK0N_117	E7	nc
MGTREFCLK0P_117	E8	nc
MGTXRXN2_117	E11	CH2_RX_N
MGTXRXP2_117	E12	CH2_RX_P
MGTXTXN2_117	B9	CH2_TX_N
MGTXTXP2_117	B10	CH2_TX_P
MGTXRXN3_117	C11	CH3_RX_N
MGTXRXP3_117	C12	CH3_RX_P
MGTXTXN3_117	A11	CH3_TX_N
MGTXTXP3_117	A12	CH3_TX_P

4.4 RTM Channel Definition

Table 20: RTM Channel Definition

Channel	Signal	Characteristic	Description
J30 Zone3 Connector			
J30-3A/3B	Clock (f = configurable)	LVDS / output	General purpose clock from PLL Generated by AMC
J30-4A/4B	Clock TCKLA	LVDS / output	TCLKA from AMC backplane From MCH
J30-3C/3D	Clock (f = 81.25 / 162.5 MHz)	LVDS / input	General purpose clock derived from MO Generated by RTM
J30-3E/3F	nc	LVDS / output	-
J30-4C/4D	Interlock 0	LVDS / output	Non-programmable interlock logic Hardwired to MLVDS bus
J30-4E/4F	Interlock 1	LVDS / output	Non-programmable interlock logic Hardwired to MLVDS bus
J30-5A to 10F	Digital I/Os	LVDS / programmable via FPGA	General purpose digital I/Os Clock capable pins: 5A/5B, 6A/6B, 9A/9B, 10A/10B
J31 Zone 3 Connector			
J31-1A-6F, 7A-8B	Digital I/Os	LVDS / programmable via FPGA	General purpose digital I/Os Clock capable pins: 7A/7B, 8A/8B
J31-10C/10D/10E/10F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 0
J31-9C/9D/9E/9F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 1
J31-8C/8D/8E/8F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 2

Channel	Signal	Characteristic	Description
J31-7C/7D/7E/7F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 3
J31-9A/9B	Clock (Xilinx GTX)	LVDS / input	Reference clock for GTX transceiver Generated by RTM, connected to GTX tile
J31-10A/10B	Clock (Xilinx GTX)	LVDS / output	Reference clock for GTX transceiver Generated by AMC, output from PLL
IPMI Signals			
J30-1A/1B/2A/2B	PP +12V	RTM power supply	Payload power 3A max.
J30-2C	MP +3V3	RTM power supply	Management power 30 mA max.
J30-1C	RTM_Presence	LVCMOS (3.3V)	Presence detection (negative) MMC
J30-1D/2D	I²C	LVCMOS (3.3V)	MAIN IPMI bus (SCL/SDA) MMC
J30-1E/1F/2E/2F	JTAG	LVCMOS (3.3V)	JTAG signals for FPGA and PROM Switch shorting TDO/TDI controlled my MMC

4.5 Front Panel & LEDs

The **NAMC-TCK7** is equipped with the standard AMC LEDs and additionally features two indicator LEDs at each SFP+-Bay. For further explanation see table below.

Figure 5: NAMC-TCK7 – Front Panel

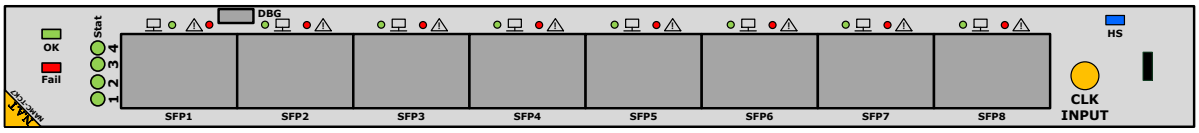


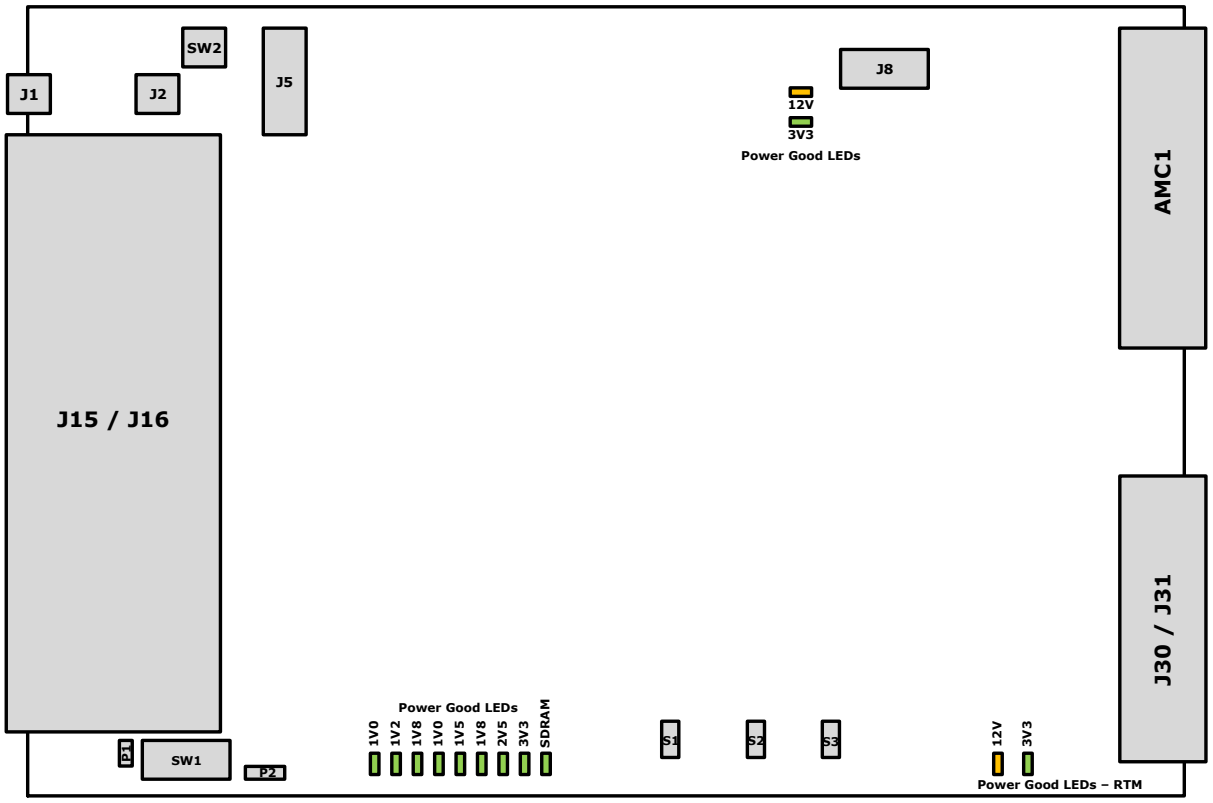
Table 21: LED Description

LED	Colour	Function	Control
SFP+1..8	green	Link presence	FPGA
SFP+1..8	red	Fault indication	FPGA
OK	green	Board status	IPMI
Fail	red	Board fault indication	IPMI
HS	blue	Hot-Swap status	IPMI
Stat1..4	green	Application free use	FPGA

4.6 Connectors, Switches and on-board LEDs

The following figure shows a connector diagram of the **NAMC-TCK7**.

Figure 6: NAMC-TCK7 – Connector Diagram



4.6.1 AMC1: AMC Connector

Table 22: AMC1: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	VCC+12V	TDI	169
3	PS1	TDO	168
4	VCC+3V3_MP	TRST'	167
5	GA0	TMS	166
6	RSRVD6	TCK	165
7	GND	GND	164
8	RSRVD8	AMC_INTERLOCK2_P	163
9	VCC+12V	AMC_INTERLOCK2_N	162
10	GND	GND	161
11	AMC_LLL0_TX_P	AMC_INTERLOCK1_P	160
12	AMC_LLL0_TX_N	AMC_INTERLOCK1_N	159
13	GND	GND	158
14	AMC_LLL0_RX_P	AMC_INTERLOCK0_P	157
15	AMC_LLL0_RX_N	AMC_INTERLOCK0_N	156
16	GND	GND	155
17	GA1	AMC_CRYO_OK_P	154
18	VCC+12V	AMC_CRYO_OK_N	153
19	GND	GND	152
20	AMC_LLL1_TX_P	AMC_CLK_AUX_P	151
21	AMC_LLL1_TX_N	AMC_CLK_AUX_N	150
22	GND	GND	149
23	AMC_LLL1_RX_P	AMC_TRGREADOUT_P	148
24	AMC_LLL1_RX_N	AMC_TRGREADOUT_N	147
25	GND	GND	146
26	GA2	AMC_TRGEND_P	145
27	VCC+12V	AMC_TRGEND_N	144
28	GND	GND	143
29	AMC_LLL2_TX_P	AMC_TRGSTART_P	142
30	AMC_LLL2_TX_N	AMC_TRGSTART_N	141
31	GND	GND	140
32	AMC_LLL2_RX_P	TCLKD_P	139
33	AMC_LLL2_RX_N	TCLKD_N	138
34	GND	GND	137
35	AMC_LLL3_TX_P	TCLKC_P	136
36	AMC_LLL3_TX_N	TCLKC_N	135
37	GND	GND	134
38	AMC_LLL3_RX_P	AMC_LLL15_TX_P	133
39	AMC_LLL3_RX_N	AMC_LLL15_TX_N	132
40	GND	GND	131
41	ENABLE_N	AMC_LLL15_RX_P	130
42	VCC+12V	AMC_LLL15_RX_N	129
43	GND	GND	128
44	AMC_PCIE1_TX_P	AMC_LLL14_TX_P	127
45	AMC_PCIE1_TX_N	AMC_LLL14_TX_N	126

Pin #	AMC-Signal	AMC-Signal	Pin #
46	GND	GND	125
47	AMC_PCIE1_RX_P	AMC_LLL14_RX_P	124
48	AMC_PCIE1_RX_N	AMC_LLL14_RX_N	123
49	GND	GND	122
50	AMC_PCIE2_TX_P	AMC_LLL13_TX_P	121
51	AMC_PCIE2_TX_N	AMC_LLL13_TX_N	120
52	GND	GND	119
53	AMC_PCIE2_RX_P	AMC_LLL13_RX_P	118
54	AMC_PCIE2_RX_N	AMC_LLL13_RX_N	117
55	GND	GND	116
56	SCL_L	AMC_LLL12_TX_P	115
57	VCC+12V	AMC_LLL12_TX_N	114
58	GND	GND	113
59	AMC_PCIE3_TX_P	AMC_LLL12_RX_P	112
60	AMC_PCIE3_TX_N	AMC_LLL12_RX_N	111
61	GND	GND	110
62	AMC_PCIE3_RX_P	AMC_LLL11_TX_P	109
63	AMC_PCIE3_RX_N	AMC_LLL11_TX_N	108
64	GND	GND	107
65	AMC_PCIE4_TX_P	AMC_LLL11_RX_P	106
66	AMC_PCIE4_TX_N	AMC_LLL11_RX_N	105
67	GND	GND	104
68	AMC_PCIE4_RX_P	AMC_LLL10_TX_P	103
69	AMC_PCIE4_RX_N	AMC_LLL10_TX_N	102
70	GND	GND	101
71	SDA_L	AMC_LLL10_RX_P	100
72	VCC+12V	AMC_LLL10_RX_N	99
73	GND	GND	98
74	TCLK_A_P	AMC_LLL9_TX_P	97
75	TCLK_A_N	AMC_LLL9_TX_N	96
76	GND	GND	95
77	TCLK_B_P	AMC_LLL9_RX_P	94
78	TCLK_B_N	AMC_LLL9_RX_N	93
79	GND	GND	92
80	FCLK_P	AMC_LLL8_TX_P	91
81	FCLK_N	AMC_LLL8_TX_N	90
82	GND	GND	89
83	PS0	AMC_LLL8_RX_P	88
84	VCC+12V	AMC_LLL8_RX_N	87
85	GND	GND	86

4.6.2 J1: Reference Clock Input

SMB Connector J1 features a reference clock input.

Table 23: J1: Reference Clock Input – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RF_Ref_CLK_IN	GND	2

4.6.3 J2: MMC JTAG Header

Pin Header J2 connects to the JTAG-programming-port of the Atmel µC device.

Table 24: J2: MMC JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MMC_TCK	GND	2
3	MMC_TDO	VCC+3V3_MMC	4
5	MMC_TMS	MMC_RESET_N	6
7	nc	nc	8
9	MMC_TDI	GND	10

4.6.4 J5: Main JTAG Header

Pin Header J5 offers a standard XILINX programming interface to access the FPGA and CPLD via JTAG.

Table 25: J5: Main JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	VCC+3V3	2
3	GND	JTAG_CONN_TMS	4
5	GND	JTAG_CONN_TCK	6
7	GND	JTAG_CONN_TDO	8
9	GND	JTAG_CONN_TDI	10
11	GND	nc	12
13	GND	nc	14

4.6.5 J8: Power Supply Debug Connector

Pin Header J8 features a power supply option if the **NAMC-TCK7** is operated outside a chassis.

Table 26: J8: Power Supply Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC+12V	GND	2
3	VCC+3V3	-	-

4.6.6 J15/16: SFP Connectors

Connectors J15/J16 offer low-latency connections via optical fibre.

Table 27: J3: SFP Connector J15/J16 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	TX_FAULT	2
3	TX_DISABLE	SDA	4
5	SCL	MOD_ABS	6
7	RS0	RX_LOS	8
9	RS1	GND	10
11	GND	RX_N	12
13	RX_P	GND	14
15	VCCR	VCCT	16
17	GND	TX_P	18
19	TX_N	GND	20

4.6.7 J30: RTM Connector

Table 28: J30: RTM Connector – Pin-Assignment

	a	b	ab	c	d	cd	e	f	ef
1	PWR+12V	PWR+12V	GND	MP+3.3V	RTM_SDA	GND	TCKL	TDO	GND
2	PWR+12V	PWR+12V	GND	GND	RTM_SCL	GND	TDI	TMS	GND
3	AMC_CLK_P	AMC_CLK_N	GND	RTM_CLK_P	RTM_CLK_N	GND	nc	nc	GND
4	AMC_TCLK_P	AMC_TCLK_N	GND	INT_0_P	INT_0_N	GND	INT_1_P	INT_1_N	GND
5	IO1_CC_P	IO1_CC_N	GND	IO2_P	IO2_N	GND	IO3_P	IO3_N	GND
6	IO4_CC_P	IO4_CC_N	GND	IO5_P	IO5_N	GND	IO6_P	IO6_N	GND
7	IO7_P	IO7_N	GND	IO8_P	IO8_N	GND	IO9_P	IO9_N	GND
8	IO10_P	IO10_N	GND	IO11_P	IO11_N	GND	IO12_P	IO12_N	GND
9	IO13_CC_P	IO13_CC_N	GND	IO14_P	IO14_N	GND	IO15_P	IO15_N	GND
10	IO16_CC_P	IO16_CC_N	GND	IO17_P	IO17_N	GND	IO18_P	IO18_N	GND

4.6.8 J31: RTM Connector

Table 29: J31: RTM Connector – Pin-Assignment

	a	b	ab	c	d	cd	e	f	ef
1	IO1_P	IO1_N	GND	IO2_P	IO2_N	GND	IO3_P	IO3_N	GND
2	IO4_P	IO4_N	GND	IO5_P	IO5_N	GND	IO6_P	IO6_N	GND
3	IO7_P	IO7_N	GND	IO8_P	IO8_N	GND	IO9_P	IO9_N	GND
4	IO10_P	IO10_N	GND	IO11_P	IO11_N	GND	IO12_P	IO12_N	GND
5	IO13_P	IO13_N	GND	IO14_P	IO14_N	GND	IO15_P	IO15_N	GND
6	IO16_P	IO16_N	GND	IO17_P	IO17_N	GND	IO18_P	IO18_N	GND
7	IO19_CC_P	IO19_CC_N	GND	MGT3_TX_P	MGT3_TX_N	GND	MGT3_RX_P	MGT3_RX_N	GND
8	IO20_CC_P	IO20_CC_N	GND	MGT2_TX_P	MGT2_TX_N	GND	MGT2_RX_P	MGT2_RX_N	GND
9	RTM_MGT_P	RTM_MGT_N	GND	MGT1_TX_P	MGT1_TX_N	GND	MGT1_RX_P	MGT1_RX_N	GND
10	AMC_MGT_P	AMC_MGT_N	GND	MGT0_TX_P	MGT0_TX_N	GND	MGT0_RX_P	MGT0_RX_N	GND

4.6.9 P1: MMC Debug Header

Shortening the Pins of P1 enables the MMC for operation outside a chassis – for debugging purposes only.

4.6.10 P2: JTAG Chain Header

The configuration of JTAG Chain Header P2 determines which device is addressed.

Pin 1-2 connected – FPGA
Pin 2-3 connected – CPLD

4.6.11 S1: MMC Reset Switch

S1 resets the MMC.

4.6.12 S2: FPGA Reset Switch

S2 resets the FPGA.

4.6.13 S3: FPGA Configuration Switch

S3 reloads the FPGA.

4.6.14 SW1: FPGA Configuration Switch

This DIP switch is connected to FPGA Bank17 pins and can be used for any FPGA design specific functionality.

Table 30: SW1 DIP-Switch Configuration

	ON	OFF
SW1-1	tbd	tbd
SW1-2	tbd	tbd
SW1-3	tbd	tbd
SW1-4	tbd	tbd
SW1-5	tbd	tbd
SW1-6	tbd	tbd
SW1-7	tbd	tbd
SW1-8	tbd	tbd

4.6.15 SW2: Hot Swap Switch

Switch SW2 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

5 Board Specification

Table 31: NAMC-TCK7 – Features – Overview

FPGA	XILINX Kintex-7 FPGA (XC7K355T or XC7420T)
AMC-Module	Advanced Mezzanine Card, double width, mid-size with full-size-option
RAM	DDR3 SDRAM (256M x 64 bit)
PROM	QSPI FLASH (2x 256 Mbit)
Firmware	na
Power Consumption	12V / 6.5A
Operating Temperature	0°C – +50°C with forced cooling
Storage Temperature	-40°C - +90°C
Humidity	5% – 90% rh non-condensing
Standards compliance	AMC.0, AMC.1, AMC.2, MTCA.4 IMPI V2.0 MMC V1.0 compatible

6 Installation

6.1 Safety Note

To ensure proper functioning of the **NAMC-TCK7** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-TCK7** read this installation section
- Before installing or uninstalling the **NAMC-TCK7**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-TCK7** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-TCK7** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

6.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

6.2.1 Requirements

The installation requires only
- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-TCK7** power supply
- cooling devices

6.2.2 Power supply

The power supply for the **NAMC-TCK7** must meet the following specifications:
- required for the module:
  - +12V / 6.5A max.

6.2.3 Automatic Power Up

In the following situations the **NAMC-TCK7** will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.

6.3 Statement on Environmental Protection

6.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.3.4 Product Safety

The board complies with EN60950 and UL1950.

6.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] XILINX 7 Series FPGAs Data Sheet, DS180 (v2.6) 02/2018
[2] XILINX XC2C256 CoolRunner-II CPLD, DS094 (v3.2) 03/2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	21.06.2018	Initial Release	se
1.1	11.09.2018	Block diagram updated Information on GTX-Transceiver-Assignment added Minor changes on layout	se
1.2	14.08.2019	Moved "GTX-Transceiver-Assignment" to chapter 4 Added chapter 4.2 FPGA Pin-Out	se