NAMC-xE1
Telecom AMC Module
Technical Reference Manual V1.3
HW Revision 1.1

The NAMC-xE1 has been designed by:

N.A.T. GmbH
Konrad-Zuse-Platz 9
D-53227 Bonn

Phone: +49 / 228 / 965 864 - 0

Internet: http://www.nateurope.com

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
AMC	Advanced Mezzanine Card
ASIC	Application Specific Integrated Circuit
CPU	Central Processing Unit
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
µTCA	Micro Telecommunications Computing Architecture
PCI	Peripheral Component Interconnect
PCIe	PCI Express
RAM	Random Access Memory
ROM	Read Only Memory
SerDes	Serializer-Deserializer

1 Introduction

The **NAMC-xE1** is an E1/T1/J1 line interface card in AMC (Advanced Mezzanine Card) form factor. Beside the line interfaces it features a powerful FPGA for offering flexible data path and control path options.

The **NAMC-xE1** is available as a single compact-, a single mid-, or a single full-size module. The full-size version can be equipped with an additional extension board to increase the line interface count up to 16 E1/T1/J1.

2 Overview

2.1 Major Features

The **NAMC-xE1** has the following major features implemented on-board:

- Lattice ECP3 FPGA
- Dual 32Mbit QDR2 SRAM external to FPGA (optional)
- Fat Pipe Interface at Ports 4 / 8 with option for PCIe / SRIO / GbE
- 2 x Gigabit Ethernet to AMC Ports 0 / 1
- 8 x E1/T1/J1 Primary Rate Line Interfaces on base board
- Additional 8x E1/T1/J1 Primary Rate Line Interfaces on extension board
- iTDM Interface
  - 1024 bidirectional 64kbit/s channels
  - 125µs-mode and 1ms-mode support (mixture possible)
- Ethernet Control Interface: Both data and control path via Ethernet
- Optional: H.110 alike Backplane TSI bus
- Front panel height either Compact- / Mid- or Full-Size AMC

For detailed description see the following chapter.

2.2 Block Diagram

Figure 1 shows a detailed block diagram of the **NAMC-xE1** (8 Ports). If the extension module is added (only available for full-size face plate), 8 additional line interface ports are added (Figure 2).

Figure 1: **NAMC-xE1 – Block Diagram – Base Board**

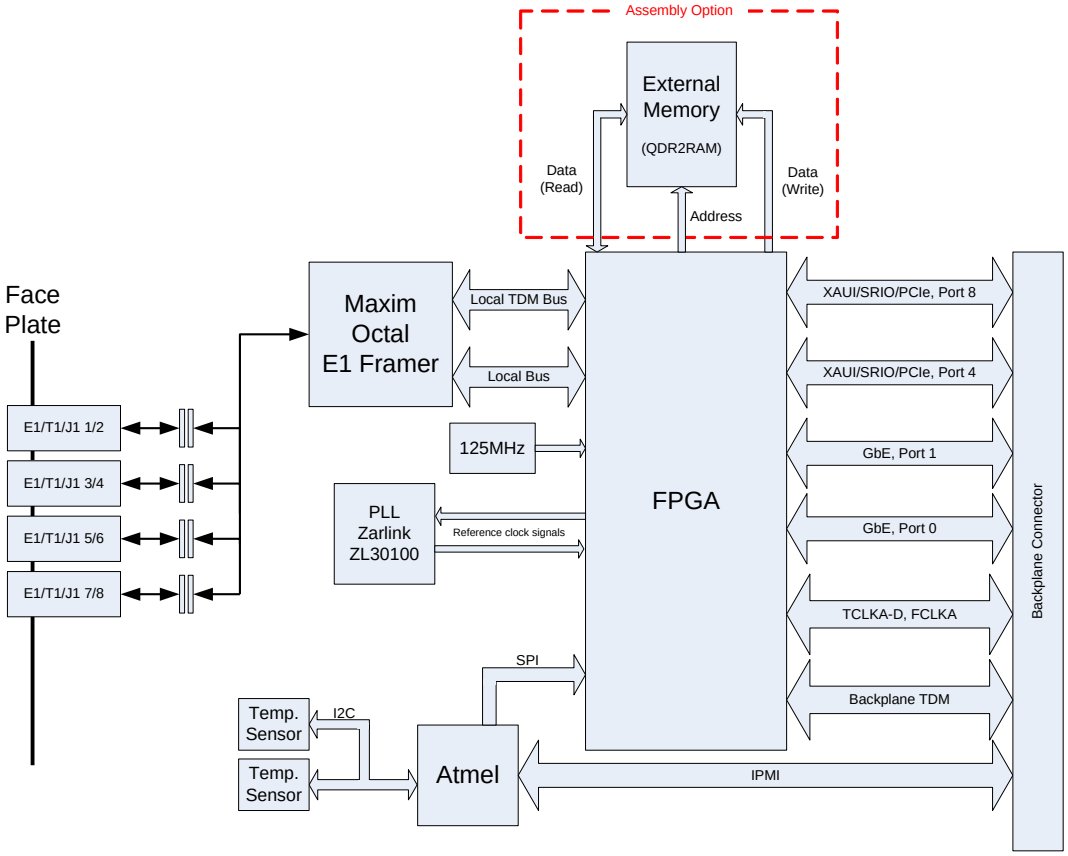
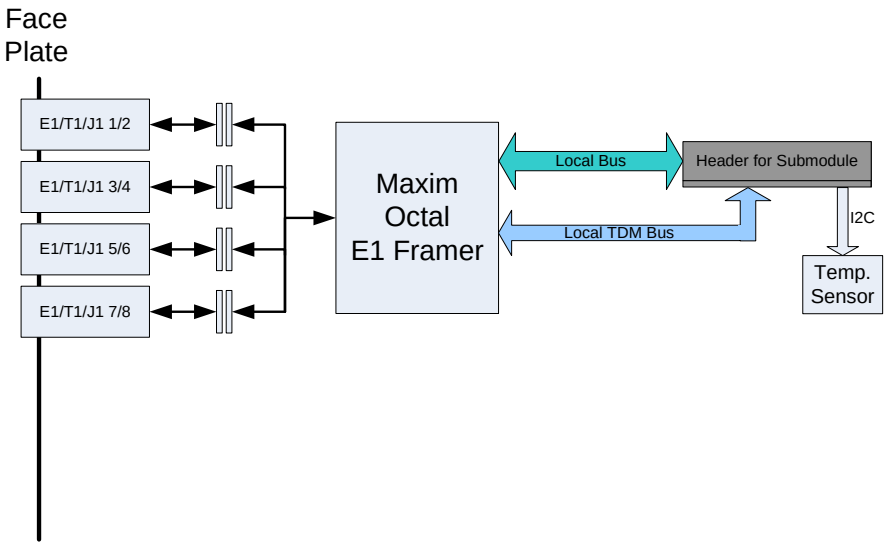


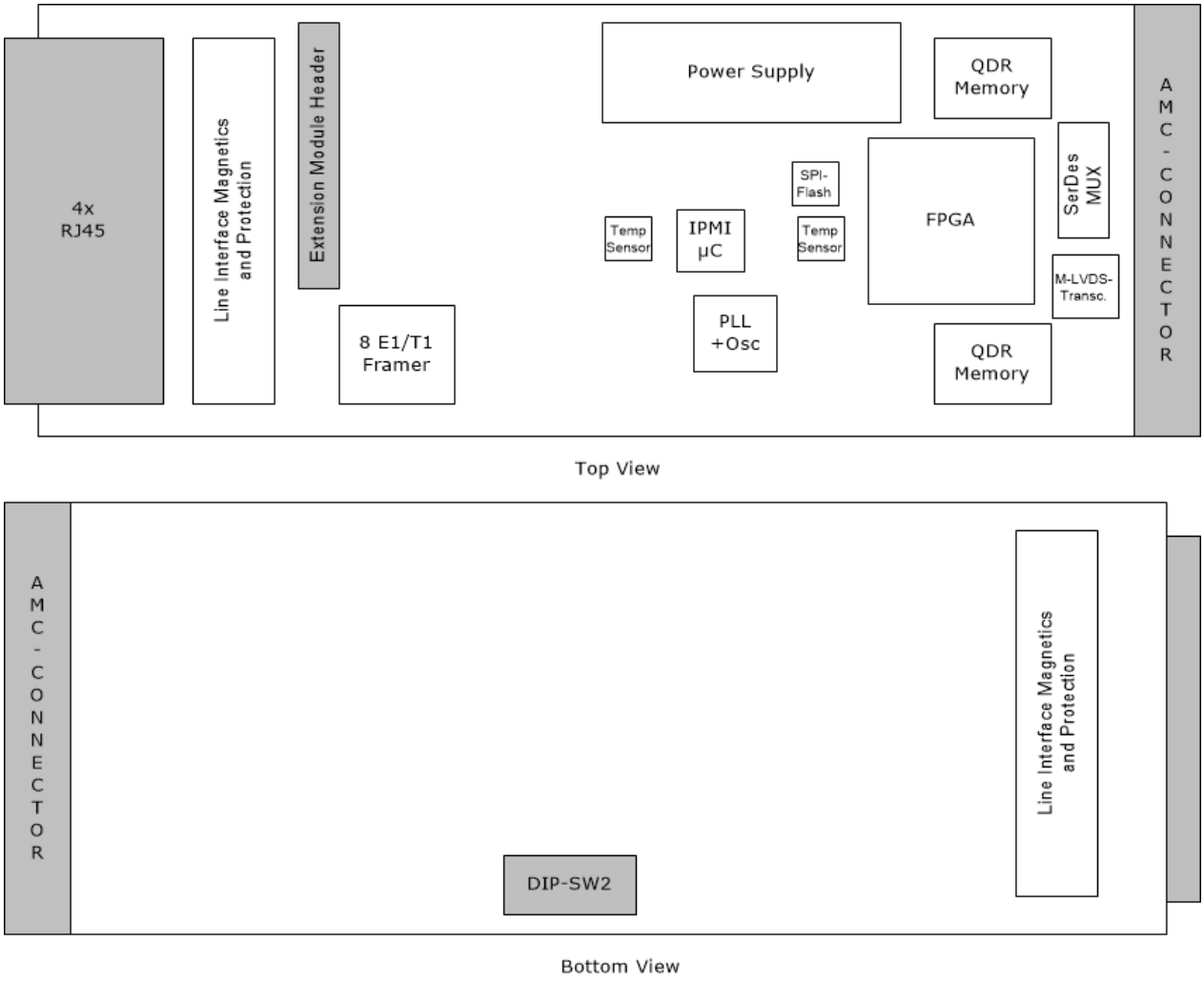
Figure 2: **NAMC-xE1 – Block Diagram – Extension Board**



2.3 Location Diagram

Figure 3 shows the position of important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: **NAMC-xE1 – Location Diagram – Base Board**



3 Board Features

The **NAMC-xE1** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 FPGA

The Lattice ECP3 FPGA is a versatile programmable logic device that integrates on one chip high-performance logic elements, a large amount of SRAM memory, and a flexible SerDes unit.

The standard FGPA image for the **NAMC-xE1** implements two main functionalities:

- ITDM Engine
  Realizes data path from the line interfaces to the application specific destination.
- Ethernet Control Interface
  Realizes control path from a controlling host instance that runs the driver to the board' devices.

3.2 Memory

3.2.1 FPGA internal memory

The FPGA offers 4Mbit internal SRAM memory for general usage.

3.2.2 QDR2 SRAM

Two QDR2 SRAM memory devices – default size 32 MB - can be assembled on the **NAMC-xE1** (optional). Each of these devices is 8 bit wide and offers simultaneous read and write access for realizing buffering functionality.
The interface to the QDR2 SRAM is implemented in the FPGA and is application specific. The regular iTDM FPGA implementation does not need this additional memory, it comes along with the FPGA internal memory. So these two devices are used for customer specific functionality.

3.2.3 FLASH

The FPGA loads its configuration from a serial SPI Flash memory device. This memory is also used to store additional information like the board's serial number and release code. It can further be used to store application specific data that has to be kept non-volatile.

3.3 PCI Express and SRIO Interface

The ECP3 FPGA has four of its SerDes lanes connected to the backplane, which is used to equip the **NAMC-xE1** with GbE, PCIe, SRIO or a combination of them. The configuration options include the following:

- PCIe x1 on Port 4 or Port 8
- SRIO x1 on Ports 4 and/or Port 8; Speed 1,25Gb/s or 2,5Gb/s
- PCIe x1 on Port 4 and SRIO x1 on Port 8; Speed 2,5Gb/s
- GbE on Port 0 and/or Port 1

3.4 Backplane Ethernet

The FPGA internal SerDes Ethernet is connected to the further logic through two GMII interfaces, which are routed through the FPGA. Within FPGA logic the control Ethernet data is multiplexed with the iTDM data and transferred through the same physical port.

3.5 iTDM

Main task of the FPGA residing on the **NAMC-xE1** is offering a powerful TDM to iTDM conversion engine to the board. For the on-board TDM devices, the extension PCB and the framer, it implements 1024 bidirectional iTDM channels that can be used for either connecting framer or extension PCB channels to destinations outside the board. The iTDM engine shares the Ethernet path with the Ethernet Control Interface by doing arbitration for iTDM packets to be sent and for control Ethernet packets to be sent.

3.6 Ethernet Control Interface

The standard FPGA image for the **NAMC-xE1** offers the control path to be operated via the basic Common Options Ethernet on AMC Port 0/1. This enables the system designer to build very cost effective systems with no need for an additional system fabric in the AMC Fat Pipe Region.
The Ethernet Control Interface (ECI) is based on regular Layer2 Ethernet. It is used to encapsulate memory mapped accesses from a host instance into Ethernet frames. The main functional key elements are the following ones:

- Based on regular Layer2 Ethernet
- Simple and reliable Error detection mechanism for assured memory accesses
- Read-Modify-Write operation with one access cycle
  - Perform logical AND
  - Perform logical OR
- Variable data width of 1/2/4 Bytes
- Reading of one or multiple data word(s)
- Writing of one or multiple data word(s)

Options:

- Transmitting IRQ over Ethernet
- Performing DMA over Ethernet

For additional information please ask N.A.T. for driver code and extended documentation.

3.7 Backplane TDM

The **NAMC-xE1** implements an 8-bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz. Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. It bridges to a module-internal TDM bus, which connects to the extension PCB TDM lines and to the DS26518 framer. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Extended Options Region of the AMC connector.

3.8 E1/T1/J1 Line Interfaces

The eight E1/T1/J1 interfaces connect the Maxim/Dallas DS26518 framer to the front panel RJ45 connectors. Timing and interface characteristics can be set up by software within the DS26518. The line interfaces conform to EN60950 and G.703 / G.823 (Jitter Attenuation). The front panel RJ45 connector consists of 4 RJ45 jacks, stacked 4 x 1, with integrated LED. In order to support 8 E1/T1/J1 interfaces each RJ45 jack carries 2 E1/T1/J1 interfaces. The LEDs are bi-coloured and programmable through registers which reside within the FPGA.
By equipping the **NAMC-xE1** with an additional extension board, the number of available E1/T1/J1 interfaces raises to 16.

3.9 AMC Clock Interface

The **NAMC-xE1** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D and FCLKA.

All TCLK ports are connected directly to the FPGA and can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from the line interfaces or to synchronize the **NAMC-xE1** to an external clock.

AMC backplane clock port FCLKA is connected to a multiplexer, which allows programming the clock source of the SerDes reference clock input to be either sourced from FCLKA, or an internal differential reference clock.

3.10 IPMB Interface

The **NAMC-xE1** implements an IPMB interface consisting of an AVRmega16 microcontroller and a couple of I2C devices, such as a temperature sensor, and an EEPROM. The IPMB controller manages also the hot swap functionality and the geographical address as requested by the AMC specification.

4 Hardware

4.1 AMC Port Definition

Table 2: AMC Port Mapping Strategy

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and Control Ethernet), default
	1		1000BaseX Ethernet Channel 2 (iTDM and Control Ethernet), redundant
	2		Unassigned
	3		Unassigned
	4	Fat Pipes	FGPA SerDes Lane 3
	5		Unassigned
	6		Unassigned
	7		Unassigned
Extended Connector	8	Region	FPGA SerDes Lane 4
	9		Unassigned
	10		Unassigned
	11		Unassigned
	12	Extended Options Region	TDM Bus D0-3 (H.110 extended)
	13		TDM Bus D4-7 (H.110 extended)
	14		optional clock lines (H.110 extended)/ unassigned
	15		Unassigned
	16		TCLKC / TCLKD
	17		Unassigned
	18		Unassigned
	19		Unassigned
	20		Unassigned

4.2 Front Panel and LED

The **NAMC-xE1** module is equipped with 8 LED integrated in the RJ45 interface jacks. For the case the extension module is present there are additional 8 LED in the second row of RJ45 jacks. All these LED are controlled via the FPGA and can be assigned with any functionality.

Additionally, the module contains the standard AMC LED consisting of a fault indication LED controlled by the IPMI controller and a general purpose status LED controlled by the FPGA.

Figure 4: **NAMC-xE1 – Front Panel – Base Board (8 Port)**

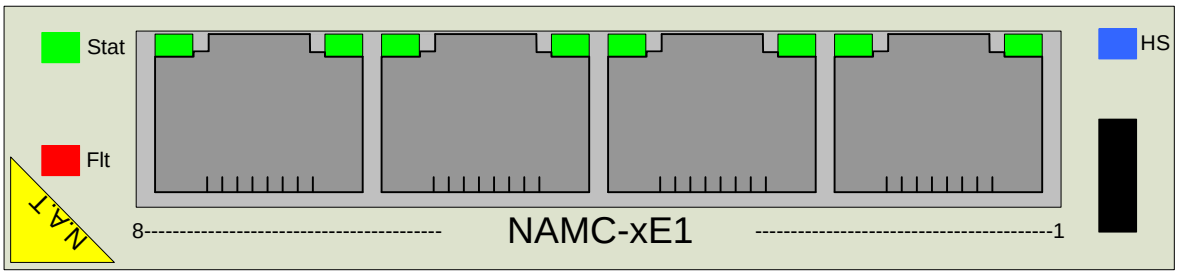
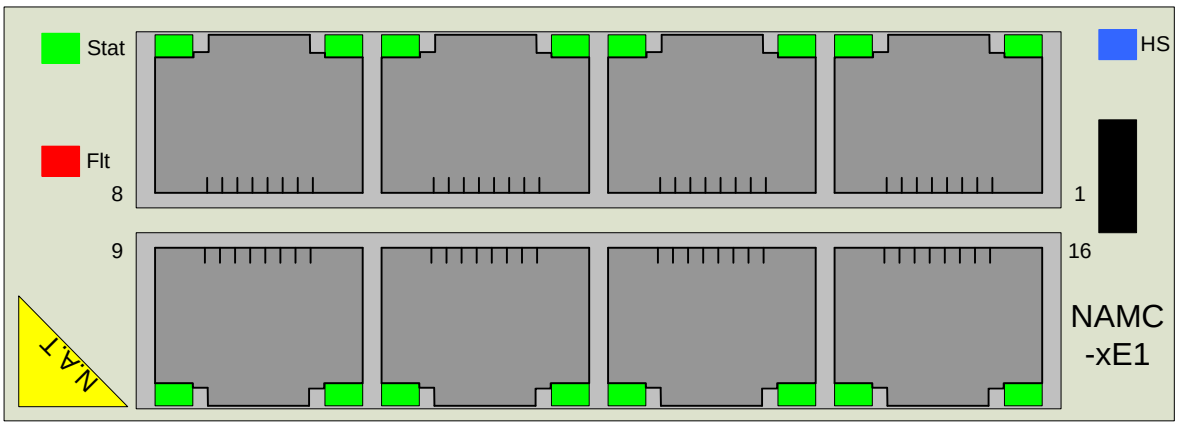
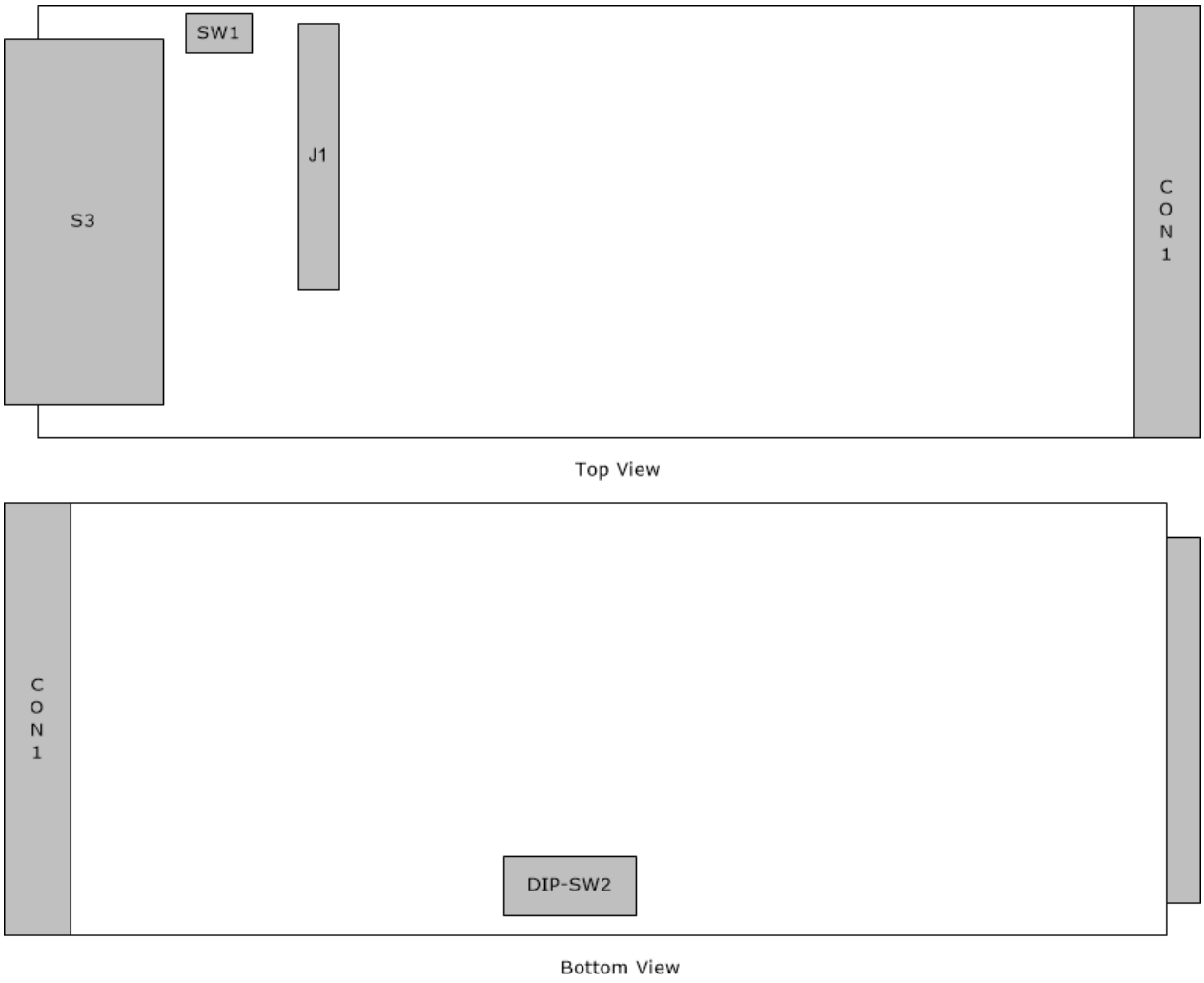


Figure 5: **NAMC-xE1 – Front Panel – Extension Board (16 Port)**



4.3 Connectors

Figure 6: **NAMC-xE1 – Connector and Switch Location – Base Board**



Please refer to the following tables to look up the connector pin assignment of the **NAMC-xE1**.

4.3.1 CON1: AMC Connector

Table 3: CON1: AMC Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	NC	163
9	PWR	NC	162
10	GND	GND	161
11	PORT0_TX_P	NC	160
12	PORT0_TX_N	NC	159
13	GND	GND	158
14	PORT0_RX_P	NC	157
15	PORT0_RX_N	NC	156
16	GND	GND	155
17	GA1	NC	154
18	PWR	NC	153
19	GND	GND	152
20	PORT1_TX_P	NC	151
21	PORT1_TX_N	NC	150
22	GND	GND	149
23	PORT1_RX_P	NC	148
24	PORT1_RX_N	NC	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	TCLKD_P	139
33	NC	TCLKD_N	138
34	GND	GND	137
35	NC	TCLKC_P	136
36	NC	TCLKC_N	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PORT4_TX_P	RESVD	127
45	PORT4_TX_N	TDM_REF	126

Pin #	AMC-Signal	AMC-Signal	Pin #
46	GND	GND	125
47	PORT4_RX_P	TDM_FS	124
48	PORT4_RX_N	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	NC	TDM5	118
54	NC	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	TCLKA_P	NC	97
75	TCLKA_N	NC	96
76	GND	GND	95
77	TCLKB_P	NC	94
78	TCLKB_N	NC	93
79	GND	GND	92
80	FCLKA_P	PORT8_TX_P	91
81	FCLKA_N	PORT8_TX_N	90
82	GND	GND	89
83	/PS0	PORT8_RX_P	88
84	PWR	PORT8_RX_N	87
85	GND	GND	86

4.3.2 J1: Extension Module Connector

Connector J1 connects to an extension module mounted on the **NAMC-xE1** and is used for initial programming of the board.

Table 4: J1: Extension Module Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	SGND	+12V	2
3	NC	+12V	4
5	NC	GND	6
7	GND	PS1_PIGGYn	8
9	SCL_INT	SDA_INT	10
11	RJ45_LED1_P	RJ45_LEDA_P	12
13	RJ45_LED2_P	RJ45_LEDB_P	14
15	FPGA_TDI	RJ45_LEDC_P	16
17	FPGA_DONE	RJ45_LEDD_P	18
19	FPGA_TDO	CPU_TDO	20
21	/PROGRAMN	CPU_TDI	22
23	FPGA_TMS	CPU_TCK	24
25	FPGA_TCK	CPU_TMS	26
27	INITN	CPU_/SRESET	28
29	ATMEL_MISO	CPU_/HRESET	30
31	ATMEL_MOSI	/CKSTP_OUT	32
33	ATMEL_SCK	/CKSTP_IN	34
35	/RST_IPMI	UART_Rx	36
37	DS2_REFCLKIO	UART_Tx	38
39	DS2_TSERCLK	RS232_Presense	40
41	GND	/CPU_TRST	42
43	DS2_RMSYNC1	DS_TXEN	44
45	DS2_RMSYNC2	/LCS6	46
47	DS2_RMSYNC3	/LCS7	48
49	DS2_RMSYNC4	/LWE1	50
51	DS2_RMSYNC5	LA11	52
53	DS2_RMSYNC6	LA12	54
55	DS2_RMSYNC7	LA13	56
57	DS2_RMSYNC8	LA14	58
59	GND	GND	60
61	VCC_IPMB	USB_RXD	62
63	NC	GND	64
65	UCC1_MDIO	USB_TP	66
67	UCC1_MDC	USB_TN	68
69	DS2_MCLK	USB_/OE	70
71	DS2_/RESET	USB_RP	72
73	DS2_TSSYNCIO	USB_RN	74
75	DS2_/INT	GND	76
77	DS2_TSYSCLK	DS2_RSER1	78
79	GND	GND	80
81	DS2_TSER1	DS2_RSYSCLK	82
83	GND	GND	84
85	DS2_TSYNC	DS2_RSYNC	86

Pin #	Signal	Signal	Pin #
87	GND	GND	88
89	DS2_TSIG1	DS2_RSIG1	90
91	GND	GND	92
93	LAD0	DS2_/CSB	94
95	LAD1	/LOE	96
97	LAD2	/LWE0	98
99	LAD3	LA18	100
101	LAD4	LA19	102
103	LAD5	LA20	104
105	LAD6	LA21	106
107	LAD7	LA22	108
109	LA15	LA23	110
111	LA16	LA24	112
113	LA17	LA25	114
115	GND	LA26	116
117	+3.3V	LA27	118
119	+3.3V	GND	120

4.3.3 S3: Front-Panel-Connector: RJ45 E1/T1/J1

Connector S3 offers access to the 8 E1/T1/J1 interfaces.

Table 5: S3D: Front-Panel Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX1+	RX1-	2
3	RX2+	TX1+	4
5	TX1-	RX2-	6
7	TX2+	TX2-	8

Table 6: S3C: Front-Panel Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX3+	RX3-	2
3	RX4+	TX3+	4
5	TX3-	RX4-	6
7	TX4+	TX4-	8

Table 7: S3B: Front-Panel Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX5+	RX5-	2
3	RX6+	TX5+	4
5	TX5-	RX6-	6
7	TX6+	TX6-	8

Table 8: S3A: Front-Panel Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX7+	RX7-	2
3	RX8+	TX7+	4
5	TX7-	RX8-	6
7	TX8+	TX8-	8

4.3.4 Sw1: Hot-Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

4.3.5 SW2: DIP Switch

Switch SW2 can be used for customer specific FPGA functionality.

5 NAMC-xE1 Programming Notes

Table 9: FPGA Memory Map – Overview

	Logical Block	Description
0x00000..0x000ff	General Purpose Status	General Purpose Read-Only
0x00100..0x001ff	General Purpose Registers	General Purpose Read/Write
0x01000..0x01fff	FPGA SPI Flash Interface	
0x02000..0x02fff	Atmel SPI Interface	
0x10000..0x1ffff	GigabitEthernet Interface Block	
0x20000..0x2ffff	Local TDM Block	
0x80000..0xfffff	iTDM Block	

5.1 FPGA Register Description General Purpose Status Registers - 0x00..0x1ff

Table 10: FPGA Register Description General Purpose Status / Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	FPGA_TYPE								PCB_VERS							
0x02	DEV_VERS/FPGA_VERS															
0x04	TEST_VAL_1															
0x06	TEST_VAL_2															
0x08	BOARD_ID															
0x0A	Reserved												ASS_OPT			
0x0C	IRQ_STAT															
0x0E	Reserved										PLL_STAT					
0x10	CARRIER_ID								GEO_ADDRESS							
0x20	GBE_ERR_CNT															
0x22	PCS_ERR_CNT															
0x100	RST															
0x102	Reserved								AMC_LED_CTRL							
0x10C	IRQ_ENBL															
0x10E	TCKL_A_CTRL															
0x110	TCKL_B_CTRL															
0x112	TCKL_C_CTRL															
0x114	TCKL_D_CTRL															
0x116	ZPLL_REF0_SEL															
0x118	ZPLL_REF1_SEL															
0x11A	tbd															
0x11C	Reserved															
0x11E	Reserved															
0x120	PLL_CTRL															
0x122	TDM_LB_EN															

5.1.1 FPGA Register Description – FPGA_TYPE/PCB_VERS – 0x00

Bit	Name	Description	Default	Access
15..8		FPGA_TYPE	0x00	Read Only
7..4	PCB_MAJ_VERS	PCB Major Version (**x**.y) 4 bit unsigned number	HW init	Read Only
3..0	PCB_MIN_VER	PCB Minor Version (x.**y**) 4 bit unsigned number	HW init	Read Only

Note: The PCB Version is determined by the level of unused pins hardcoded on the PCB.

5.1.2 FPGA Register Description – FPGA_VERS – 0x02

Bit	Name	Description	Default	Access
15..8	FPGA_SUB_VERS	FPGA Sub Version (x.y.**z**); 8 bit unsigned number	n/a	Read Only
7..4	FPGA_MAJ_VERS	FPGA Major Version (**x**.y.z) 4 bit unsigned number	n/a	Read Only
3..0	FPGA_MIN_VERS	FPGA Minor Version (x.**y**.z) 4 bit unsigned number	n/a	Read Only

5.1.3 FPGA Register Description – TEST_VAL_1 – 0x04

Bit	Name	Description	Default	Access
15..0	TEST_1	Random number for testing purposes	0xAA55	Read Only

5.1.4 FPGA Register Description – TEST_VAL_2 – 0x06

Bit	Name	Description	Default	Access
15..0	TEST_2	Random number for testing purposes	0xDEAD	Read Only

5.1.5 FPGA Register Description – BOARD_ID – 0x08

Bit	Name	Description	Default	Access
15..0	BOARD_ID	Holds internal Board-ID	0x0Bb10	Read Only

5.1.6 FPGA Register Description – ASS_OPT – 0x0A

Bit	Name	Description	Default	Access
15..4		Reserved	0x00	Read Only
3	ASS_OPT_SRAM2	SRAM2 present	0	Read Only
2	ASS_OPT_SRAM1	SRAM1 present	0	Read Only
1..0	ASS_OPT_E1	Number of E1-Interfaces: 00: 1x E1 01: 2x E1 10: 4x E1 11: 8x E1	11	Read Only

5.1.7 FPGA Register Description – IRQ_STAT – 0x0C

Bit	Name	Description	Default	Access
15..0	IRQ_STAT	IRQ_Status	0x0000	Read Only

5.1.8 FPGA Register Description – PLL_STAT – 0x0E

Bit	Name	Description	Default	Access
15..10	Reserved	Reserved	n/a	Read Only
9	Tbd	pcie_dl_up	n/a	Ready Only
8	Tbd	mr_an_complete	n/a	Read Only
7..5	Reserved	Reserved	n/a	Read Only
4	LOCK	PLL locked	n/a	Read Only
3	HLD_OV	PLL in Hold_Over_Mode	n/a	Read Only
1..2	REF_FAIL	PLL reference failed	n/a	Read Only
0	REF_SEL_SIG	Selected reference signal	n/a	Read Only

5.1.9 FPGA Register Description – CARRIER_ID / GEO_ADDRESS – 0x10

Bit	Name	Description	Default	Access
15..8	CARRIER_ID	Carrier Manager ID 0x80 + 2*Carrier Number	na	Read Only
7..0	GEO_ADDRESS	Geographical Address (Slot ID) 0x72: AMC1 0x74: AMC2 0x76: AMC3 0x78: AMC4 0x7A: AMC5 0x7C: AMC6 0x7E: AMC7 0x80: AMC8 0x82: AMC9 0x84: AMC10 0x86: AMC11 0x88: AMC12	na	Read Only

5.1.10FPGA Register Description – GbE_ERR_CNT – 0x20

Bit	Name	Description	Default	Access
15..0	GBE_ERR_CNT	GbE Error Counter	0x0000	Read Only

5.1.11FPGA Register Description – PCS_ERR_CNT – 0x22

Bit	Name	Description	Default	Access
15..0	PCS_ERR_CNT	PCS Error Counter	0x0000	Read Only

5.1.12FPGA Register Description – RST – 0x100

Writing "1" to a bit of this register causes a reset pulse on the respective device. All bits are self-clearing.

Bit	Name	Description	Default	Access
15	BOARD_RST	Complete System reset	0x0	Read/Write
7..14		Reserved	0x0	Read/Write
6	IPMI_RST	IPMI reset	0x0	Read/Write
5		Reserved	0x0	Read/Write
4	SPI_RST	SPI controller to FPGA configuration EEPROM reset	0x0	Read/Write
3	LOC_TDM_RST	Local TDM logic reset	0x0	Read/Write
2	GBE_RST	Gigabit Ethernet logic reset	0x0	Read/Write
1	ITDM_RST	IDTM reset	0x0	Read/Write
0	LOC_RST	Local bus devices reset	0x0	Read/Write

5.1.13FPGA Register Description – AMC_LED_CTRL – 0x102

Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read/Write
7..4	ORNG	AMC_LED control orange	0x0	Read/Write
3..0	GRN	AMC_LED control green	0x7	Read/Write

5.1.14FPGA Register Description – IRQ_ENBL – 0x10C

Bit	Name	Description	Default	Access
15..0	IRQ_ENBL	IRQ_Enable	0x0000	Read/Write

5.1.15FPGA Register Description – TCKL_A_CTRL – 0x10E

Bit	Name	Description	Default	Access
15..0	TCKL_A	TCKLA control	0x0000	Read/Write

5.1.16FPGA Register Description – TCKL_B_CTRL – 0x110

Bit	Name	Description	Default	Access
15..0	TCKL_B	TCKLB control	0x0000	Read/Write

5.1.17FPGA Register Description – TCKL_C_CTRL – 0x112

Bit	Name	Description	Default	Access
15..0	TCKL_C	TCKLC control	0x0000	Read/Write

5.1.18FPGA Register Description – TCKL_D_CTRL – 0x114

Bit	Name	Description	Default	Access
15..0	TCKL_D	TCKLD control	0x0000	Read/Write

5.1.19FPGA Register Description – ZPLL_REF0_SEL – 0x116

Bit	Name	Description	Default	Access
15..0	ZPLL_REF0_SEL	Selects which signal is driven to ZPLL_REF0	0x0011	Read/Write

5.1.20FPGA Register Description – ZPLL_REF1_SEL – 0x118

Bit	Name	Description	Default	Access
15..0	ZPLL_REF1_SEL	Selects which signal is driven to ZPLL_REF1	0x0000	Read/Write

5.1.21FPGA Register Description – tbd – 0x11A

Bit	Name	Description	Default	Access
15..0		tbd	0x0000	Read/Write

5.1.22FPGA Register Description – Reserved – 0x11C

Bit	Name	Description	Default	Access
15..0		Reserved	0x00b7	Read/Write

5.1.23FPGA Register Description – Reserved – 0x11E

Bit	Name	Description	Default	Access
15..0		Reserved	0x0000	Read/Write

5.1.24FPGA Register Description – PLL_CTRL – 0x120

Bit	Name	Description	Default	Access
15..0	PLL_CTRL	PLL control	0x0000	Read/Write

5.1.25FPGA Register Description – TDM_LB_EN – 0x122

Bit	Name	Description	Default	Access
18..4	Reserved	Reserved	0x000	Read/Write
3..0	TDM_LB_EN	TDM_LB_EN	0	Read/Write

6 Board Specification

Table 11: NAMC-xE1 Features - Overview

FPGA	Lattice ECP3 FPGA (LFE3-70)
AMC-Module	Standard Advanced Mezzanine Card, single width
Front-I/O	4x RJ45 Ethernet
Firmware	OK1, Linux (on request)
Power Consumption	12V / 1.0A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG AMC.2 Rev. 1.0 (Type E2) PCI Express Base Specification Rev. 1.1 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0 ITU-T G.703 (for E1/T1 Standard) ITU-T G.823 (Jitter Attenuation)

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAMC-xE1** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-xE1** read this installation section
- Before installing or uninstalling the **NAMC-xE1**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-xE1** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-xE1** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires only:

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-xE1**
- power supply
- cooling devices

7.2.2 Power supply

The power supply for the **NAMC-xE1** must meet the following specifications:

- required for the module: +12V / 1.0A max.

7.2.3 Automatic Power Up

In the following situations the **NAMC-xE1** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset
  - when +12V voltage level drops below 10V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on

"Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Maxim, DS26518 Data Sheet, Rev. 103008
[2] Atmel, AT24C128/256 Data Sheet, Rev. 0670J-SEEPR-4/1/03
[3] Atmel, Atmega16/16L Product Data, Rev. 2466C-03/02
[4] Lattice, ECP3 Handbook, Version 1.7
[5] N.A.T.: Ethernet Control Interface Technical Reference Manual, Ver. 1.1, 08/2008
[6] N.A.T., iTDM-FPGA Technical Reference Manual, 03/2009, Ver. 1.3

Appendix B: Document's History

Revision	Date	Description	Author
1.0	01.10.2010	initial revision	te
1.1	14.05.2013	Address, phone and fax updated	Fh
1.2	19.06.2013	Reworked, updated to new layout, typo correction	se
1.3	18.02.2014	Added chapter 5 – Register Description	se
	24.06.2014	Updated Location and Connector Diagram Update chapter 7.3 RoHS-Directive / REACH	se
	24.06.2021	Updated chapter 5 – Register Description minor changes (typos etc.)	se