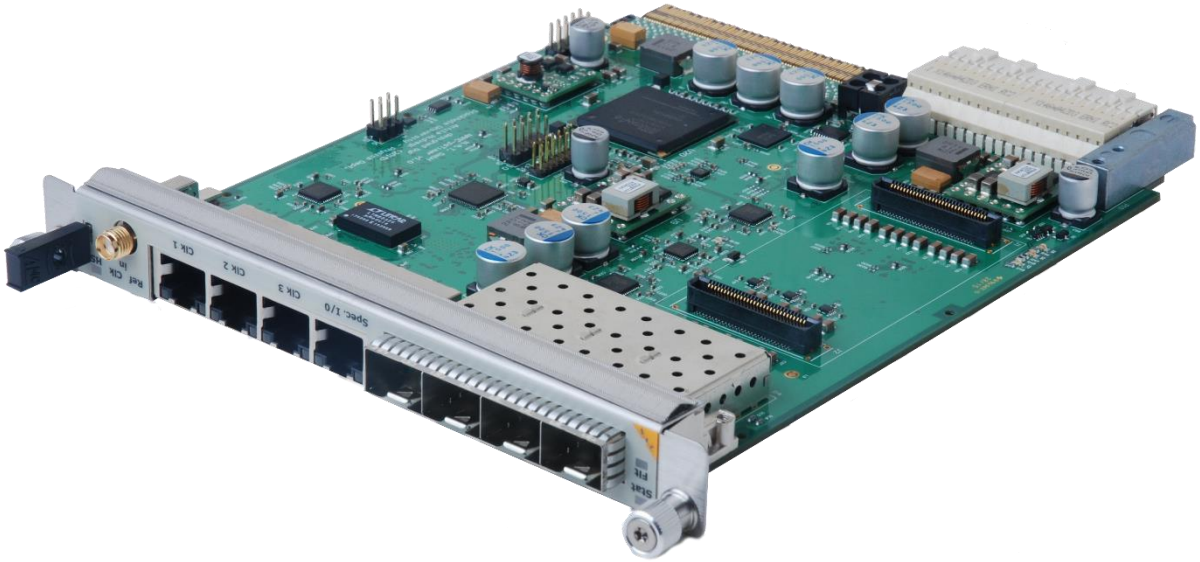
NAMC-PSTIMER

PICOSECOND TIMING MODULE

DESIGNED BY DESY HAMBURG / UNIVERSITY OF STOCKHOLM

OPTIMIZED AND MANUFACTURED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.1

HW REVISION 1.X

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1. PREFACE

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1.2. About This Document

This document is intended to give an overview on the **NAMC-psTimer's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAMC-psTimer's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAMC-psTimer** for the first time

Functional Description

Detailed information on the individual devices and the **NAMC-psTimer's** main features

Hardware

Description of the connectors, switches, and LEDs located on the **NAMC-psTimer**

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document and standards, the **NAMC-psTimer** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAMC-psTimer** is handled by qualified personnel only!

2. INTRODUCTION

The **NAMC-psTimer** is an AMC based Fast Timing System with a pico-second stable clock in double width, mid-size AMC format for usage in the MicroTCA.4 architecture. Its main purpose is to output triggers and clock signals, which may be based on local stand-alone configuration, or information provided by a global timing system installation.

The number of output triggers and clock signals can be extended by adding an RTM, e.g. the **NAMC-psTimer-RTM-C** (copper). Triggers, clocks, and data coming from the Zone3 connector of the **NAMC-psTimer** are routed to 9 Lemo connectors at the face plate; three of nine channels offer a 5ps resolution.

2.1. Basic Functionality

The **NAMC-psTimer** system is designed for large timing systems installations, such as the European XFEL (X-Ray Free Electron Laser) in Hamburg, Germany – please refer to chapter 6.1 Internal Reference Documentation for details – but it can be used in a single stand-alone setup as well.

The module can work in transmitter, receiver, and gateway mode. Moreover, it adapts to different timer requirements of master clocks and configurations. Clocks and triggers are programmed and generated by a master module and distributed in a multi-star topology. All triggers within the entire timing system are synchronized with a jitter of approximately 10ps.

In addition to the distribution of triggers and clocks, the system is able to distribute data words and tables through its fiber distribution network. A precision 1.3GHz clock with modulated data is used on the fiber links. Receivers can recover both clock and data. Synchronized dividers are used to generate local clocks at the receivers.

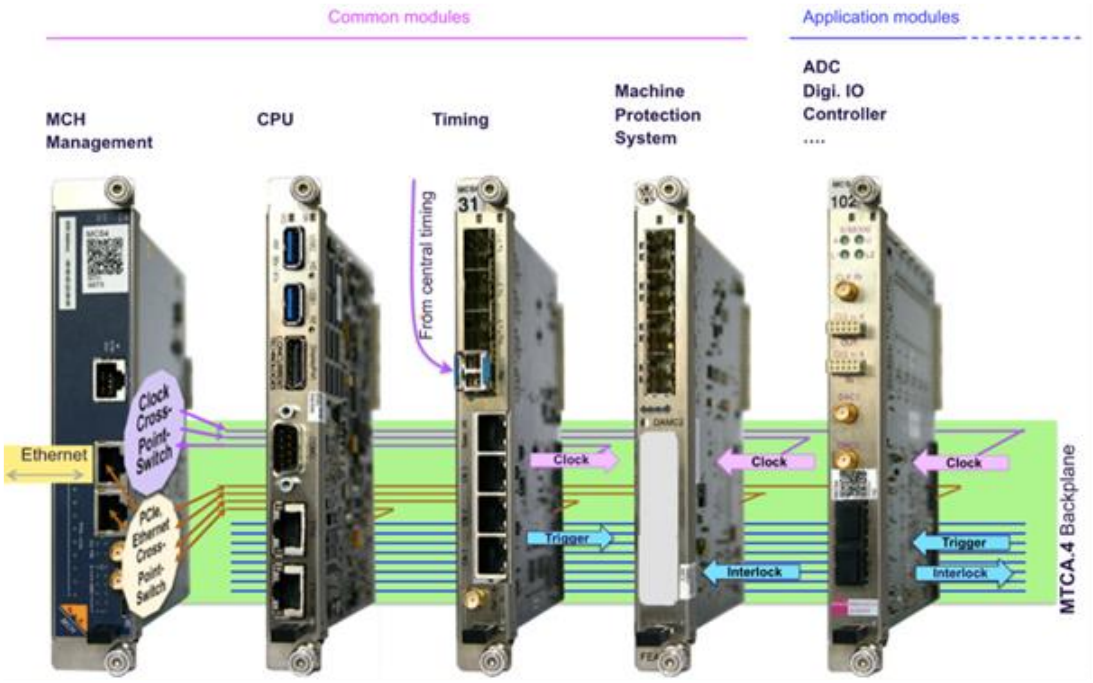
The receiver has 23 programmable outputs:

- Trigger with delay
- Immediate or delayed trigger events
- Gates between trigger events
- Slow clocks
- Two different slow data protocols
- Fast data protocol

2.2. Applications

As mentioned above, a typical application is the operation at the XFEL facility. A usual setup is shown below.

Figure 1 – Typical Setup NAMC-psTimer



Note: The former name of **NAMC-psTimer** was **x2Timer**. The name was changed to reflect the picosecond resolution in the product name as well as the new manufacturer N.A.T., who optimized the design for better productivity and signal quality.

2.3. Main Features

Table 1 – Technical Data

Form Factor	
	• Double-width, mid-size AMC with RTM-option
Processing Resources	
FPGA	• Xilinx Spartan-6
Crosspoint Switch	• Analog Devices ADN4600
Backplane	
	• TCLKA/B • 8x MLVDS • PCIe
RTM Interconnect	
	• Timing Stream OUT • Reference Clock OUT • Timing Stream IN • 10x LVDS • User Clock IN/OUT
Front Panel	
	• 4x RJ45 (CLK1-3, Special I/O) • 2x + 2x SFP (with additional mezzanine card) • 1x SMA (Ref CLK IN) • Standard MTCA LEDs
Compliance	
	• PICMG µTCA.0 Rev. 1.0 • PICMG µTCA.4 Rev. 1.0 • PICMG AMC.0 Rev. 2.0 • PICMG AMC.2 Rev. 2.0 (Type E2) • IPMI Specification V2.0 Rev. 1.0
Firmware	
	• DESY Timing Image
Order Codes	
NAMC-psTimer	• double mid-size AMC with one trigger input and one trigger output
NAMC-psTimer-P1	• mezzanine submodule for **NAMC-psTimer**, increasing number of trigger inputs and outputs to a total of four
Environmental	
Operating Environment	• Default: 0°C to +55 °C (with forced cooling) • Humidity: 10% to 90% (non-condensing)
Storage Environment	• Default: -40°C to +85°C • Humidity: 10% to 90% (non-condensing)

3. QUICK START

To ensure proper functioning of the **NAMC-psTimer** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the connectors to ensure proper contact when connecting the **NAMC-psTimer** to its associated AMC and the backplane connector to the RF-Backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAMC-psTimer** is designed to meet the requirements of µTCA systems but can be plugged onto any ATCA carrier board supporting AMC standards as well. So, the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAMC-psTimer**, a power supply, and cooling devices.

Before installing or uninstalling the **NAMC-psTimer**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-swap-capable, if you do not switch off the power.

Ensure that the **NAMC-psTimer** is connected to the carrier board or to the µTCA backplane with the connectors completely inserted. If an optional RTM module is used, these connections must be checked as well.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAMC-psTimer** must meet the following specifications:

+12V / 2.5A max.

3.3.2. Hot-Swap

The **NAMC-psTimer** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAMC-psTimer** or the system it is plugged into from damage!

Insertion of a hot-swap-capable Module

- Ensure the module and the AMC / MTCA-System it shall be connected to support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAMC-psTimer** carefully into the dedicated connector(s), until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the AMC detects the board
- If the information provided by the **NAMC-psTimer** is valid, payload power is enabled and the blue HS-LED turns off

Extraction of a hot-swap-capable Module

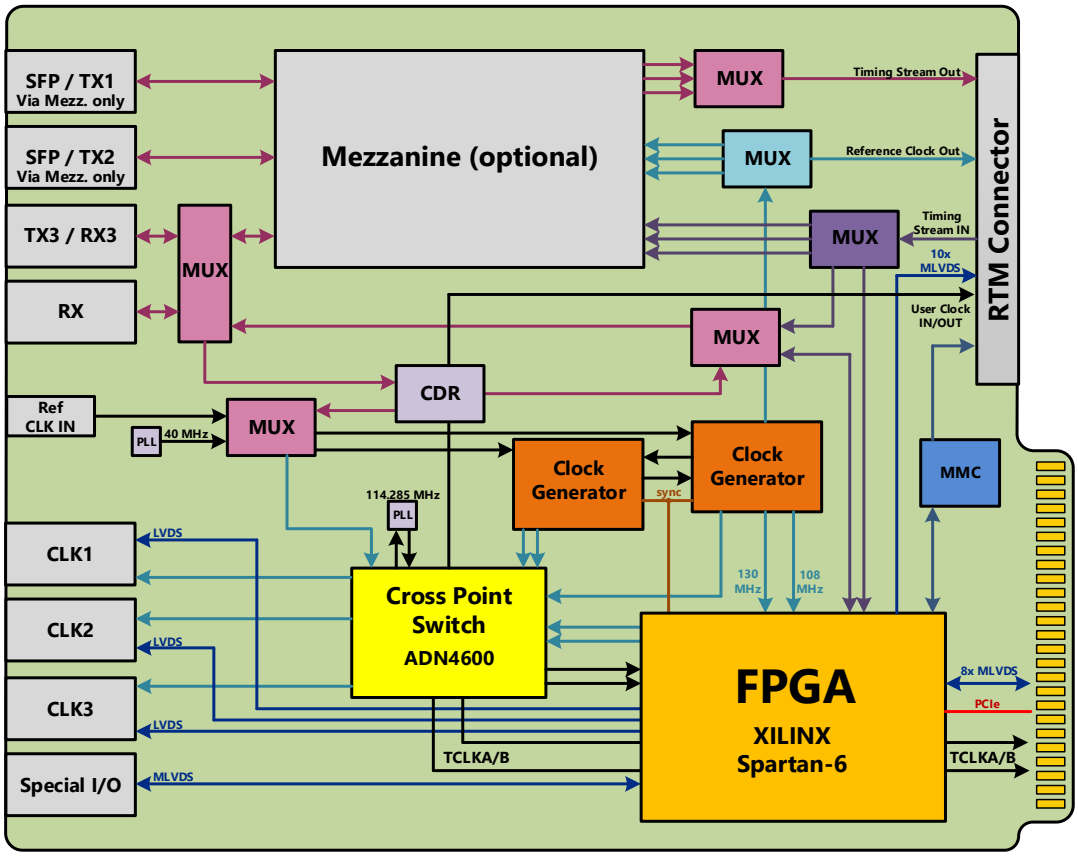
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- Payload power is disabled
- The HS-LED turns solid on
- Pull the **NAMC-psTimer** carefully out of the system

4. FUNCTIONAL DESCRIPTION

The **NAMC-psTimer** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 2 – Block Diagram



4.1. FPGA

The **NAMC-psTimer** is equipped with a XILINX Spartan-6-FPGA, which features an ideal balance between power consumption and performance. The board is controlled and managed via the PCIe-Interface of the FPGA.

4.2. Front Panel Interfaces

The **NAMC-psTimer** offers several interfaces towards the front panel. This section describes the functionality, whereas the connector- and pin assignments are detailed in chapter 5.2 Component-, Connector-, and Switch-Location.

4.2.1. Reference Clock IN

The main clock signal (also called 'base frequency'), to which all on-board generated clocks and triggers are phase-stable, may be provided optically from another **NAMC-psTimer**, electrically via a front SMA connector, or generated locally via an onboard PLL. The clock frequency must be between 500MHz and 1.4GHz.

If provided electrically by an external clock source, the input voltage must be in range 0V < VIL < 0.8V and 0.9V < VIH < 2.5V.

4.2.2. SFP Interfaces

The **NAMC-psTimer**-Baseboard offers one trigger in- and output each. The number increases to a total of four by installing the optional available transmitter mezzanine card.

SFP modules with a bandwidth of at least 1.25GBaud are supported.

Via Connector 'Rx', a 500-1.400MHz modulated timing signal from another (master)-**NAMC-psTimer** may be received or is unused in stand-alone mode.

The 'Rx/Tx3' connector is configurable either as redundant input (same functionality as 'Rx' connector), or as an output of a 500-1.400MHz modulated timing signal.

Both connectors 'Tx1' and 'Tx2' will output a 500-1.400MHz modulated timing signal if the transmitter mezzanine board is installed on the **NAMC-psTimer**.

4.2.3. RJ45 Outputs

Three RJ45-Outputs at the front panel offer two triggers and one precision clock as LVDS signals.

Each of the RJ45 connectors labelled 'Clk1', 'Clk2', and 'Clk3' contains a switchable 5V power supply line and three pairs of LVDS signals. The first output is a high precision clock line which can be configured to output any frequency that can be generated from the main clock frequency by integer division. The other two output channels can be configured to output, delivering any signal generated by the on-board-FPGA.

Currently triggers, clocks (main clock frequency/24 divided by an integer), bunch pattern (special pattern generated by a master timing system), or any of the special I/O input signals can be provided.

4.2.4. Special Input-/Output Connector

The RJ45 connector labelled 'Spec. I/O' on the AMC front panel contains 4 pairs of M-LVDS signals which are connected to the on-board FPGA. Depending on the FPGA firmware, each pair can be used as input or output independently.

With the currently available firmware, all pairs are configured as inputs. They can be used for external trigger inputs and routed directly or combined (AND, OR, Gate) with other triggers to any other trigger output on the front, backplane, or RTM.

Each pair could also be configured to temporarily inhibit the generation of any trigger output channel. The polarity of any input signal can be inverted in the configuration. An external adapter for converting single-ended TTL-signals to LVDS-signals is available

4.3. Optional Mezzanine Module

The number of interfaces of the **NAMC-psTimer** can be increased by installing an optional mezzanine module.

Currently, just one mezzanine module without drift compensation is available. Please refer to Table 1 – Technical Data for the order code.

4.4. Optional RTMs

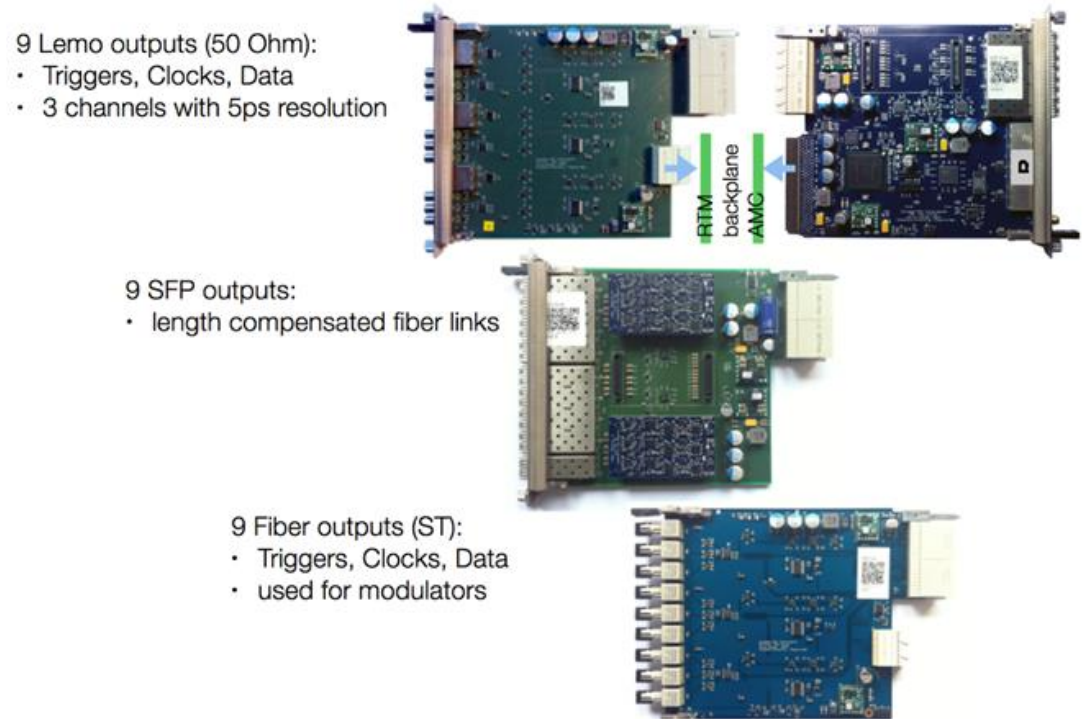
The number of output triggers and clock signals can be extended by adding one of the following Rear Transition Modules (RTMs):

NAMC-psTimer-RTM-C (copper) with 9 Lemo connectors

NAMC-psTimer-RTM-F (fiber) with 9 SFP cages

NAMC-psTimer-RTM-ST (ST connector) currently only available from Desy

Figure 3 – Optional RTMs for NAMC-psTimer

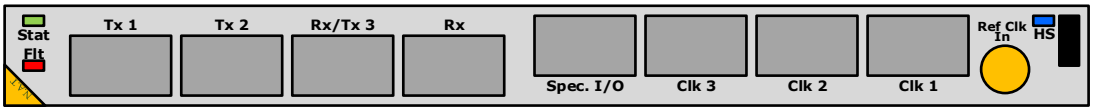


For more information, please refer to chapter 6.1 Internal Reference Documentation.

5. HARDWARE

5.1. Face Plate and LEDs

Figure 4 – Face Plate



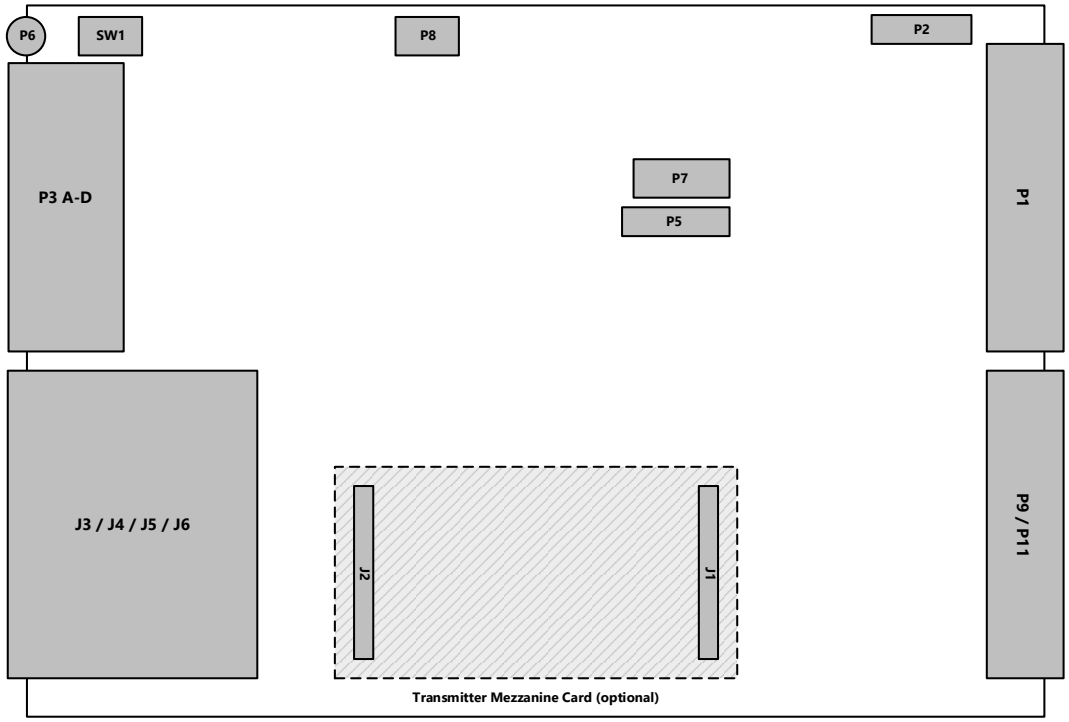
The **NAMC-psTimer-RTM** features the standard AMC IPMI LEDs with the blue one indicating the hot-swap-status.

The red Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the General Purpose LED (Stat) physically consists of two LEDs (green and orange) sharing the same hole in the face plate.

5.2. Component-, Connector-, and Switch-Location

Figure 5 – Location Diagram



Please refer to the following tables to look up the connector pin assignment of the **NAMC-psTimer**.

5.2.2. J1/J2: Mezzanine Module Connector

Connector J1 and J2 connect to an optional available transmitter mezzanine card.

Table 2 – J1: Mezzanine Module Connector 1 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	2
3	VCC3V3	Ch3_Ref_Clk_IN_P	4
5	VCC2V5	Ch3_Ref_Clk_IN_N	6
7	GND	GND	8
9	VCC3V3	Ch3_Rx_OUT_P	10
11	VCC2V5	Ch3_Rx_OUT_N	12
13	GND	GND	14
15	VCC3V3	Ch3_Tx_IN_P	16
17	VCC2V5	Ch3_Tx_IN_N	18
19	VCC2V5	GND	20
21	GND	GND	22
23	VCC3V3	Ch2_Ref_Clk_IN_P	24
25	VCC2V5	Ch2_Ref_Clk_IN_N	26
27	GND	GND	28
29	VCC3V3	Ch2_Rx_OUT_P	30
31	VCC2V5	Ch2_Rx_OUT_N	32
33	GND	GND	34
35	VCC3V3	Ch2_Tx_IN_P	36
37	VCC2V5	Ch2_Tx_IN_N	38
39	VCC2V5	GND	40
41	GND	GND	42
43	VCC3V3	Ch1_Ref_Clk_IN_P	44
45	VCC2V5	Ch1_Ref_Clk_IN_N	46
47	GND	GND	48
49	VCC3V3	Ch1_Rx_OUT_P	50
51	VCC2V5	Ch1_Rx_OUT_N	52
53	GND	GND	54
55	VCC3V3	Ch1_Tx_IN_P	56
57	VCC2V5	Ch1_Tx_IN_N	58
59	VCC2V5	GND	60

Table 3 – J2: Mezzanine Module Connector 2 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	2
3	CH3_Rx_IN_P	Ch3_IIC_SDA	4
5	CH3_Rx_IN_N	Ch3_IIC_SCL	6
7	GND	Ch3_INTERRUPT	8
9	CH3_Tx_OUT_P	Ch3_PDI_DATA	10
11	CH3_Tx_OUT_N	Ch3_PDI_CLK	12
13	GND	GND	14
15	VCC3V3	VCC3V3	16
17	VCC2V5	VCC2V5	18
19	GND	GND	20
21	GND	GND	22
23	CH2_Rx_IN_P	Ch2_IIC_SDA	24
25	CH2_Rx_IN_N	Ch2_IIC_SCL	26
27	GND	Ch2_INTERRUPT	28
29	CH2_Tx_OUT_P	Ch2_PDI_DATA	30
31	CH2_Tx_OUT_N	Ch2_PDI_CLK	32
33	GND	GND	34
35	VCC3V3	VCC3V3	36
37	VCC2V5	VCC2V5	38
39	GND	GND	40
41	GND	GND	42
43	CH1_Rx_IN_P	Ch1_IIC_SDA	44
45	CH1_Rx_IN_N	Ch1_IIC_SCL	46
47	GND	Ch1_INTERRUPT	48
49	CH1_Tx_OUT_P	Ch1_PDI_DATA	50
51	CH1_Tx_OUT_N	Ch1_PDI_CLK	52
53	GND	GND	54
55	VCC3V3	VCC3V3	56
57	VCC2V5	VCC2V5	58
59	GND	GND	60

5.2.3. J3/J4/J5/J6: SFP Connectors

Connectors J3-J6 serve as trigger interfaces. Please note, that J3 and J4 are only available with an optional mezzanine card.

Table 4 – J3: SFP Connector 1 (with mezzanine only) – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	SFP1_TxFault	2
3	SFP1_TxDisable	SFP1_IIC_SDA	4
5	SFP1_IIC_SCL	SFP1_MOD_DETECTn	6
7	SFP1_RateSel0	SFP1_LOS	8
9	SFP1_RateSel1	GND	10
11	GND	Ch1_Rx_IN_N	12
13	Ch1_Rx_IN_P	GND	14
15	VCCR	VCCT	16
17	GND	Ch1_Tx_OUT_P	18
19	Ch1_Tx_OUT_N	GND	20

Table 5 – J4: SFP Connector 2 (with mezzanine only) – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	SFP2_TxFault	2
3	SFP2_TxDisable	SFP2_IIC_SDA	4
5	SFP2_IIC_SCL	SFP2_MOD_DETECTn	6
7	SFP2_RateSel0	SFP2_LOS	8
9	SFP2_RateSel1	GND	10
11	GND	Ch2_Rx_IN_N	12
13	Ch2_Rx_IN_P	GND	14
15	VCCR	VCCT	16
17	GND	Ch2_Tx_OUT_P	18
19	Ch2_Tx_OUT_N	GND	20

Table 6 – J5: SFP Connector 3 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	SFP3_TxFault	2
3	SFP3_TxDisable	SFP3_IIC_SDA	4
5	SFP3_IIC_SCL	SFP3_MOD_DETECTn	6
7	SFP3_RateSel0	SFP3_LOS	8
9	SFP3_RateSel1	GND	10
11	GND	SFP3_Rx_N	12
13	SFP3_Rx_P	GND	14
15	VCCR	VCCT	16
17	GND	SFP3_Tx_P	18
19	SFP3_Tx_N	GND	20

Table 7 – J6: SFP Connector 4 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	SFP4_TxFault	2
3	SFP4_TxDisable	SFP4_IIC_SDA	4
5	SFP4_IIC_SCL	SFP4_MOD_DETECTn	6
7	SFP4_RateSel0	SFP4_LOS	8
9	SFP4_RateSel1	GND	10
11	GND	SFP4_Rx_N	12
13	SFP4_Rx_P	GND	14
15	VCCR	VCCT	16
17	GND	SFP4_Tx_P	18
19	SFP4_Tx_N	GND	20

5.2.4. P1: AMC Connector

P1 connects the **NAMC-psTimer** to the MTCA-Backplane.

Figure 6 – P1: AMC Connector

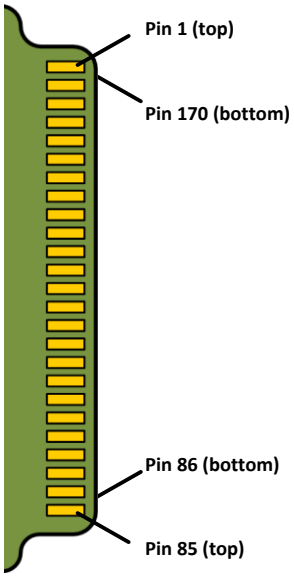


Table 8 – P1: AMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	MP_12V	TDI_EDGE	169
3	PS1_n	TDO_EDGE	168
4	MP_3V3	TRST#	167
5	GA0	TMS_EDGE	166
6	nc	TCK_EDGE	165
7	GND	GND	164
8	nc	AMC_MLVDS_7_P	163
9	MP_12V	AMC_MLVDS_7_N	162
10	GND	GND	161
11	GbE_Tx_P	AMC_MLVDS_6_P	160
12	GbE_Tx_N	AMC_MLVDS_6_N	159
13	GND	GND	158
14	nc	AMC_MLVDS_5_P	157
15	nc	AMC_MLVDS_5_N	156
16	GND	GND	155
17	GA1	AMC_MLVDS_4_P	154
18	MP_12V	AMC_MLVDS_4_N	153
19	GND	GND	152
20	nc	AMC_MLVDS_3_P	151
21	nc	AMC_MLVDS_3_N	150
22	GND	GND	149
23	RX1+	AMC_MLVDS_2_P	148
24	RX1-	AMC_MLVDS_2_N	147
25	GND	GND	146
26	GA2	AMC_MLVDS_1_P	145
27	MP_12V	AMC_MLVDS_1_N	144
28	GND	GND	143
29	nc	AMC_MLVDS_0_P	142
30	nc	AMC_MLVDS_0_N	141
31	GND	GND	140
32	RX2+	nc	139
33	RX2-	nc	138
34	GND	GND	137
35	nc	RX16+	136
36	nc	RX16-	135
37	GND	GND	134
38	RX3+	nc	133
39	RX3-	nc	132
40	GND	GND	131
41	ENABLE_n	RX15+	130
42	MP_12V	RX15-	129
43	GND	GND	128
44	PCIe_Tx_P	nc	127
45	PCIe_Tx_N	nc	126
46	GND	GND	125
47	nc	RX14+	124

Pin #	Signal	Signal	Pin #
48	nc	Rx14-	123
49	GND	GND	122
50	nc	AMC_GTP1_Tx_P	121
51	nc	AMC_GTP1_Tx_N	120
52	GND	GND	119
53	RX5+	nc	118
54	RX5-	nc	117
55	GND	GND	116
56	SCL_L	AMC_GTP0_Tx_P	115
57	MP_12V	AMC_GTP0_Tx_N	114
58	GND	GND	113
59	nc	nc	112
60	nc	nc	111
61	GND	GND	110
62	RX6+	nc	109
63	RX6-	nc	108
64	GND	GND	107
65	nc	RX11+	106
66	nc	RX11-	105
67	GND	GND	104
68	RX7+	nc	103
69	RX7-	nc	102
70	GND	GND	101
71	SDA_L	RX10+	100
72	MP_12V	RX10-	99
73	GND	GND	98
74	AMC_CLK1_P	nc	97
75	AMC_CLK1_N	nc	96
76	GND	GND	95
77	AMC_CLK2_P	RX9+	94
78	AMC_CLK2_N	Rx9-	93
79	GND	GND	92
80	PCIe_Ref_CLK0_P	nc	91
81	PCIe_Ref_CLK0_N	nc	90
82	GND	GND	89
83	PS0_n	RX8+	88
84	MP_12V	RX8-	87
85	GND	GND	86

5.2.5. P2: Lab Power Supply

Pin Header P2 offers the option to operate the **NAMC-psTimer** outside a chassis in stand-alone-mode.

Table 9 – P2: Lab Power Supply

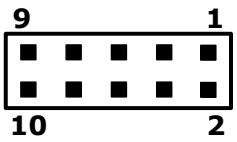


Table 10 – P2: Lab Power Supply – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MP_12V	GND	2
3	MP_12V	GND	4
5	MP_12V	GND	6
7	MP_12V	GND	8
9	ENABLE_n	GND	10

5.2.6. P3 A-D: RJ45-Connectors

P3 A-C serve as trigger outputs, whereas P3 D is a special input/output, configurable via FPGA firmware.

Figure 7 – P3 A-D: RJ45-Connectors

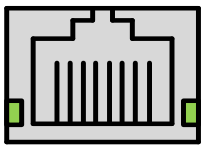


Table 11 – P3A: Trigger Output CLK1 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RJ45_1_D0_P	RJ45_1_D0_N	2
3	VCC5V_1	RJ45_1_D1_P	4
5	RJ45_1_D1_N	GND	6
7	RJ45_1_D2_P	RJ45_1_D2_N	8
9	RJ45_1_LED_1a	RJ45_1_LED_1b	10
11	RJ45_1_LED_2a	RJ45_1_LED_2b	12

Table 12 – P3B: Trigger Output CLK2 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RJ45_2_D0_P	RJ45_2_D0_N	2
3	VCC5V_2	RJ45_2_D1_P	4
5	RJ45_2_D1_N	GND	6
7	RJ45_2_D2_P	RJ45_2_D2_N	8
9	RJ45_2_LED_1a	RJ45_2_LED_1b	10
11	RJ45_2_LED_2a	RJ45_2_LED_2b	12

Table 13 – P3C: Trigger Output CLK3 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RJ45_3_D0_P	RJ45_3_D0_N	2
3	VCC5V_2	RJ45_3_D1_P	4
5	RJ45_3_D1_N	GND	6
7	RJ45_3_D2_P	RJ45_3_D2_N	8
9	RJ45_3_LED_1a	RJ45_3_LED_1b	10
11	RJ45_3_LED_2a	RJ45_3_LED_2b	12

Table 14 – P3D: Special I/O – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RJ45_4_D0_P	RJ45_4_D0_N	2
3	RJ45_4_D3_P	RJ45_4_D1_P	4
5	RJ45_4_D1_N	RJ45_4_D3_N	6
7	RJ45_4_D2_P	RJ45_4_D2_N	8
9	RJ45_4_LED_1a	RJ45_4_LED_1b	10
11	RJ45_4_LED_2a	RJ45_4_LED_2b	12

5.2.7. P5: FPGA JTAG Header

Pin Header P5 offers a standard XILINX programming interface to access the Spartan-FPGA via JTAG.

Table 15 – P5: FPGA JTAG Header

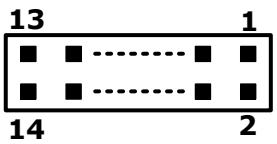


Table 16 – P5: FPGA JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	VCC3V3	2
3	GND	TMS	4
5	GND	TCK	6
7	GND	TDO	8
9	GND	TDI	10
11	GND	nc	12
13	GND	nc	14

5.2.8. P6: Reference Clock Input

SMA Connector P6 features a reference clock input.

Table 17 – P6: Reference Clock Input – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	VCC3V3	2

5.2.9. P7: Microcontroller JTAG Header

Pin Header P7 connects to the JTAG-programming-port of the Atmel µC device.

Table 18 – P7: Microcontroller JTAG Header

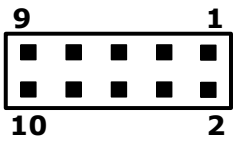


Table 19 – P7: Microcontroller JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MMC_TCK	GND	2
3	MMC_TDO	MP_3V3	4
5	MMC_TMS	MMC_RST_n	6
7	MP_3V3	nc	8
9	MMC_TDI	GND	10

5.2.10. P8: Microcontroller BDM Header

Pin Header P8 connects to the BDM-programming-port of the Atmel µC device.

Table 20 – P8: Microcontroller BDM Header

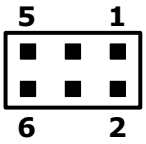


Table 21 – P8: Microcontroller BDM Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MMC_PDI_DATA	MP_3V3	2
3	nc	nc	4
5	MMC_RST_n	GND	6

5.2.11. P9 / P11: RTM-Connectors (Zone3)

RTM-Connectors P9 and P11 interface to an optional RTM.

Figure 8 – P9 / P11: RTM-Connectors

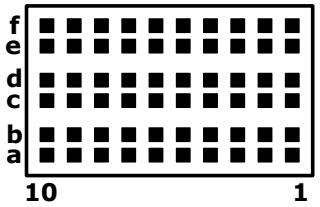


Table 22 – P9: RTM-Connector – Pin Assignment

	A	B	AB	C	D	CD	E	F	EF
1	RTM_ChX_INTERRUPT1	nc	GND	RTM_ChX_IIC_SDA1	RTM_ChX_IIC_SCL1	GND	RTM_SFP_IIC_SDA1	RTM_SFP_IIC_SCL1	GND
2	RTM_ChX_INTERRUPT2	nc	GND	RTM_ChX_IIC_SDA2	RTM_ChX_IIC_SCL2	GND	RTM_SFP_IIC_SDA2	RTM_SFP_IIC_SCL2	GND
3	RTM_ChX_INTERRUPT3	nc	GND	RTM_ChX_IIC_SDA3	RTM_ChX_IIC_SCL3	GND	RTM_SFP_IIC_SDA3	RTM_SFP_IIC_SCL3	GND
4	RTM_ChX_INTERRUPT4	nc	GND	RTM_ChX_IIC_SDA4	RTM_ChX_IIC_SCL4	GND	RTM_SFP_IIC_SDA4	RTM_SFP_IIC_SCL4	GND
5	RTM_ChX_INTERRUPT5	nc	GND	RTM_ChX_IIC_SDA5	RTM_ChX_IIC_SCL5	GND	RTM_SFP_IIC_SDA5	RTM_SFP_IIC_SCL5	GND
6	RTM_ChX_INTERRUPT6	nc	GND	RTM_ChX_IIC_SDA6	RTM_ChX_IIC_SCL6	GND	RTM_SFP_IIC_SDA6	RTM_SFP_IIC_SCL6	GND
7	RTM_ChX_INTERRUPT7	nc	GND	RTM_ChX_IIC_SDA7	RTM_ChX_IIC_SCL7	GND	RTM_SFP_IIC_SDA7	RTM_SFP_IIC_SCL7	GND
8	RTM_ChX_INTERRUPT8	nc	GND	RTM_ChX_IIC_SDA8	RTM_ChX_IIC_SCL8	GND	RTM_SFP_IIC_SDA8	RTM_SFP_IIC_SCL8	GND
9	GND	GND	GND	GND	GND	GND	GND	GND	GND
10	RTM_Ref_CLK_P	RTM_Ref_CLK_N	GND	RTM_GTP_Tx_P	RTM_GTP_Tx_N	GND	RTM_GTP_Rx_P	RTM_GTP_Rx_N	GND

Table 23 – P11: RTM-Connector – Pin Assignment

	A	B	AB	C	D	CD	E	F	EF
1	RTM_12V	RTM_12V	GND	RTM_PS_n	RTM_SDA	GND	JTAG_TCK_RTM	JTAG_TDO_TRM	GND
2	RTM_12V	RTM_12V	GND	RTM_3V3	RTM_SCL	GND	JTAG_TDI_TRM	JTAG_TMS_RTM	GND
3	RTM_D1_P	RT_D1_N	GND	RTM_D2_P	RTM_D2_N	GND	RTM_Trg_P	TRM_Trg_N	GND
4	nc	nc	GND	nc	nc	GND	nc	nc	GND
5	PDI_DATA	PDI_CLK	GND	RTM_PDI_SEL0	RTM_PDI_SEL1	GND	RTM_PDI_SEL2	RTM_PDI_SEL3	GND
6	RTM_Trg_Tx_0_P	RTM_Trg_Tx_0_N	GND	RTM_Trg_Tx_1_P	RTM_Trg_Tx_1_N	GND	RTM_Trg_Tx_2_P	RTM_Trg_Tx_2_N	GND
7	RTM_Trg_Tx_3_P	RTM_Trg_Tx_3_N	GND	RTM_Trg_Tx_4_P	RTM_Trg_Tx_4_N	GND	RTM_Trg_Tx_5_P	RTM_Trg_Tx_5_N	GND
8	RTM_Trg_Tx_6_P	RTM_Trg_Tx_6_N	GND	RTM_Trg_Tx_7_P	RTM_Trg_Tx_7_N	GND	RTM_Trg_Tx_8_P	RTM_Trg_Tx_8_N	GND
9	RTM_Rx_SEL0	RTM_Rx_SEL1	GND	RTM_Rx_SEL2	RTM_Rx_SEL3	GND	nc	nc	GND
10	RTM_ChX_INTERRUPT0	nc	GND	RTM_ChX_IIC_SDA0	RTM_ChX_IIC_SCL0	GND	RTM_SFP_IIC_SDA0	RTM_SFP_IIC_SCL0	GND

5.2.12. SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

- **NAMC-psTimer-RTM-C, Technical Reference Manual:**
  https://www.nateurope.com/manuals/namc_psTimer-RTM-C_man_hw.pdf
- **XFEL**
  https://www.nateurope.com/documents/SS_High_Energy_Physics.pdf

6.2. External Reference Documentation

- Analog Devices ADN4600 Cross Point Switch, Datasheet Rev. B, 04/2015
- Atmel ATxmega128A1-AU Microcontroller, Datasheet 8067O–AVR, 06/2013
- Xilinx Spartan-6 FPGA Family Overview, DS160 V2.0, 10/2011

6.3. Standards Compliance

- PICMG µTCA.0 Rev. 1.0
- PICMG µTCA.4 Rev. 1.0
- PICMG AMC.0 Rev. 2.0
- PICMG AMC.2 Rev. 2.0 (Type E2)
- IPMI Specification V2.0 Rev. 1.0P
- ICMG µTCA.4 Rev. 1.0

6.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.6. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.7. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6.8. Abbreviation List

Table 24 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
BDM	Background Debug Mode
CDR	Clock & Data Recovery
CPU	Central Processing Unit
DESY	"Deutsches Elektronen-Synchrotron; German national research center"
EEPROM	Electrically Erasable PROM
FPGA	Field Programmable Gate Array
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
(M)LVDS	(Multipoint) Low Voltage Differential Signaling
µC	Microcontroller
µTCA/MTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
MUX	Multiplexer
PCI(e)	Peripheral Component Interconnect (Express)
(P)ROM	(Programmable) Read Only Memory
PoE	Power over Ethernet
ps	picosesond
RF	Radio Frequency
RTM	Rear Transition Module
SFP	Small Form-Factor Pluggable
SMA	SubMiniature version A Connector
TCKL	Telecom Clock
XFEL	X-Ray Free Electron Laser

7. DOCUMENT'S HISTORY

Table 25 – Document's History

Rev	Date	Description	Author
1.0	14.06.2018	• Initial Release	se
1.1	27.07.2022	• Update to new layout • Rework of whole document	se