NAMC-PTM

PRECISION TIMING MODULE

DESIGNED BY N.A.T. GMBH

TECHNICAL REFERENCE MANUAL V1.0

HW REVISION 1.X

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1. PREFACE

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAMC-PTM's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAMC-PTM's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAMC-PTM** for the first time

Functional Description

Detailed information on the individual devices and the **NAMC-PTM's** main features

Configuration

Options to adapt the **NAMC-PTM** to personal needs

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAMC-PTM** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAMC-PTM** is handled by qualified personnel only!

2. INTRODUCTION

The **NAMC-PTM** is a redundant, high-accuracy holdover clocking source. It features a Voltage Controlled Oven Compensated Crystal Oscillator (VCOCXO) as well as a Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO), several sensors for controlling/compensating tasks, and various customization options.

2.1. Basic Functionality

Main purpose of the **NAMC-PTM** is the detection of clocks or pulses from an external (GPS) or chassis-internal source (**NAT-MCH)**, rating of the quality of these signals, and offering a high-accurate clock source to the µTCA-System and/or towards the front plate.

2.2. Applications

The **NAMC-PTM** can be operated in a standard AMC-slot in nearly any µTCA-chassis.

If the customer's demands require the full payload board capacity of an µTCA-system, the **NAMC-PTM** can be operated in designated PTM-slots of a specialized and modified µTCA-chassis.

2.3. Main Features

Table 1 – Technical Data

Form Factor	
	• Single-width, full-size AMC • Width: 73.5 mm, Depth: 180.6 mm
Processing Resources	
CPU	• Atmel/Microchip SAMV71 ARM F7
Memory	• 32MB DRAM (16bit wide) • 64MB SPI NOR FLASH • MicroSD-Card socket • I^2C EEPROM
Microcontroller	• Atmel ATXmega128 as IPMI-Controller
Sensors	
Acceleration	• MEMS acceleration sensor KX126-1063
Current / Power	• 2x INA 226
Voltage	• INA3221
Temperature	• TMP100
Clock	
	• PLL AD9545
	• VCOCXO OX-171
	• VCTCXO M725
	• DAC8560
Backplane Interconnect (depending on operation mode)	
	• Regular AMC power pinout • Regular AMC IPMI pinout • Regular Backplane GbE via Port 0 / 1 ***(AMC operation mode only)*** • Backplane clock I/O via regular TCLKA-D
Front Panel	
	• BNC clock input for reception of 1PPS or 10MHz reference • BNC clock output, capable of driving 1PPS, 10MHz or 120MHz • RJ45 100/1000Base-T Ethernet to switch-internal PHY • USB based UART to SAMV71 microcontroller • 5 bicolor LED (Green and Red) • Standard AMC-LEDs
Compliance	
	• PICMG AMC.0 Rev. 2.0
Environmental	
Operating Environment	• Default: 0°C to +50 °C (with forced cooling) • Humidity: 10% to 90% at +55°C (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 2g from 36Hz to 2KH vibration compensation – especially hold-over stability – feasible via customer software) • Shocks: 20g, 11ms, 1⁄2 sine • Altitude: 0 to 5000m • Vibration compensation (especially hold-over stability) via custom software
Storage Environment	• Default: -40°C to +85°C • Humidity: 5% to 95% (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 3g from 36Hz to 2KH • Shocks: 30g, 11ms, 1⁄2 sine • Altitude: 0 to 15000m

3. QUICK START

To ensure proper functioning of the **NAMC-PTM** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the AMC-Edge-Connector to ensure proper contact when inserting the **NAMC-PTM** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAMC-PTM** can be plugged onto any ATCA carrier board supporting AMC standards and is also designed to meet the requirements of µTCA systems. So the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAMC-PTM**, a power supply, and cooling devices.

Before installing or uninstalling the **NAMC-PTM**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is Hot-Swap-capable, if you don't switch off the power.

Ensure that the **NAMC-PTM** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAMC-PTM** must meet the following specifications:

+12V / 0.8A max.

+ 3,3V / 0.05A max.

3.3.2. Hot-Swap

The **NAMC-PTM** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAMC-PTM** or the system it is plugged into from damage!

Insertion of a hot-swap-capable module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAMC-PTM** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAMC-PTM** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable module

- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAMC-PTM** carefully out of the backplane/carrier

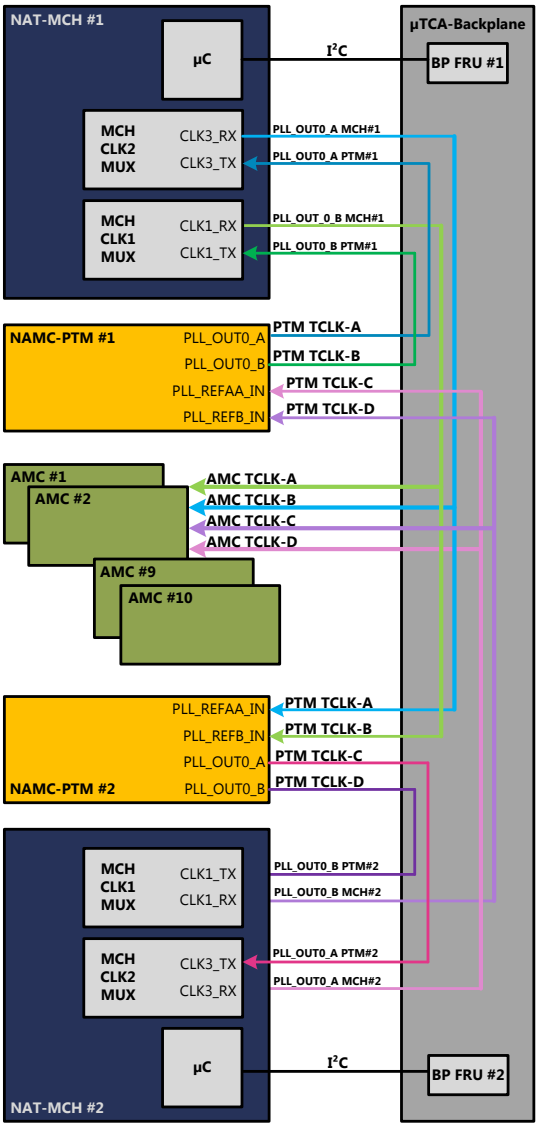
4. OPERATION MODES

4.1. Operation in a Standard AMC-Slot

As the **NAMC-PTM** complies to AMC.0, the board can be operated as a standard AMC in a standard AMC-slot in nearly any µTAC-chassis; only some minor changes in the setup of the IDT MLVDS clock MUXs on the **NAT-MCH-CLK**-module have to be taken.

The figure below gives an overview of this mode of operation.

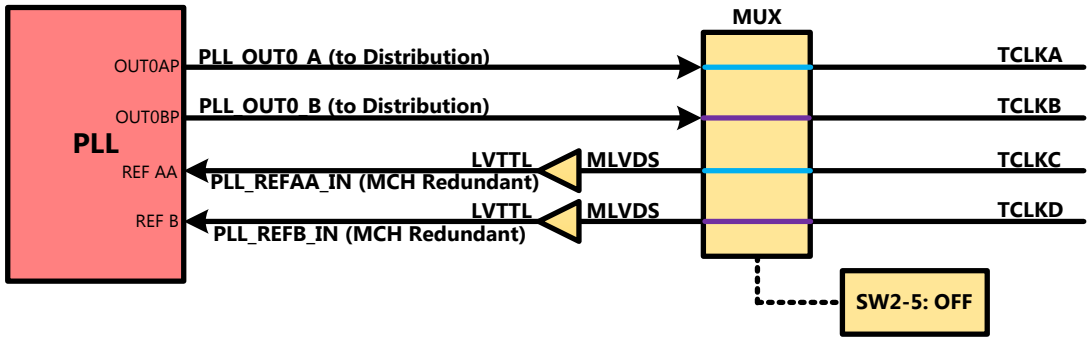
Figure 1 – Operation in AMC-Mode



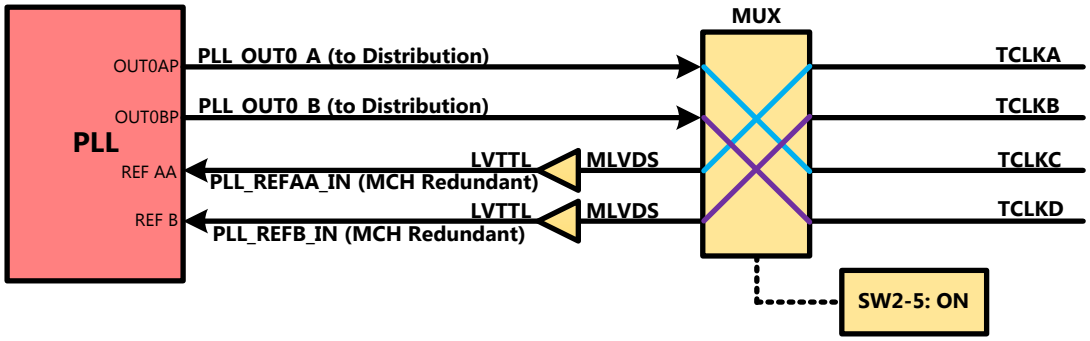
Moreover, to connect **NAMC-PTM** #1 to **NAT-MCH** #1 (TCLK A/B) and **NAMC-PTM** #2 to **NAT-MCH** #2 (TCLK C/D), adjustment of the multiplexer is mandatory. The following figure illustrates the setting via DIP-switch.

Figure 2 – MUX-Setting in AMC-Mode

NAMC-PTM #1 – connected to NAT-MCH #1



NAMC-PTM #2 – connected to NAT-MCH #2

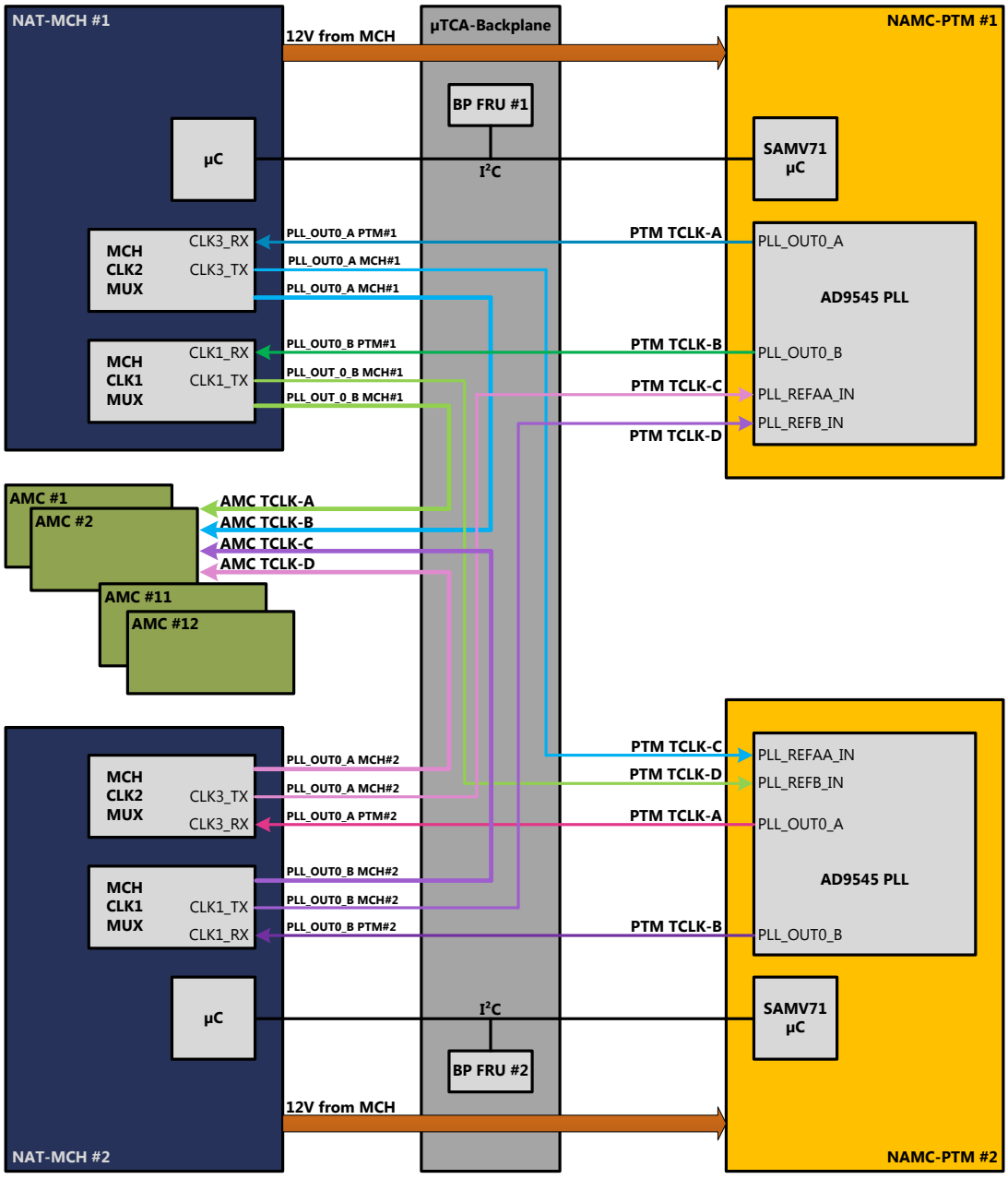


4.2. Operation in a Designated PTM-Slot

The **NAMC-PTM** is designed to be installed in a special PTM-Slot in a modified chassis. The backplane of this chassis features special hardwired connections between MCH- and PTM-modules to link **NAMC-PTM** #1 to **NAT-MCH** #1 and **NAMC-PTM** #2 to **NAT-MCH** #2.

The figure below gives an overview of this mode of operation.

Figure 3 – Operation in PTM-Mode



In this setup, further modifications on the **NAT-MCH-CLK** and setting of SW2-5 are needless.

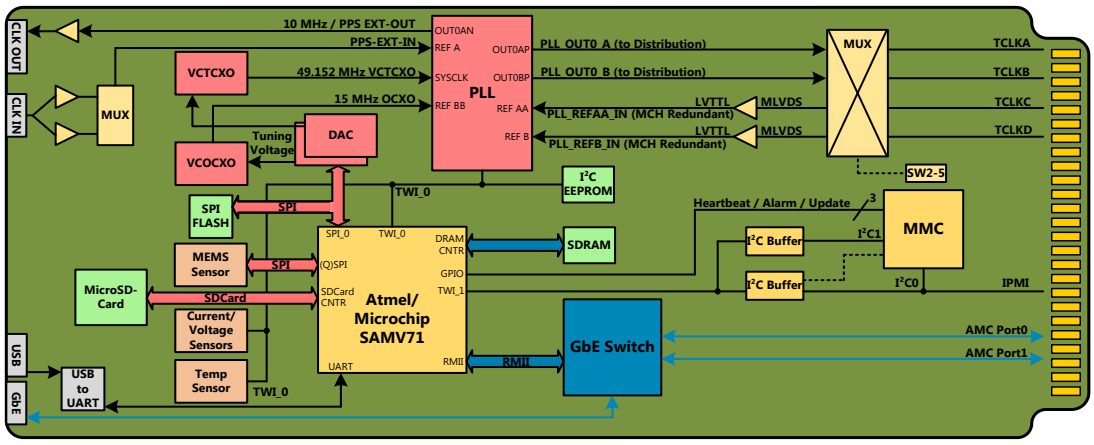
For more information on a specialized chassis, please refer to chapter 8.1 Internal Reference Documentation.

5. FUNCTIONAL DESCRIPTION

The **NAMC-PTM** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 4 – Block Diagram



5.1. Processing System

Core component is a high performance microcontroller featuring an ARM F7 CPU (Microchip SAMV71). It is extended by:

- 32MB DRAM chip (16bit wide)
- 64MB SPI NOR FLASH
- MicroSD-Card socket
- I^2C EEPROM

An ATXmega128 microcontroller is used as IPMI controller, operated via 3.3V management power.

5.2. Sensor Subsystem

Various sensor data is used to compensate frequency variations of the local oscillator caused by mechanical vibration, temperature and supply voltage changes. The sensors are:

- MEMS acceleration sensor KX126-1063
- Current/Voltage sensor INA226 / INA 3221

- Temperature sensor TMP100

The temperature and current sensors will be located as close as possible towards the OCXO. The MEMS sensor will be located as close as possible to the VCOCXO. The MEMS sensor will be placed mid underneath the oscillator.

5.3. Clock Subsystem

The clock system is capable to lock to various incoming references, generate a wide range of possible output clocks and provides and extremely accurate holdover functionality based on the compensated local oscillator.

- PLL AD9545
- Voltage Controlled Oven Compensated Crystal Oscillator (VCOCXO) OX-171, covered by plastic housing to reduce mechanical influence
- Voltage Controlled, Temperature Compensated Crystal Oscillator (VCTCXO) M725
- Digital Analog Converter (DAC) DAC8560

5.4. Communication Paths

Basically, two paths are available for PTM control/status/update communication:

- Ethernet
  - Via regular AMC GbE on Port 0 or Port 1 (only in regular AMC operation)
  - Via front panel RJ45 100(0)Base-T
- IPMI

As the IPMI path will be available both when operating the PTM in the dedicated PTM slots as well as in any regular AMC slot, this method will be implemented as basic path. N.A.T. already uses IPMI as communication method for control/status/update of the MCH clock and switch modules, so already proven software can be re-used here.

5.5. Clock I/O Circuitry and Details

The following aspects shall be realized via the circuitry and component selection concerning the front panel clock input and output connectors:

- Clock input will be used in the standard application (relevant for immunity testing), clock output is intended for debugging purpose
- Exact method of immunity testing has to be defined

- Clock input shall pass through dual signal reception circuitry, one optimized for 1pps and one for 10MHz
    - 1pps signal shall be 3.3V - 5V TTL logic levels with 50 ohms input impedance
    - 10MHz signal shall be -10 to 13 dBm sine wave but should be operational if customer hooks up 5V TTL with a 50 ohms input impedance. The output should be disconnected if input powers fall below approximately -10 dBm
    - An analog multiplexer shall select which of these signal paths is connected to PLL input
- Clock output 10MHz/1pps shall drive 3.3V TTL level into 50Ohm load

6. HARDWARE

6.1. Front Panel and LEDs

The **NAMC-PTM** module is equipped with 5 bi-coloured, user-configurable LEDs. Additionally it features the standard AMC LEDs and two green LEDs integrated in the RJ45 connector to reflect the GbE status.

Figure 5 – Front Panel

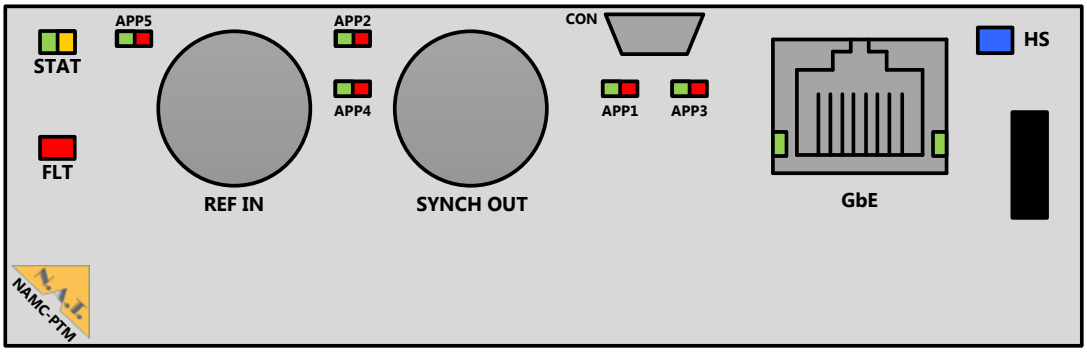


Table 2 – LED Functionality

LED	Colour	Function	Control
APP 1-5	green / red	User-configurable LEDs	SAMV71 µC
HS	blue	AMC hot-swap LED	MMC
FLT	red	Fault indication LED	MMC
STAT	green / orange	General purpose LED	MMC

The fault indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the STAT LED physically consists of two LEDs (green and orange) sharing the same hole in the front plate.

6.2. Component-, Connector-, and Switch-Location

Figure 6 – Location Diagram – Top

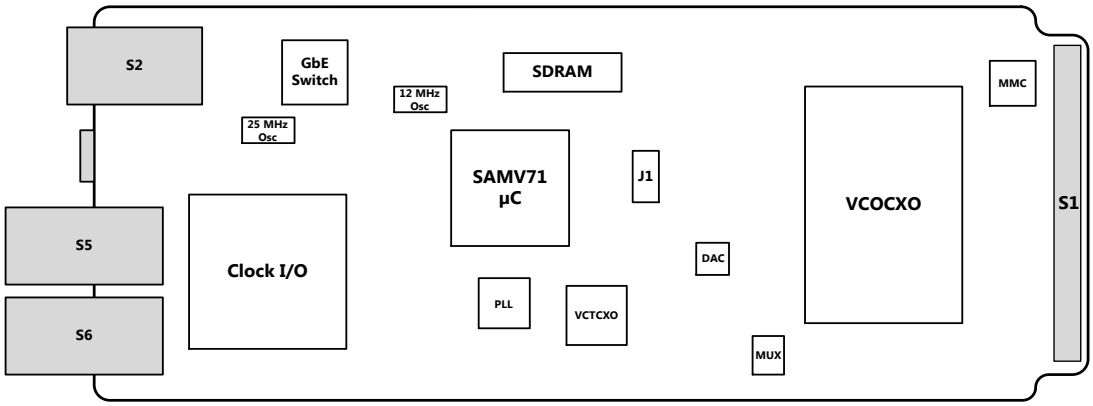
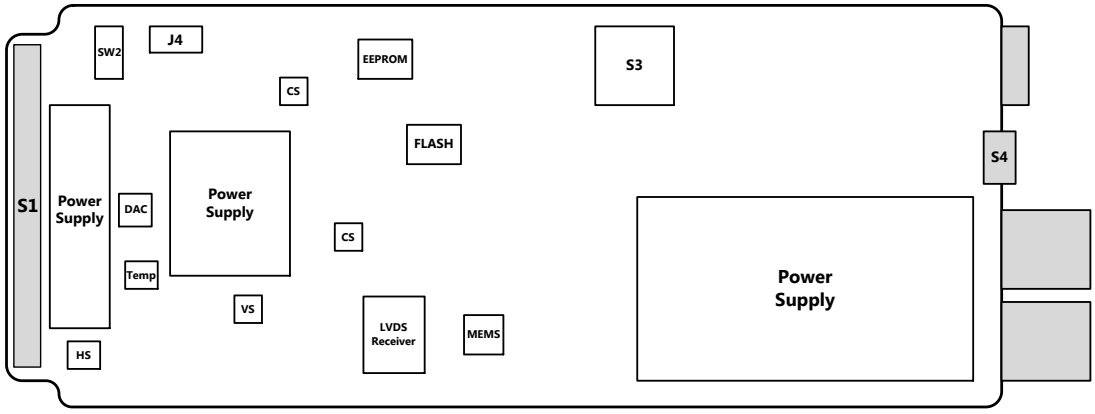


Figure 7 – Location Diagram – Bottom



VS: Voltage Sensor CS: Current Sensor MEMS: Acceleration Sensor

Connectors on top side: drawings imply the board is orientated with the AMC Edge Connector to the ***right*** side

Connectors on bottom side: drawings imply the board is orientated with the AMC Edge Connector to the ***left*** side

Please refer to the following tables to look up the connector pin assignment of the **NAMC-PTM**.

6.2.1. J1: SWD Debug Port

Connector J1 offers a debugging port towards the Atmel/Microchip SAMV71 µC.

Figure 8 – J1: SWD Debug Port

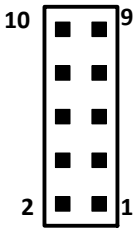


Table 3 – J1: SWD Debug Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	3P3V	SWD_IO	2
3	GND	SDW_CLK	4
5	GND	SWO/TRACE	6
7	nc	nc	8
9	GND	TARGET_RESETn	10

6.2.2. J4: Atmel Programming Header

Connector J4 connects to the programming-port of the MMC Atmel µC device.

Figure 9 – J4: Atmel Programming Header

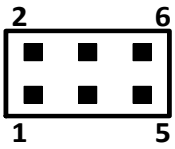


Table 4 – J4: Atmel Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V_MP_LIMSAMV71	2
3	RXD	TXD	4
5	PDI_CLK	GND	6

6.2.3. S1: AMC Connector

Figure 10 – S1: AMC-Connector (top view)

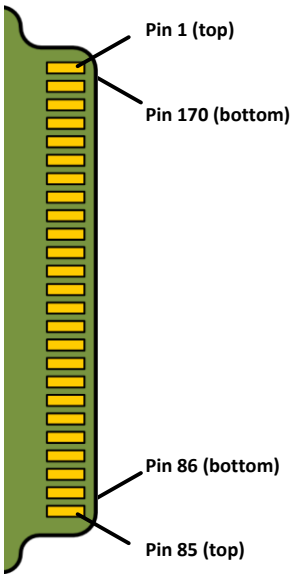


Table 5 – S1: AMC-Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	+12V	TDI	169
3	PS1 (NC in PTM Slot)	TDO	168
4	MP	\TRS	167
5	GA0	TMS	166
6	RSRVD6	TCLK	165
7	GND	GND	164
8	RSRVD8	NC	163
9	+12V	NC	162
10	GND	GND	161
11	TX0+	NC	160
12	TX0-	NC	159
13	GND	GND	158
14	RX0+	NC	157
15	RX0-	NC	156
16	GND	GND	155
17	GA1	NC	154
18	+12V	NC	153
19	GND	GND	152
20	TX1+	NC	151
21	TX1-	NC	150
22	GND	GND	149
23	RX1+	NC	148

Pin #	Signal	Signal	Pin #
24	RX1-	NC	147
25	GND	GND	146
26	GA2	NC	145
27	+12V	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	TCLKD+	139
33	NC	TCLKD-	138
34	GND	GND	137
35	NC	TCLKC+	136
36	NC	TCLKC-	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	ENABL	NC	130
42	+12V	NC	129
43	GND	GND	128
44	NC	NC	127
45	NC	NC	126
46	GND	GND	125
47	NC	NC	124
48	NC	NC	123
49	GND	GND	122
50	NC	NC	121
51	NC	NC	120
52	GND	GND	119
53	NC	NC	118
54	NC	NC	117
55	GND	GND	116
56	SCL	NC	115
57	+12V	NC	114
58	GND	GND	113
59	NC	NC	112
60	NC	NC	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	SDA	NC	100
72	+12V	NC	99

Pin #	Signal	Signal	Pin #
73	GND	GND	98
74	TCLKA+	NC	97
75	TCLKA-	NC	96
76	GND	GND	95
77	TCKLB+	NC	94
78	TCKLB-	NC	93
79	GND	GND	92
80	NC	NC	91
81	NC	NC	90
82	GND	GND	89
83	PS0 (NC in PTM Slot)	NC	88
84	+12V	NC	87
85	GND	GND	86

6.2.4. S2: RJ45 Connector

Figure 11 – S2 RJ45 Ethernet Connector

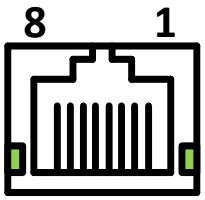


Table 6 – S2: RJ45 Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MX0+	MX0-	2
3	MX1+	MX2+	4
5	MX2-	MX1-	6
7	MX3+	MX3-	8

6.2.5. S3: MicroSD-Card Slot

The **NAMC-PTM** can be equipped with a Micro-SD-Card which can be used as removable FLASH memory.

Figure 12 – S3: Micro-SD-Card Slot

Table 7 – S3: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SD_DATA2	SD_DATA3	2
3	SD_CMD	3P3V	4
5	SD_CLK	GND	6
7	SD_DATA0	SD_DATA1	8

6.2.6. S4: Debug Connector

S4 features a Micro-USB debug interface on the **NAMC-PTM**.

Figure 13 – S4: USB Debug Connector

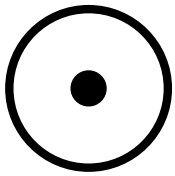
Table 8 – S4: USB Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC	D-	2
3	D+	Nc	4
5	GND	SGND	6
7	SGND	SGND	8
9	SGND	SGND	10
11	SGND		

6.2.7. S5/S6: Clock Connectors

The **NAMC-PTM** owns a clock output at the front plate (S5) as well as a clock input (S6) in shape of a 50Ω BNC connector.

Figure 14 – S5/S6: Clock Connectors



The signal is routed via the pin, the shield is connected to GND.

6.3. Switches

6.3.1. SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

6.3.2. SW2: Multipurpose DIP-Switch

The tables below provide information on the operating parameters and configuration options of SW2.

Figure 15 – SW2: Multipurpose Dip-Switch

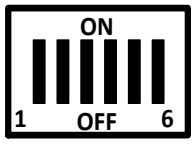


Table 9 – SW2 – Operating Parameters

Switch #	Function
SW2-1	Future use for Atmel IPMI-µC
SW2-2	Future use for Atmel IPMI-µC
SW2-3	Future use for Atmel IPMI-µC
SW2-4	Future use for Atmel IPMI-µC
SW2-5	PTM-MCH Assignment
SW2-6	Future use for Atmel/Microchip SAMV71

Table 10 – DIP SW2 – Configuration

Switch #	ON	OFF
SW2-1	Tbd	***Tbd***
SW2-2	Tbd	***Tbd***
SW2-3	Tbd	***Tbd***
SW2-4	Tbd	***Tbd***
SW2-5*****	Assigns PTM to MCH #2	***Assigns PTM to MCH #1***
SW2-6	Tbd	***Tbd***

Note:

*****Adjustment of DIP-SW5 is only valid if the **NAMC-PTM** is operated in a standard AMC-slot!

Default configuration is labelled with ***bold, italic letters***.

7. SOFTWARE

The software relevant aspects of the PTM development can be divided into the following sections.

7.1. PTM Local Software

The software running on the SAMV71 microcontroller will be based on the FreeRTOS operating system. A board support package (BSP) will be prepared as an example project and will cover at least the following items:

- Bootloader
- FreeRTOS Kernel
- Driver for internal Ethernet MAC
- Driver for basic Ethernet switch control
- IP stack (lwIP)
- Driver for communication via IPMI
- Access driver for external components like
    - Serial console via USB
    - All sensors
    - SPI Flash
    - MicroSD-Card
    - DAC devices

The implementation/adaptation and optimization of the algorithms to perform the desired OCXO tuning/compensation will be handled by the customer.

7.1.1. Software Update Procedure

To update the Software on the SAMV71, a HPM based procedure will be realized as specified in the µTCA and AMC standards. Thus, by using RMCP through the **NAT-MCH**, the software can be written to the internal and external flash devices over UDP from an update agent like ipmitool.

The MMC will initiate the update by asserting the dedicated firmware request GPIO which will put the SAMV71 into the bootloader that resides within a dedicated flash partition. The MMC will then forward IPMI firmware update packets to the SAMV71 microcontroller using an I^2C bus connection. The SAM will then write the contents to the flash memory. The

firmware image will be verified using a SHA hash during boot and the end of the update process. In case the firmware is not valid, the SAMV71 will reside in the bootloader.

7.2. MCH Firmware Extensions

If the **NAMC-PTM** operates in a standard AMC slot, no **NAT-MCH** firmware adaptions are needed. However, in the target system the PTMs will be assembled in special slots which are not covered by the µTCA standard. Therefore the **NAT-MCH** firmware has to be extended to manage the PTMs in this case. That will include most of the standard AMC management tasks, especially

- Detection of the presence of a PTM
- Readout of static module information like serial number or version
- Power budged calculation
- Monitoring of sensor values of temperature and voltage sensors (independently from sensors for the Crystal Oscillator)

These extensions will be accomplished with the development of the firmware of the MMC on the PTM realizing the IPMI communication with the **NAT-MCH**.

The configuration of the **NAT-MCH-CLK** module routing can be done via the already available script-based mechanism of the current **NAT-MCH** firmware.

8. SPECIFICATIONS AND COMPLIANCES

8.1. Internal Reference Documentation

- **NAT-MCH** User's Manual
  https://www.nateurope.com/manuals/nat_mch_man_usr.pdf
- **NAT-MCH-PHYS** Hardware Reference Manual
  Please contact N.A.T.
- **NAT-MCH-CLK-PHYS** Hardware Reference Manual
  https://www.nateurope.com/manuals/nat_mch_clk_phys_man_hw.pdf

8.2. External Reference Documentation

- Atmel SAMV71 ARM-based MCU, Rev.44003E, 10/2016
- Analog Devices AD9545 PLL and Jitter Cleaner, Rev.B, 10/2018
- Connor Winfield M725 VCTCXO, Rev.09, 11/2016
- Microsemi OX-171 OCXO, Rev. 8-7-18
- Kionix 126-1063 MEMS sensor, Rev2.0, 02/2018
- Texas Instruments INA226 Current and Power Monitor, Rev.A, 08/2015
- Texas Instruments INA3221 Voltage Monitor, Rev.B, 03/2016
- Texas Instruments TMP 10x Temperature Sensor, Rev.I, 11/2015

8.3. Standards Compliance

- PICMG AMC.0 Rev. 2.0
- IPMI Specification v2.0 Rev. 1.0

8.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

8.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

8.6. Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

8.7. Product Safety

The board complies with EN60950 and UL1950.

8.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8.9. Abbreviation List

Table 11 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
BNC	Bayonet Neill Concelman – Coax Connector
DAC	Digital Analog Converter
dBM	Decibel Milliwatts
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
FLASH	Non-Volatile Memory
GbE	Gigabit Ethernet
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MCH	µTCA Carrier Hub
MEMS	Micro-Electro-Mechanical System
MicroSD-Card	Micro Secure Digital Memory Card
MLVDS	Multipoint Low Voltage Differential Signaling
MMC	Module Management Controller
MUX	Multiplexer
PLL	Phase-Locked Loop
(P)ROM	(Programmable) Read Only Memory
PTM	Precision Timing Module
RMCP	Remote Management Control Protocol
SDRAM	Synchronous Dynamic Random Access Memory
SHA	Secure Hash Algorithm

Abbreviation	Description
SPI	Serial Peripheral Interface
TCKL	Telecom Clock
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCOCXO	Voltage Controlled Oven Compensated Crystal Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator

9. DOCUMENT'S HISTORY

Table 12 – Document's History

Rev	Date	Description	Author
1.0	13.02.2019	initial release	se
	27.032019	corrected layout issues	se