NAMC-ODSP-M
DSP AMC Module
Technical Reference Manual V1.1
HW Revision 1.0

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

Table of Contents

List of Tables

List of Figures

Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

Table 1: **List of used abbreviations**

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
BDM	Background Debug Mode
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
ECC	Error Correction Code
FCLK	Fabric Clock
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GMII	Gigabit Media Independent Interface
I²C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
iTDM	Internal TDM
LSB	Least Significant Bit
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MSB	Most Significant Bit
MUX	Multiplexing Unit
PCB	Printed Circuit Board
PHY	Physical Layer Device
R/W	Read/Write
RAM	Random Access Memory
(P)ROM	(Programmable) Read Only Memory
SerDes	Serializer/Deserializer
SGMII	Serial GMII
SPI	Serial Peripheral Interface
TCKL	Telecom Clock
TDM	Time Division Multiplex
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XAUI	10 GbE (via 4x 3.125 GB/s)

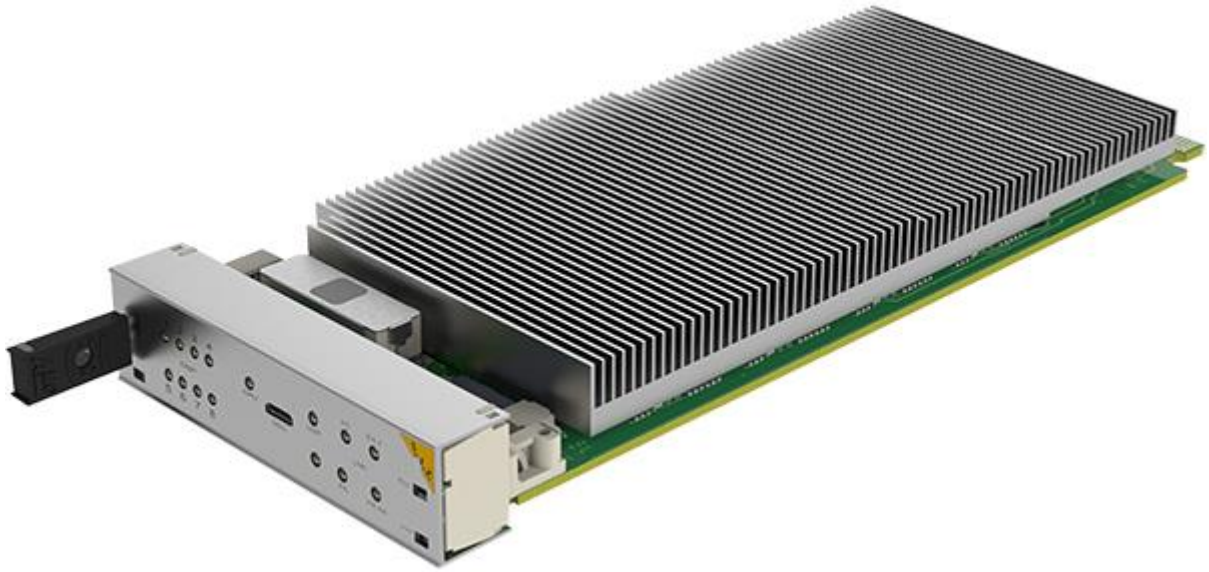
1 Introduction

The NAMC-ODSP-M from N.A.T. combines a powerful FPGA with an array of DSPs, an on-board switch and advanced media gateway software in a single-width, mid-size AMC module package to make it easier to add video and audio acceleration to any communications and networking systems.

Form factor for this board is the Advanced Mezzanine Card (AMC) standard, offering access to the flexible and powerful system standards ATCA and µTCA.

The following figure shows a picture of the **NAMC-ODSP-M:**

Figure 1: **NAMC-ODSP-M**



2 Overview

2.1 Major Features

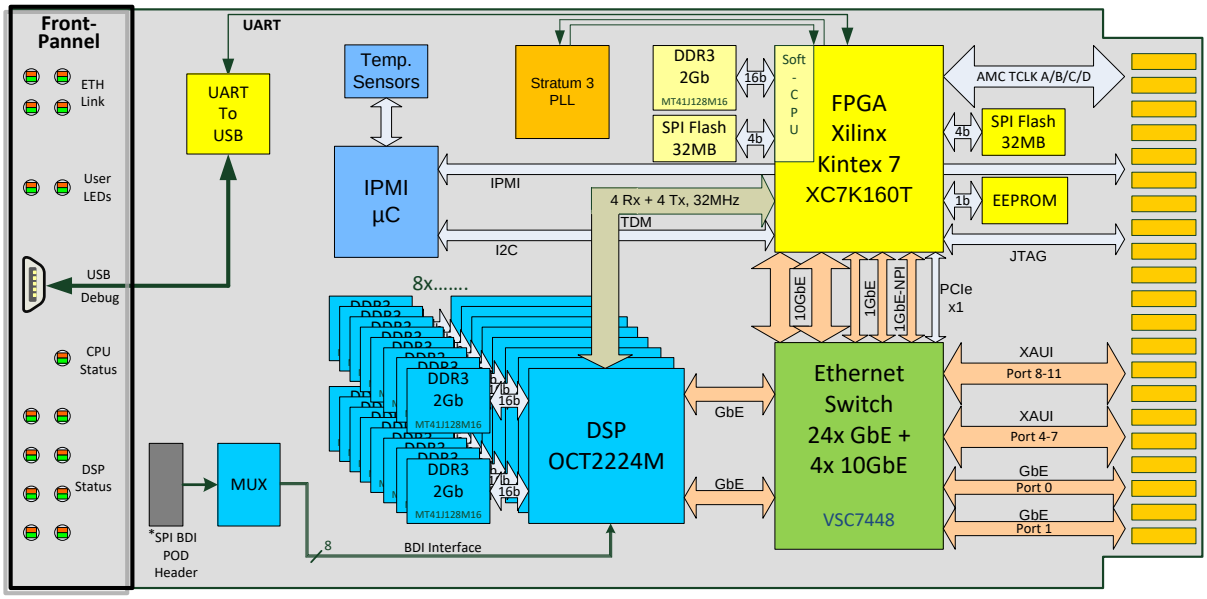
- DSP – Octasic OCT2224M
  - 24 OPUS2 Cores
  - C programmable DSP
  - 6 dynamically reconfigurable Hardware Acceleration Blocks (HABs)
  - TDM interface
  - 3W typical power consumption
- FPGA: Xilinx Kintex7 XC7K160T
  - 160k LE
  - 12Mbit internal SRAM
  - 8 SerDes
- CPU: Xilinx Microblaze Softcore in FPGA
- 512MB DDR3 DRAM per DSP
- 2x 32MB NOR Flash memory
- Secured EEPROM
- Advanced Ethernet Switch Vitesse VSC7448
  - 4 x 10GbE
  - 21x GbE
  - VLAN, QoS, Advanced options
- Backplane Interfaces:
  - 2x XAUI to AMC fat pipe region
  - 2x Gigabit Ethernet to AMC Ports 0/1
  - TCLKA/B/C/D
- Front Panel Interfaces:
  - USB

For detailed description see the following chapter.

2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-ODSP-M**.

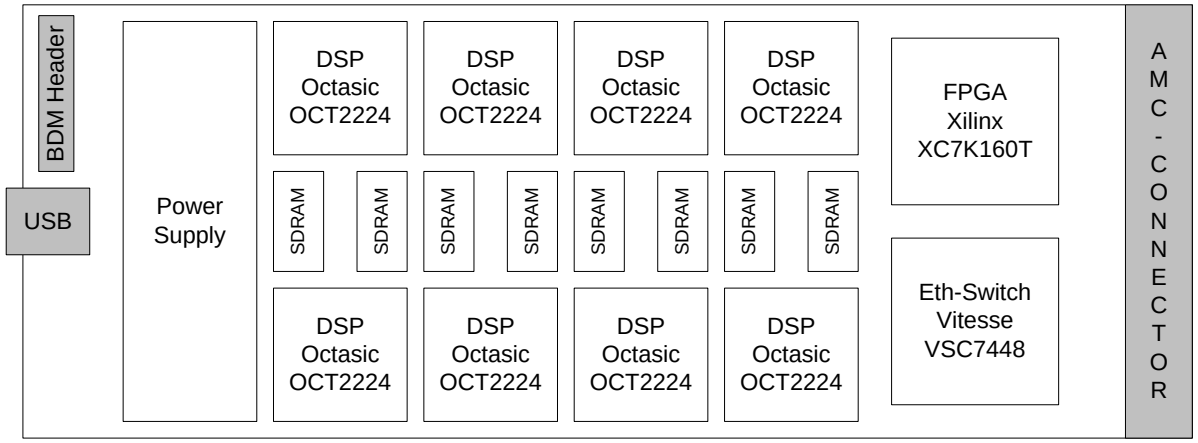
Figure 2: **NAMC-ODSP-M – Block Diagram – Overview**



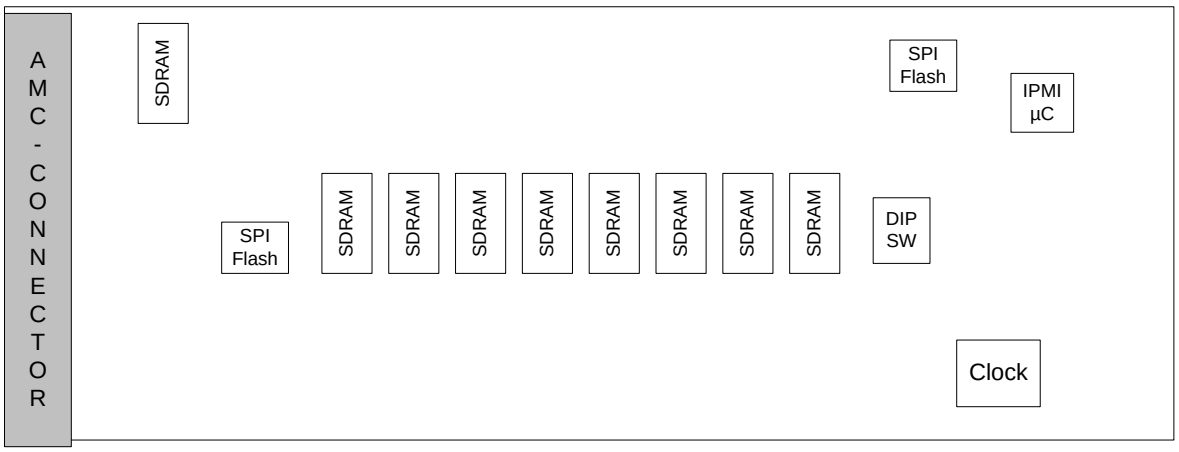
2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: **NAMC-ODSP-M – Location Diagram – Overview**



Top View



Bottom View

3 Board Features

The **NAMC-ODSP-M** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 DSP

The **NAMC-ODSP-M** has an array of eight Octasic OCT2224M devices assembled. All DSP all connected via two GbE interface towards the central Ethernt switch and further they have via the FPGA ITDM connectivity, each DSP 1024 64kbit/s (standard) channels.

An indicator LED is supported for each DSP to provide a visual feedback of the current load balancing between the individual DSP chips (option).

3.2 FPGA

The **NAMC-ODSP-M** is equipped with a Xilinx FPGA which implements several blocks:

- Microblaze soft-core CPU
- ITDM <-> TDM Engine
- Media Flow Aggregator (optional)

All clocking relevant signals are present at the FPGA to provide maximum flexible clocking structure for the board.

3.3 Memory

3.3.1 DSP DDR3 DRAM

The onboard per-DSP DDR3 DRAM memory is 32-bit wide and is per default assembled with 512MB DDR3 SDRAM.

3.3.2 CPU DDR3 DRAM

The onboard Microblaze CPU DDR3 DRAM memory is 16-bit wide and is per default assembled with 256MB DDR3 SDRAM

3.3.3 FPGA Basic SPI Flash

On power up the FPGA configures itself from a serial attached SPI NOR Flash device. Beside the FPGA configuration file this memory is used to store the CPU's first-stage bootloader and further the UBoot and Linux Kernel images. Per default it is 32MB in size.

3.3.4 FPGA Secondary SPI Flash

A further SPI NOR Flash device is available to store further software elements belonging to the Linux system or files like the DSP firmware. Per default it is 32MB in size.

3.3.5 EEPROM

An EEPROM with security feature and an unique serial number can be used to store board-individual items like serial number and license elemets.

3.4 Ethernet Architecture

The NAMC-ODSP-M is equipped with a powerful and feature rich Ethernet switch, the Vitesse VSC7448. It is configured via an API that runs on the Microblaze Linux. Features like VLAN, various prioritization mechanisms, redundancy options, etc. can be used to optimize the Ethernet flow both within the NAMC-ODSP-M board and as well towards the backplane.

It interconnects the following nodes (as also shown in the block diagram):

- Per DSP one primary GbE
- Per DSP one secondary GbE
- FPGA ITDM GbE
- FPGA Microblaze GbE
- FPGA aux. GbE
- FPGA primary 10GbE (can be used for Media Flow Aggregator extension)
- FPGA secondary 10GbE (can be used for Media Flow Aggregator extension)
- Backplane Port 0 GbE
- Backplane Port 1 GbE
- Backplane Port 4-7 10GbE (XAUI)
- Backplane Port 8-11 10GbE (XAUI)

3.5 Backplane Interfaces

3.5.1 XAUI

The most powerful interface to be used with the NAMC-ODSP-M is the 10Gb/s Ethernet transmitted via 4 parallel 3.125Gbaud/s lanes (XAUI). This protocol offers a lot of headroom to aggregate multiple NAMC-ODSP-M together using an MCH with XAUI Ethernet switch.

3.5.2 Gigabit Ethernet

The **NAMC-ODSP-M** is equipped with two Gigabit Ethernet paths connecting to the backplane AMC ports 0 and 1.
Per default the Ethernet interfaces on Port 0 is available in any MTCA or ATCA system and for many application the available bandwidth will be sufficient.

3.6 Front Panel Interfaces

3.6.1 MicroUSB

The **NAMC-ODSP-M** features a MicroUSB jack on its face plate which connects to an USB-to-serial converter chip. It can be used to access the serial terminal on the Microblaze CPU that runs the on-board Linux.

3.7 AMC Clock Interface

The **NAMC-ODSP-M** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D and FCLKA.

All TCLK ports are connected directly to the FPGA and can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from a packet stream or to synchronize the **NAMC-ODSP-M** to an external clock.

4 Hardware

4.1 AMC Port Definition

Table 2: **AMC Port Mapping Strategy**

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and CPU Ethernet), default
	1		1000BaseX Ethernet Channel 2 (iTDM and CPU Ethernet), redundant
	2		SATA
	3		SATA
	4	Fat Pipes	XAUI1 Lane 0
	5		XAUI1 Lane 1
	6		XAUI1 Lane 2
	7		XAUI1 Lane 3
Extended Connector	8	Region	XAUI2 Lane 0
	9		XAUI2 Lane 1
	10		XAUI2 Lane 2
	11		XAUI2 Lane 3
	12	Extended Options Region	unassigned
	13		unassigned
	14		unassigned
	15		Unassigned
	16		TCLKC / TCLKD
	17		unassigned
	18		unassigned
	19		unassigned
	20		unassigned

4.2 Front Panel and LEDs

The **NAMC-ODSP-M** module is equipped with various LED to display an overview real time status of the most important board functions.

A detailed description of these will follow in a later version of this manual.

4.3 Connector

S1: AMC Connector

Table 3: **S1: AMC Connector – Pin-Assignment**

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	NC	163
9	PWR	NC	162
10	GND	GND	161
11	PORT0_TX_P	NC	160
12	PORT0_TX_N	NC	159
13	GND	GND	158
14	PORT0_RX_P	NC	157
15	PORT0_RX_N	NC	156
16	GND	GND	155
17	GA1	NC	154
18	PWR	NC	153
19	GND	GND	152
20	PORT1_TX_P	NC	151
21	PORT1_TX_N	NC	150
22	GND	GND	149
23	PORT1_RX_P	NC	148
24	PORT1_RX_N	NC	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	PORT2_TX_P	NC	142
30	PORT2_TX_N	NC	141
31	GND	GND	140
32	PORT2_RX_P	TCLKD_P	139
33	PORT2_RX_N	TCLKD_N	138
34	GND	GND	137
35	PORT3_TX_P	TCLKC_P	136
36	PORT3_TX_N	TCLKC_N	135
37	GND	GND	134
38	PORT3_RX_P	NC	133
39	PORT3_RX_N	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129

Pin #	AMC-Signal	AMC-Signal	Pin #
43	GND	GND	128
44	PORT4_TX_P	RESVD	127
45	PORT4_TX_N	NC	126
46	GND	GND	125
47	PORT4_RX_P	NC	124
48	PORT4_RX_N	NC	123
49	GND	GND	122
50	PORT5_TX_P	NC	121
51	PORT5_TX_N	NC	120
52	GND	GND	119
53	PORT5_RX_P	NC	118
54	PORT5_RX_N	NC	117
55	GND	GND	116
56	IPMB_SCL	NC	115
57	PWR	NC	114
58	GND	GND	113
59	PORT6_TX_P	NC	112
60	PORT6_TX_N	NC	111
61	GND	GND	110
62	PORT6_RX_P	PORT11_TX_P	109
63	PORT6_RX_N	PORT11_TX_N	108
64	GND	GND	107
65	PORT7_TX_P	PORT11_RX_P	106
66	PORT7_TX_N	PORT11_RX_N	105
67	GND	GND	104
68	PORT7_RX_P	PORT10_TX_P	103
69	PORT7_RX_N	PORT10_TX_N	102
70	GND	GND	101
71	IPMB_SDA	PORT10_RX_P	100
72	PWR	PORT10_RX_N	99
73	GND	GND	98
74	TCLKA_P	PORT9_TX_P	97
75	TCLKA_N	PORT9_TX_N	96
76	GND	GND	95
77	TCLKB_P	PORT9_RX_P	94
78	TCLKB_N	PORT9_RX_N	93
79	GND	GND	92
80	FCLKA_P	PORT8_TX_P	91
81	FCLKA_N	PORT8_TX_N	90
82	GND	GND	89
83	/PS0	PORT8_RX_P	88
84	PWR	PORT8_RX_N	87
85	GND	GND	86

5 Programming Notes

5.1 TDM/ITDM Connectivity

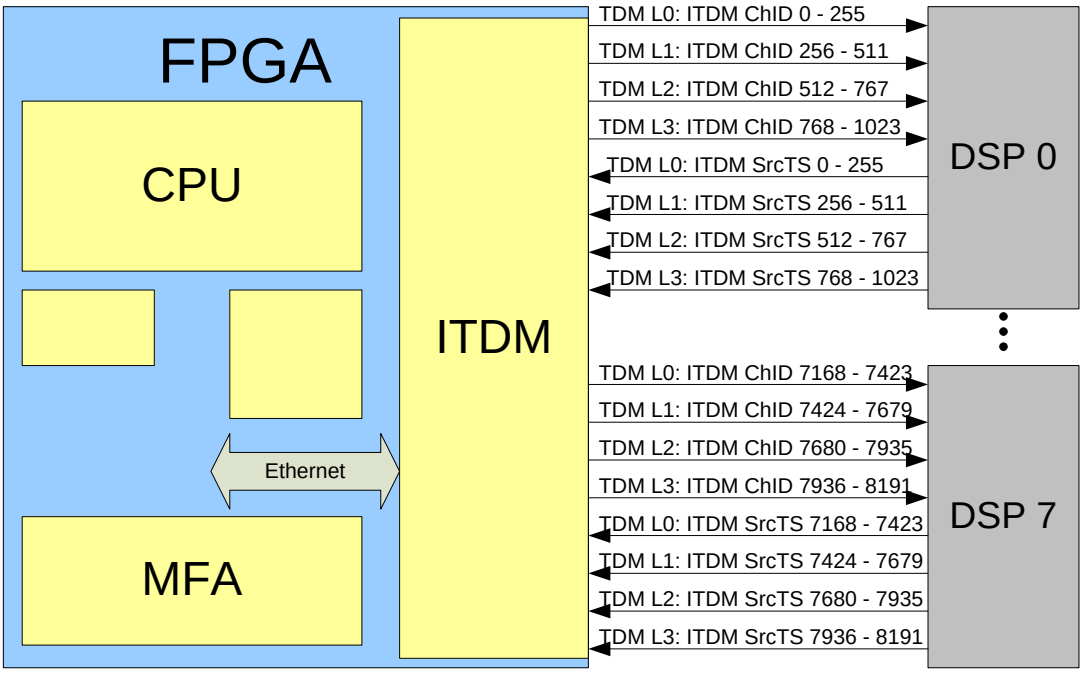
The block diagram below shows what ITDM channel-id is connected to what DSP TDM line and time-slot. There is a one-by-one relationship between the number of the ITDM channel-id in incoming direction and the ITDM engine local time-slot number in outgoing direction. The displayed connectivity can also be expressed in the following formula:

Ch-ID/Local-TS# = (DSP# * 1024) + (DSP-TDM-Line# * 256) + TS#

Table 4: **ITDM Ch-ID /Time-Slot Calculation**

Parameter	Function
Ch-ID	ITDM Channel-ID: Data coming into the NAMC-ODSP-M on a certain Ch-ID will be connected to a specific DSP time-slot as documented here.
Local-TS#	Number of the local time-slot that can be connected to any outgoing ITDM connection towards another ITDM endpoint.
DSP#	Number of the DSP one the NAMC-ODSP-M ranging from 0 to 7.
DSP-TDM-Line#	Number of the physical TDM line of a DSP. Each DSP has four TDM lines towards the FPGA ranging from 0 to 3. In the Vocallo API referred to as stream-id.
TS#	Number of the time-slot on a specific TDM line (stream-id) between FPGA and a DSP.

Figure 4: **NAMC-ODSP-M – TDM/ITDM Connectivity**



Board Specification

Table 5: **NAMC-ODSP-M Specification – Overview**

Processors	Xilinx Microblaze CPU within FPGA 8x Octasic OCT2224M DSP
AMC-Module	Standard Advanced Mezzanine Card, single width
Front-I/O	MicroUSB for serial terminal
Main Memory	256MB DDR3 SDRAM on Microblaze CPU 512MB DDR3 SDRAM per DSP
FLASH PROM	2x 32MB NAND Flash
Firmware	LINUX (on Microblaze CPU)
Power Consumption	12V, 4.5A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.2 Rev. 1.0 (Type E2) PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0

6 Installation

6.1 Safety Note

To ensure proper functioning of the **NAMC-ODSP-M** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-ODSP-M** read this installation section
- Before installing or uninstalling the **NAMC-ODSP-M**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-ODSP-M** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary
    - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-ODSP-M** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

6.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

6.2.1 Requirements

The installation requires only:

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-ODSP-M**
- power supply
- cooling devices

6.2.2 Power supply

The power supply for the **NAMC-ODSP-M** must meet the following specifications:

- required for the module: +12V / 2.5A max.

6.2.3 Automatic Power Up

In the following situations the **NAMC-ODSP-M** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
- when +12V voltage level drops below 10V
- when +3.3V voltage level drops below 3.00V
- The carrier board / backplane signals a PCIe-Reset.

6.3 Statement on Environmental Protection

6.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.3.4 Product Safety

The board complies with EN60950 and UL1950.

6.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1]
[2]

Appendix B: Document's History

Revision	Date	Description	Author
1.0	13.05.2016	initial release	te
1.1	27.05.2016	corrected product name to NAMC-ODSP-M	hk