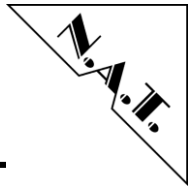

NAT-MCH
Clock-Module
Technical Reference Manual V 1.1
CLK Module HW Revision 3.1

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1: gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Board Specification

Table 2: NAT-MCH CLK Module Features

Power Consumption	12 V / 0.5 A max. (only **CLK Module**)	
Environmental Conditions	Temperature (operating):	0°C to +55°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards Compliance	PICMG µTCA.0 Rev. 1.0	
	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 2.0	
	IPMI Specification v2.0 Rev. 1.0	
Product Safety	The board complies with EN60950 and UL1950	
PLL Input Frequencies *(To be sourced from external Reference via Face Plate Connector, CLK1, CLK2 or CLK3)*	• Any multiple of 2 kHz up to 131.072 MHz. • Any multiple of 8 kHz up to 155.52 MHz. *(clocks via backplane are restricted to a maximum frequency of 100MHz by the MicroTCA specification)*	
PLL Output Frequencies *(To be distributed via Face Plate Connector, CLK1, CLK2 or CLK3)*	• Any multiple of 2 kHz up to 77.76 MHz. • Any multiple of 8 kHz up to 311.04 MHz • Any multiple of 8 kHz up to 388.79 MHz • Frame sync. of 8 kHz and 2 kHz *(clocks via backplane are restricted to a maximum frequency of 100MHz by the MicroTCA specification)*	

2 Statement on Environmental Protection

2.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

3 Installation

3.1 Safety Note

To ensure proper functioning of the **NAT-MCH CLK Module** during its usual lifetime take refer to the safety note section of the **NAT-MCH BASIC-Module** Technical Reference Manual before handling the board.

3.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

3.2.1 Requirements

The CLK-Module is always mounted on a NAT-MCH BASIC-Module. Therefore please refer to the requirements section of the **NAT-MCH BASIC-Module** Technical Reference Manual.

3.2.2 Power supply

The power supply for the **NAT-MCH CLK Module** must meet the following specifications:

+12 V / 0.5 A max. (only **CLK Module**, in addition to other PCBs of the **NAT-MCH**).

3.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH Basic-Module**

In the following situations the **NAT-MCH Basic-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

4 Introduction

The **NAT-MCH** consists of a **Basic-Module**, which can be expanded with additional PCBs. The **Basic-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **Basic-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB Modules** are available. With the **Clock-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs and a second MCH
- reception of clock signals from either of 12 AMCs, a second MCH or from the front panel input and redistribution

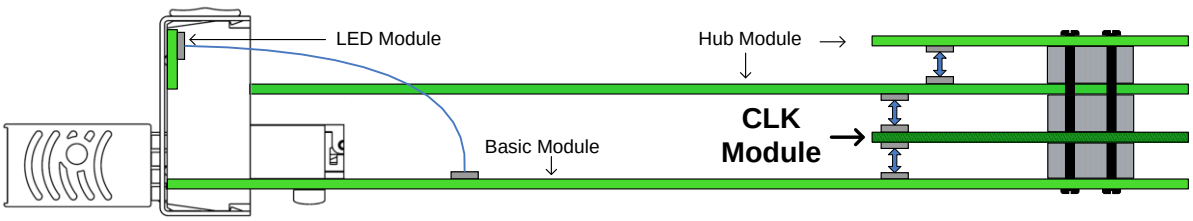
Through the extension of the **NAT-MCH** with a **HUB Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in *Figure 1*.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **Clock-PCB**.

5 CLK Module Basics

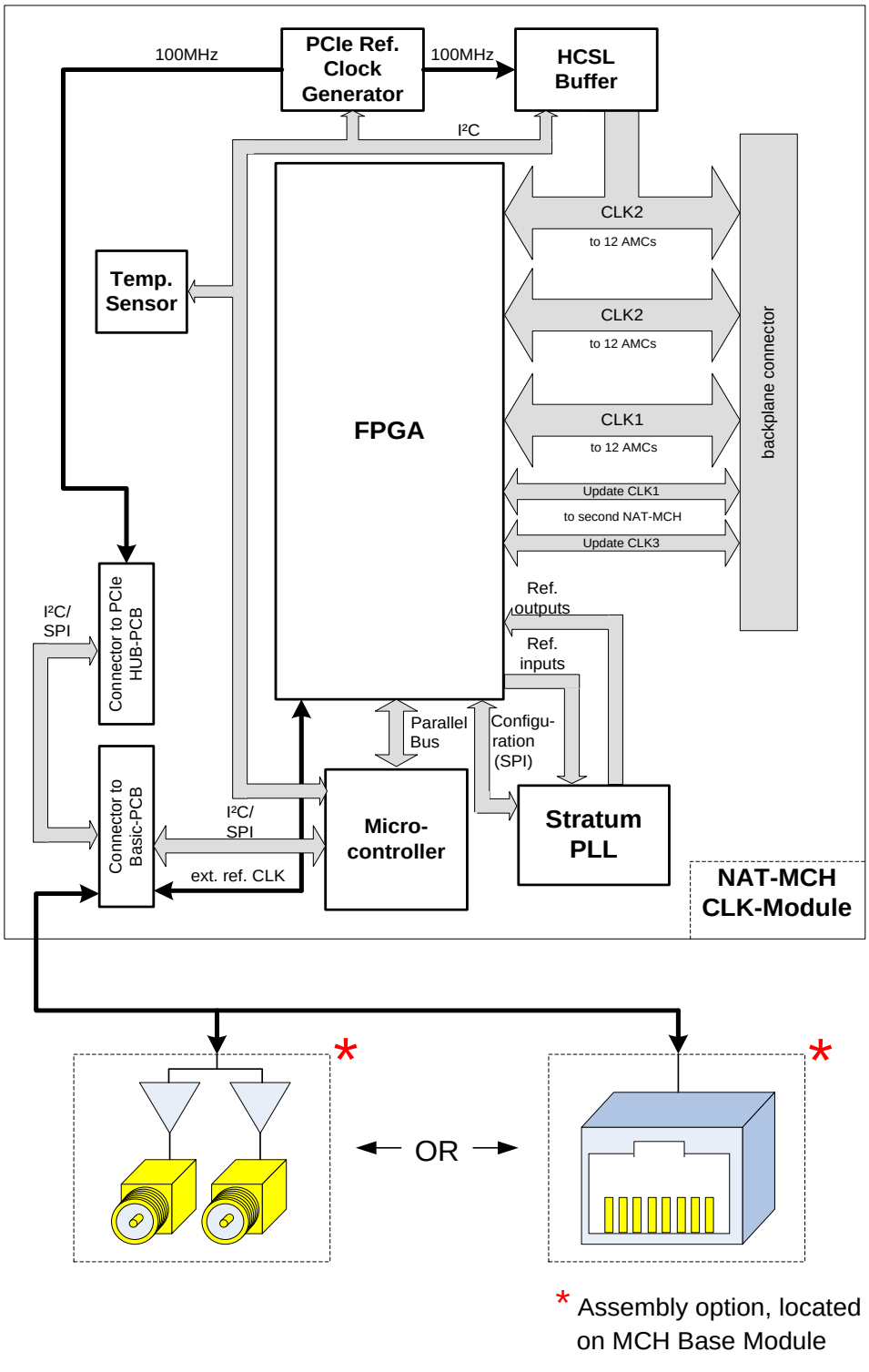
The **CLK Module** can be mounted on the **NAT-MCH Basic-PCB**. With the **CLK Module**, the 2nd tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed. The **NAT-MCH CLK Module** implements the following major features:

- support of AMC clocks CLK1* CLK2* and CLK3* for up to 12 AMCs
- support of update CLK1 and CLK3 for a second **NAT-MCH** in a redundant system
- support of the front panel reference clock In/Outputs
- Stratum 3 or 3E (depending on assembly option) type PLL clock source for telecom applications with various output frequencies
- Telecom CLK signals can be distributed over all backplane clock connections and the front panel interface
- CLK1, CLK2 and CLK3 from all 12 AMCs, the update clocks from a second **NAT-MCH**, or a signal from the front panel interface can be used as reference for the PLL
- a PCI Express compliant clock signal can be distributed via CLK3 to all 12 AMCs (only possible with a installed PCI Express **Hub-Module**)
- Support of M-LVDS **or** HCSL compliant driver and termination for CLK3 (assembly option)

* Please refer to **Appendix A** for a brief description of the correlation between the MicroTCA and AMC clock interface naming

6 Block Diagram of the NAT-MCH CLK Module

Figure 2: Block Diagram of the NAT-MCH CLK Module



7 BOARD FEATURES

- **PLL**

  The board is equipped with a Maxim DS3102 Stratum 2/3E/3 PLL, which provides various typical telecom frequencies in the range from 8 kHz to 65.536 MHz. Especially to the two frequencies 8 kHz and 19.44 MHz, which are recommended for telecom applications by the MicroTCA Specification, are supported. Also 10MHz and 30.72MHz that are often needed for GPS applications are in the supported range.

  The Maxim PLL is only assembled if the "TC-Option" is chosen.

  The Stratum accuracy depends on the assembled reference oscillator. Stratum 2 is not supported. Stratum 3E is supported by the TCOCXO option and Stratum 3 by the TCTCXO option

- **Microprocessor**

  To configure the **CLK Module** an Atmel 8-bit microprocessor resides on the **CLK Module**.

- **Interfaces**

  CLK1: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any of the 12 AMCs.

  CLK2: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any AMC.

  CLK3: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. Depending on the assembly option different signal standards are supported:
  - The M-LVDS option supports M-LVDS compliant in- or outputs.
  - The HCSL option supports HCSL compliant outputs, as recommended for a PCIe reference clock.

  Update CLK: The **NAT-MCH CLK Module** implements 2 update channels (update CLK1 and CLK3). These channels are full-duplex connections to a second NAT-MCH. They can only be used to send and receive telecom clock signals (not the PCI Express clock signal).

  Ext.-ref.-CLK: The **NAT-MCH CLK Module** supports a dual external reference clock in- or output, accessible via a face plate connector. The required

signals are routed to the **Base-Module**, were different clock transceiver modules can be assembled. These transceiver modules are using either SMA connectors or a RJ45 connector, depending on the needed signal standard.

The RJ45 connector is used for LVDS signals and the SMA connectors are used for single ended signals (e.g. TTL or CMOS level signals).

If the external clock interface is used to receive a single ended reference clock, this clock signal is amplified by a special input circuit on the **Transceiver-Module**. This circuit accepts signal forms in a wide range, concerning frequency and input voltage. For a more detailed specification of the input signal please refer to the hardware reference manual of the **Base-Module**.

- **Interface to other NAT-MCH PCBs**

Basic PCB:

- The Microprocessor on the **CLK Module** can be programmed by the CPU on the **Basic-Module** via a SPI interface. Normal communication between the Microprocessor and the CPU is done by IPMI messages via the I²C interface.

- The external clock interface on the front panel is connected to the **CLK Module** via the interface to the **Basic-PCB** (via connector CON2).

PCIe Hub-PCB:

- depending on the HUB Module version the **CLK Module** can receive a PCI Express compliant clock signal from the **Hub-PCB** or transmit that clock signal to the HUB Module. This is only possible with the PCIe HUB Module.

8 Functional Blocks

The **NAT-MCH CLK Module** is divided into a number of functional blocks, which are described in the following paragraphs.

8.1 Stratum PLL

The DS3102 supports the Stratum 2, 3E, 3, 4E and 4 requirements of GR-1244, GR-253, G.812 Types I – IV, G.813 and G.8262. The first four reference inputs of the DS3102 are connected to the FPGA. Via multiplexers in the FPGA it can be decided which source shall be routed to those inputs. These inputs can synchronize to any reference with the frequency of:

- SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
- Ethernet xMII: 2.5, 25, 125, 156.25MHz
- PDH: N x DS1, N x E1, N x DS2, DS3, E3
- Frame Sync: 2kHz, 4kHz, 8kHz
- Custom: Any Multiple of 2kHz Up to 131.072MHz,
- Any Multiple of 8kHz Up to 155.52MHz

By programming the FPGA multiplexers bit, any clock signal from any AMC (either CLK1, CLK2 or CLK3) or from the other NAT-MCH (CLK1 or CLK3 update) can be connected to these reference inputs of the PLL.

If no reference signal is available or if the reference fails the DS3102 uses a 12.8 MHz master clock for frequency generation in a free running/holdover mode. The 12.8 MHz clock is generated by an oscillator.

The DS3102 has seven clock and two frame sync outputs. These outputs are routed to the FPGA and can there be selected as source by any multiplexer. The outputs can programmed to generate the following output frequencies:

- SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
- Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
- PDH: N x DS1, N x E1, N x DS2, DS3, E3
- Other: 10, 10.24, 13, 30.72MHz
- Frame Sync: 2kHz, 8kHz
- Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz,
  Any Multiple of 8kHz Up to 311.04MHz,
  Any Multiple of 10kHz Up to 388.79MHz

The DS3102 PLL is only assembled if the TC-Option is chosen.

Please refer to the manual of the DS3102 PLL [1] for a more detailed description.

8.2 Microprocessor

An Atmel 8-bit microprocessor resides on the **CLK Module**. With the help of this microprocessor, the main CPU of the base board can configure all multiplexers implemented in the FPGA and enable the transceivers for the connection to each AMC. The firmware can be updated by the CPU of the **Base Module** via the SPI interface. The ColdFire communicates with the **CLK Module** via IPMI (using the I²C interface).

8.3 CLK-Multiplex Function

Flexible multiplexing of the various clock signals is achieved by a Lattice FPGA. Multiplexing of source clock signals to destination clock signals is performed by programming a register interface provided by the microcontroller.

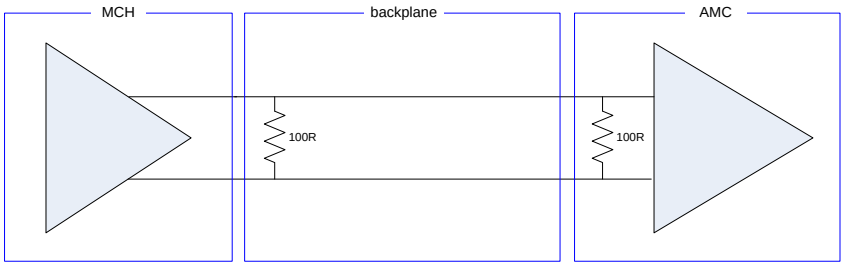
The FPGA with these multiplexers is only assembled with the TC-option

8.4 M-LVDS / HCSL Transceiver

The MicroTCA R1.0 Specification recommends that all clock interfaces are equipped with M-LVDS compliant driver/receiver and termination. Contrary to that the AMC.0 R2.0 allows for FCLKA (formerly CLK3) also HCSL compliant driver/receiver and termination.

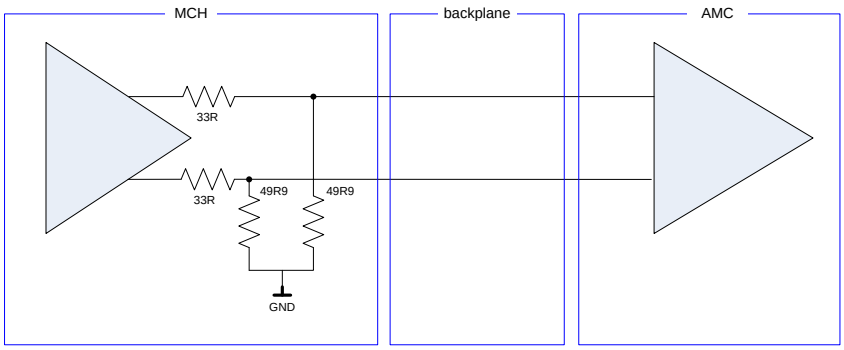
The main difference between the two signal specifications, which makes it difficult to realize both with the same hardware, is the different termination. M-LVDS uses a dual differential termination between the two complimentary clock lines at both ends of the bus. This termination is shown in Figure 3.

Figure 3: M-LVDS Termination



HCSL uses a source-only termination with two series and term-to-ground resistors. This termination is depicted in Figure 4.

Figure 4: HCSL termination



Because of this differences N.A.T. decided to offer two different assembly/ordering options SSCM (Spread Spectrum Clock M-LVDS) and SSCH (Spread Spectrum Clock HCSL). The SSCM option implements M-LVDS compliant Transmitter and termination for CLK3. The SSCH option implements HCSL compliant Transmitter and termination.

Either the SSCM or the SSCH option can be chosen. Beside these two options always the TC option can additionally be chosen. The TC option implements always M-LVDS compliant transceiver and termination for CLK1, CLK2 and Update CLK1/3.

Please Note: It is important that not only the CLK-Module and the AMC modules fit together regarding the termination, also the Backplane need to be selected adequate.

The Backplane shall have a 100Ohm termination if M-LVDS is chosen for CLK3 (refer to Figure 3). If HCSL is chosen for CLK3 the backplane shall have no termination (refer to Figure 4).

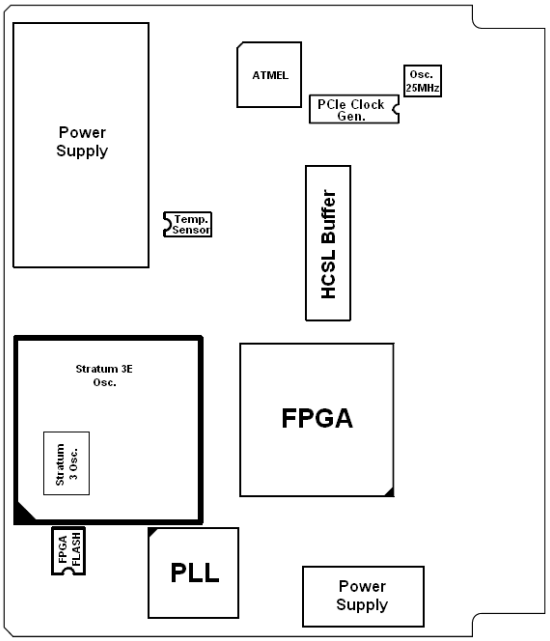
8.5 External Reference clock Transceiver Module

Reference clock signals can be received or transmitted via connectors on the NAT-MCH face plate. Depending on an assembly option different External Reference Clock Transceiver Modules can be chosen. The available Transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL, …) and the supported connector. The different External Reference Clock Transceiver Modules are assembly options of the NAT-MCH Base Module. Therefore the different options are described in more detail in the reference manual of the Base Module.

9 Location Overview

Figure 5 shows the position of important components. Depending on the chosen options it may be that the board does not include all components named in the location diagram.

Figure 5: Location Diagram of the NAT-MCH CLK Module



10 Connectors

10.1 Connector Overview

Figure 6 and Figure 7 are showing the position of the different connectors of the CLK Module.

Figure 6: Connectors of the NAT-MCH CLK Module (top view)

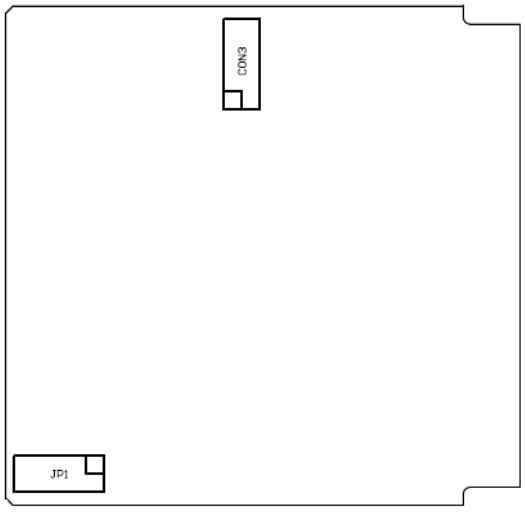
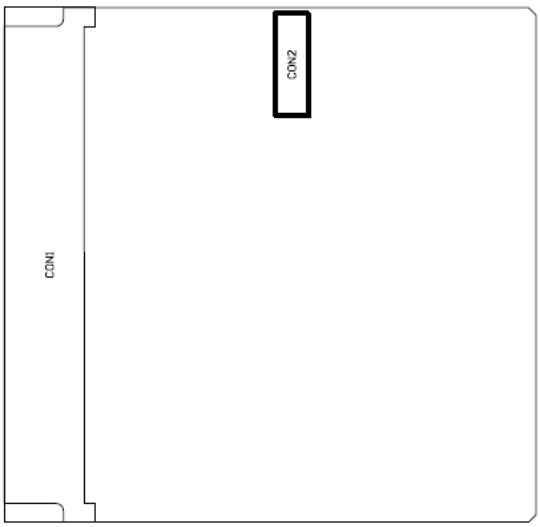


Figure 7: Connectors of the NAT-MCH CLK Module (bottom view)



Please refer to the following tables for the pin assignment of the **NAT-MCH CLK Module**.

10.2 MCH Connector CON1

Table 3: MCH Connector CON1

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	CLK3_Tx+	CLK3_Rx+	163
9	CLK3_Tx-	CLK3_Rx-	162
10	GND	GND	161
11	CLK1_Tx+	CLK1_Rx+	160
12	CLK1_Tx-	CLK1_Rx-	159
13	GND	GND	158
14	TxFB-1+	RxFB-1+	157
15	TxFB-1-	RxFB-1-	156
16	GND	GND	155
17	TxFB-2+	RxFB-2+	154
18	TxFB-2-	RxFB-2-	153
19	GND	GND	152
20	TxFB-3+	RxFB-3+	151
21	TxFB-3-	RxFB-3-	150
22	GND	GND	149
23	TxFB-4+	RxFB-4+	148
24	TxFB-4-	RxFB-4-	147
25	GND	GND	146
26	TxFB-5+	RxFB-5+	145
27	TxFB-5-	RxFB-5-	144
28	GND	GND	143
29	TxFB-6+	RxFB-6+	142
30	TxFB-6-	RxFB-6-	141
31	GND	GND	140
32	CLK3-1+	CLK3-7+	139
33	CLK3-1-	CLK3-7-	138
34	GND	GND	137
35	CLK3-2+	CLK3-8+	136
36	CLK3-2-	CLK3-8-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	CLK3-3+	CLK3-9+	133
39	CLK3-3-	CLK3-9-	132
40	GND	GND	131
41	CLK3-4+	CLK3-10+	130
42	CLK3-4-	CLK3-10-	129
43	GND	GND	128
44	CLK3-5+	CLK3-11+	127
45	CLK3-5-	CLK3-11-	126
46	GND	GND	125
47	CLK3-6+	CLK3-12+	124
48	CLK3-6-	CLK3-12-	123
49	GND	GND	122
50	CLK1-1+	CLK2-1+	121
51	CLK1-1-	CLK2-1-	120
52	GND	GND	119
53	CLK1-2+	CLK2-2+	118
54	CLK1-2-	CLK2-2-	117
55	GND	GND	116
56	CLK1-3+	CLK2-3+	115
57	CLK1-3-	CLK2-3-	114
58	GND	GND	113
59	CLK1-4+	CLK2-4+	112
60	CLK1-4-	CLK2-4-	111
61	GND	GND	110
62	CLK1-5+	CLK2-5+	109
63	CLK1-5-	CLK2-5-	108
64	GND	GND	107
65	CLK1-6+	CLK2-6+	106
66	CLK1-6-	CLK2-6-	105
67	GND	GND	104
68	CLK1-7+	CLK2-7+	103
69	CLK1-7-	CLK2-7-	102
70	GND	GND	101
71	CLK1-8+	CLK2-8+	100
72	CLK1-8-	CLK2-8-	99
73	GND	GND	98
74	CLK1-9+	CLK2-9+	97
75	CLK1-9-	CLK2-9-	96
76	GND	GND	95
77	CLK1-10+	CLK2-10+	94
78	CLK1-10-	CLK2-10-	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	CLK1-11+	CLK2-11+	91
81	CLK1-11-	CLK2-11-	90
82	GND	GND	89
83	CLK1-12+	CLK2-12+	88
84	CLK1-12-	CLK2-12-	87
85	GND	GND	86

10.3 Connector Con2: Interface to Basic-PCB

Connector CON2 connects the **NAT-MCH CLK Module** with the **Basic-PCB**

Table 4: Connector to Basic-PCB CON2

Pin No.	Signal	Signal	Pin No.
1	/SPISEL_CLKPCB	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_OUT_P	+3.3V MP	14
15	EXTREF_OUT_N	SPICLK	16
17	GND	EXTREF_IN	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUB PCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

10.4 Connector CON3: Interface to Hub-PCB

Connector CON3 connects the **CLK Module** with the **HUB-PCB**.

Table 5: Connector to Hub-PCB CON3

Pin No.	Signal	Signal	Pin No.
1	N.C.	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_P	+3.3V MP	14
15	PCIeCLK_N	SPICLK	16
17	GND	expansion3	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUB PCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

10.5 Connector JP1: Lattice FPGA Programming Port

Connector JP1 connects the serial programming-port of the Lattice FPGA device.

Table 6: Lattice FPGA Programming Port

Pin No.	Signal	Signal	Pin No.
1	+3.3V	TDO	2
3	TDI	PROGRAMN	4
5	N.C.	TMS	6
7	GND	TCK	8
9	DONE	/INIT	10

11 NAT-MCH CLK Module Programming Notes

11.1 SPI Interface

The SPI interface on the **CLK Module** is used only for maintenance purposes, e.g. updating the microcontroller firmware or the FPGA image.

11.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **Basic-Module**. All communication is based on IPMI Messages.

11.3 Register

The clock module can generate, receive and transmit various clock signals.

Different clock signals can be received by the clock module via interfaces at the MCH face plate or the backplane interfaces, e.g. CLK1/2/3 connected to AMCs as well as CLK1/2_UD connected to a redundant MCH.

Additional the clock module can generate clock signals on its own. Therefore a stratum 3/3E PLL resides on the clock module. This PLL can generate various frequencies on different outputs either in free run mode or locked onto a reference clock.

Clock signals coming from one of the interfaces described before can serve as reference for the PLL.

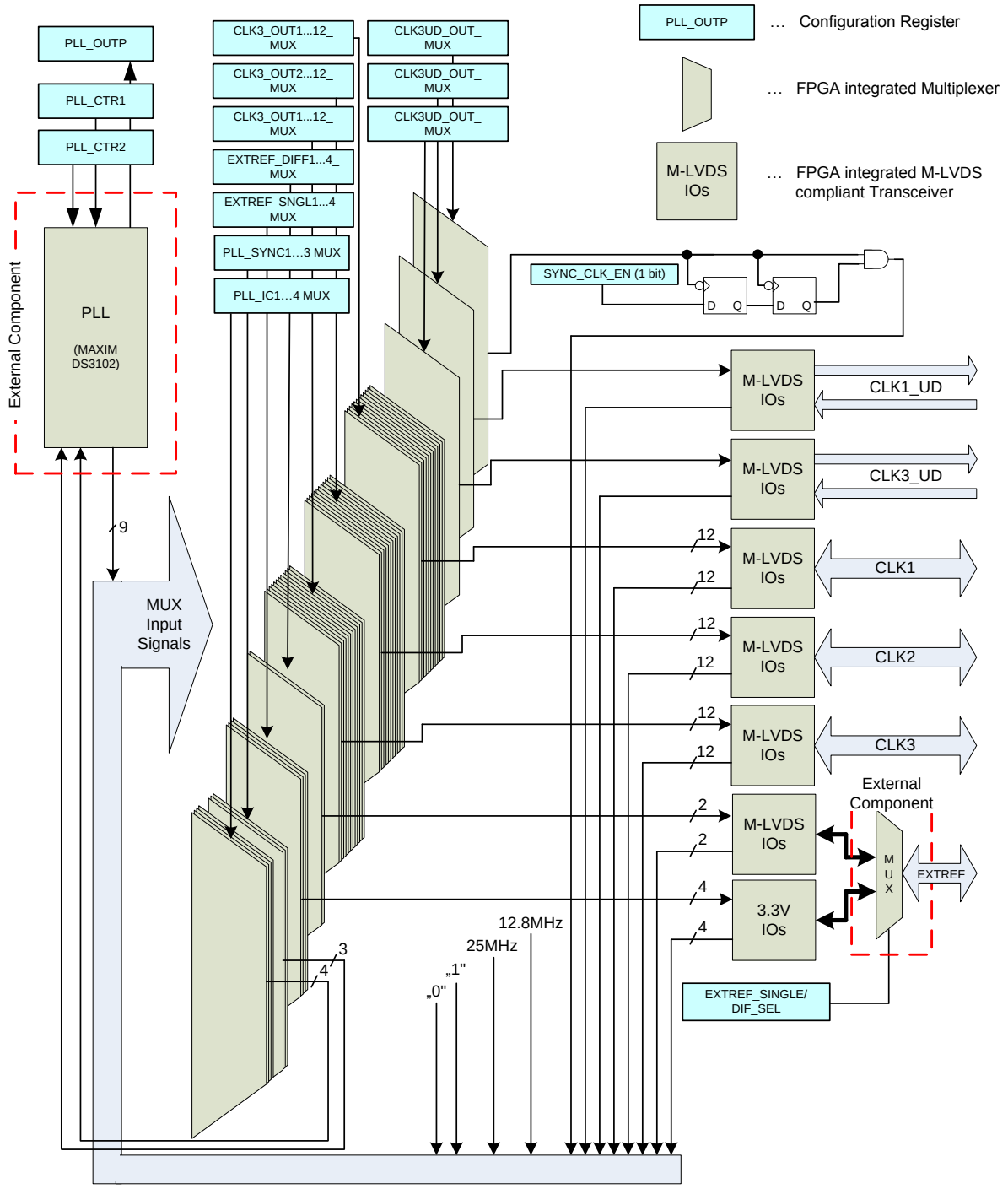
Beside receiving or generating clock signals the clock module can of course also transmit clock signals. This can also be done by the backplane interfaces (CLK1/2/3 and CLK1/2_UD).

The clock signals generated by the PLL can serve as source for the transceiver. Or received signals can directly be routed to other interfaces to be transmitted again.

To allow a maximum flexibility to choose at runtime which clock shall be routed from which interface to which interface a lot of multiplexer are implemented into the clock module FPGA.

To get a better understanding of the (multiplexer-) functions that are implemented in the CLK-Module FPGA Figure 8 is showing a detailed overview.

Figure 8: Detailed Functional overview



The multiplexer and other functions implemented on de clock module can be controlled by a register interface. The following tables are showing a detailed description of the Registers that are available. These registers are not intended to be used by the customer. N.A.T. offers a script based configuration interface that simplifies the complex configuration options. Please refer to chapter 10 “Clock Module Configuration” of the NAT-MCH User Manual for a more detailed description of this interface.

11.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH CLK Module**.

Table 7: Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xb4								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	BOARD_ID							

11.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH CLK Module**.

Table 8: PCB Revision Register

PCB Revision - Address 0x01								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB_REV							

Bit 7 to 4 contains the major revision and bit 3 to 0 contains the minor revision. That means if the PCB revision is e.g. v3.1 the PCB Revision register contains the value 0x31.

11.3.3 Firmware Version Register

The Atmel Version Register contains the Version of the Atmel firmware.

Table 9: FW_VERSION Register

FW Version - Address 0x02								
Default value # of running Firmware version								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FW_VERSION							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the Firmware running on the Atmel is v1.3 the Firmware Version register contains the value 0x13.

11.3.4 FPGA Revision Register

The FPGA Revision Register contains the revision code of the Altera FPGA.

Table 10: FPGA Revision Register

FPGA Revision - Address 0x03								
Default value # of running FPGA revision								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FPGA_REV							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the FPGA is running with the image v1.3 the FPGA Version register contains the value 0x13

11.3.5 CLK1-1 to 12 Output selection Multiplexer Register

The value of the Output selection Multiplexer Registers selects which source is connected to CLK1 of AMC slot 1 to 12.

Table 11: CLK1-1..12_OUT_MUX Register

CLK1-1_OUT_MUX - Address 0x0a								
CLK1-2_OUT_MUX - Address 0x0b								
CLK1-3_OUT_MUX - Address 0x0c								
CLK1-4_OUT_MUX - Address 0x0d								
CLK1-5_OUT_MUX - Address 0x0e								
CLK1-6_OUT_MUX - Address 0x0f								
CLK1-7_OUT_MUX - Address 0x10								
CLK1-8_OUT_MUX - Address 0x11								
CLK1-9_OUT_MUX - Address 0x12								
CLK1-10_OUT_MUX - Address 0x13								
CLK1-11_OUT_MUX - Address 0x14								
CLK1-12_OUT_MUX - Address 0x15								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	CLK1-1..12_OUT_MUX							

Table 12: CLK1-1_OUT_MUX - Register Bits

Bit	Name	Function
[7..0]	CLK1-1..12 _OUT_MUX	**Reference Select for REF0 input of the PLL** 0x00 – High impedance (recommended value for receive functionality) 0x01 – CLK1 of AMC1 0x02 – CLK1 of AMC2 : 0x0C – CLK1 of AMC12 0x0D – CLK2 of AMC1 : 0x18 – CLK2 of AMC12 0x19 – CLK3 of AMC1 : 0x24 – CLK3 of AMC12 0x25 – Update CLK1 Rx (from 2nd MCH) 0x26 – Update CLK3 Rx (from 2nd MCH) 0x27 – Extref_single1 (External reference from face plate, single ended) 0x28 – Extref_single2 0x29 – Extref_single3 0x2A – Extref_single4 0x2B – Extref_diff1 (External reference from face plate, differential) 0x2C – Extref_diff2 0x2D – PLL_OC1b (clock output of the Maxim PLL) 0x2E – PLL_OC2b (clock output of the Maxim PLL) 0x2F – PLL_OC3b (clock output of the Maxim PLL) 0x30 – PLL_OC4b (clock output of the Maxim PLL) 0x31 – PLL_OC5b (clock output of the Maxim PLL) 0x32 – PLL_OC6 (clock output of the Maxim PLL) 0x33 – PLL_OC7 (clock output of the Maxim PLL) 0x34 – PLL_fsync (frame sync output of the Maxim PLL) 0x35 – PLL_mfsync (frame sync output of the Maxim PLL) 0x36 – 12.8 MHz (Stratum3E/3 reference clock) 0x37 – 25 MHz (only with HCSL option) 0x38 – “0” 0x39 – “1” 0x3A – Sync_clk (refer to the Synchronous Clock enable Register for a description) all other values result in undefined output values

The following multiplexers are offering exactly the same reference signals. Therefore Table 12: is also true for these multiplexers and is not repeated.

11.3.6 CLK2-1 to 12 Output selection Multiplexer Register

The value of the Output selection Multiplexer Registers selects which source is connected to CLK2 of AMC slot 1 to 12.

Table 13: CLK2-1..12_OUT_MUX Register

CLK2-1_OUT_MUX - Address 0x16								
CLK2-2_OUT_MUX - Address 0x17								
CLK2-3_OUT_MUX - Address 0x18								
CLK2-4_OUT_MUX - Address 0x19								
CLK2-5_OUT_MUX - Address 0x1a								
CLK2-6_OUT_MUX - Address 0x1b								
CLK2-7_OUT_MUX - Address 0x1c								
CLK2-8_OUT_MUX - Address 0x1d								
CLK2-9_OUT_MUX - Address 0x1e								
CLK2-10_OUT_MUX - Address 0x1f								
CLK2-11_OUT_MUX - Address 0x20								
CLK2-12_OUT_MUX - Address 0x21								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	CLK2-1..12_OUT_MUX							

11.3.7 CLK3-1 to 12 Output selection Multiplexer Register

The value of the Output selection Multiplexer Registers selects which source is connected to CLK3 of AMC slot 1 to 12.

Table 14: CLK3-1..12_OUT_MUX Register

CLK3-1_OUT_MUX - Address 0x22								
CLK3-2_OUT_MUX - Address 0x23								
CLK3-3_OUT_MUX - Address 0x24								
CLK3-4_OUT_MUX - Address 0x25								
CLK3-5_OUT_MUX - Address 0x26								
CLK3-6_OUT_MUX - Address 0x27								
CLK3-7_OUT_MUX - Address 0x28								
CLK3-8_OUT_MUX - Address 0x29								
CLK3-9_OUT_MUX - Address 0x2a								
CLK3-10_OUT_MUX - Address 0x2b								
CLK3-11_OUT_MUX - Address 0x2c								
CLK3-12_OUT_MUX - Address 0x2d								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	CLK3-1..12_OUT_MUX							

11.3.8 Update CLK1-Tx Output selection Multiplexer Register

The value of the Update CLK1-Tx Output selection Multiplexer Registers selects which source is connected to Update CLK1-Tx.

Table 15: CLK1-Tx _MUX Register

CLK1-Tx _MUX - Address 0x2e								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	CLK1-Tx_MUX							

11.3.9 Update CLK3-Tx Output selection Multiplexer Register

The value of the Update CLK3-Tx Output selection Multiplexer Registers selects which source is connected to Update CLK3-Tx.

Table 16: CLK3-Tx _MUX Register

CLK3-Tx _MUX - Address 0x2f								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	CLK3-Tx_MUX							

11.3.10 External Reference Clock 1..4 single ended Output selection Multiplexer Register

The value of the Clock 1..4 single ended Output selection Multiplexer Registers selects which source is connected to the single ended external reference clock at the face plate.

Table 17: Extref_single_1..4 _MUX Register

Extref_single_1 _MUX – Address 0x30								
Extref_single_2 _MUX – Address 0x31								
Extref_single_3 _MUX – Address 0x32								
Extref_single_4 _MUX – Address 0x33								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	Extref_single_1..4_MUX							

11.3.11 External Reference Clock 1..2 differential Output selection Multiplexer Register

The value of the Clock 1..2 single ended Output selection Multiplexer Registers selects which source is connected to the differential external reference clock at the face plate.

Table 18: Extref_single_1..3 _MUX Register

Extref_diff_1 _MUX – Address 0x34								
Extref_diff_2 _MUX – Address 0x35								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	Extref_diff_1..2_MUX							

11.3.12 Maxim PLL reference input IC1..4 selection Multiplexer Register

The value of the Maxim PLL reference input IC1..4 selection Multiplexer Registers selects which source is connected to the reference input IC1 to IC4 of the Maxim PLL.

Table 19: PLL_IC1..4_MUX Register

PLL_IC1_MUX - Address 0x36								
PLL_IC2_MUX - Address 0x37								
PLL_IC3_MUX - Address 0x38								
PLL_IC4_MUX - Address 0x39								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	PLL_IC1..4_MUX							

11.3.13 Maxim PLL Sync input 1..3 selection Multiplexer Register

The value of the Maxim PLL sync input 1..3 selection Multiplexer Registers selects which source is connected to the Sync input 1 to 3 of the Maxim PLL.

Table 20: PLL_SYNC1..3_MUX Register

PLL_SYNC1_MUX - Address 0x3a								
PLL_SYNC2_MUX - Address 0x3b								
PLL_SYNC3_MUX - Address 0x3c								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	PLL_Sync_1..3_MUX							

11.3.14 Synchronous Clock Input selection Multiplexer Register

To enable the clock signals for all AMCs in a complete system the multiplexer for each AMC need to be set up one after the other. That causes that the AMCs do not get their clocks enabled at the same time. If the system application requires enabling the clock to all AMCs at the same time the Synchronous Clock function can be used.

The synchronous clock function includes a Multiplexer with the same input as the other multiplexers. The difference is that the output of this multiplexer is connected to an enable gate instead of driving directly the output buffer. The output of that enable gate ("sync_clk") can then be chosen as an input for the clock output multiplexer (e.g. CLK1-1_OUT_MUX, CLK1-2_OUT_MUX, …).

With that solution the clock output multiplexer for all AMCs can be set up one after the other and when everything is ready configured the Sync_clk_en bit in the Sync_clk_en Register can be asserted.

The Synchronous Clock function is controlled by the Sync_clk_i_MUX Register together with the Sync_clk_en Register.

The value of the Synchronous Clock Input selection Multiplexer Registers selects which source is connected to the synchronous clock function. This multiplexer has the same input signals as all the other multiplexers, described in Table 12: .

Table 21: Sync_clk_i_MUX Register

Sync_clk_i_MUX - Address 0x3d								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	Sync_clk_i_MUX							

11.3.15 Synchronous Clock enable Register

The value of the Synchronous Clock enable Registers starts or stops the synchronous clock output. Refer to 11.3.14 for a description of the Synchronous clock function.

Table 22: Sync_clk_en Register

Sync_clk_en - Address 0x60								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	**Sync_clk_ en**

Table 23: Sync_clk_en - Register Bits

Bit	Name	Function
[0]	Sync_clk_en	**Enables the synchronous clock** If this bit is set the signal that is selected by the Sync_clk_i_MUX Register is glitch free enabled. If the bit is cleared again the signal is glitch free disabled and a "0" is driven out on the Sync clock.
[7..1]	-	**no function** write as 0 and ignore when read

11.3.16 Maxim PLL Feedback Register

The value of the Maxim PLL Feedback Registers shows the status of different feedback pins of the Maxim PLL.

Table 24: PLL_FB Register

PLL_FB - Address 0x61								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	-	-	-	-	-	**PLL_ INTREQ**	**PLL_ SRFAIL**	**PLL_ LOCK**

Table 25: PLL_FB - Register Bits

Bit	Name	Function
[0]	PLL_LOCK	**This bit shows the status of the LOCK pin of the PLL.** The PLL_LOCK bit is set to high when the T0 DPLL is in the lock state.
[1]	PLL_SRFAIL	**This bit shows the status of the SRFAIL pin of the PLL.** This bit is set to 1 when the selected reference to the DS3102 T0 DPLL fails, (i.e., no clock edges in two UI). SRFAIL is not set in free-run mode or holdover mode.
[2]	PLL_INTREQ	**This bit shows the status of the INTREQ pin of the PLL.** By default the function of that pin is disabled into the PLL.
[7..3]	-	**no function** write as 0 and ignore when read

11.3.17 External clock termination select Register

The value of the External clock termination select Registers chooses which termination is used for the external reference clock from the face plate.

Table 26: Ext_clk_term Register

Ext_clk_term - Address 0x62								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	**Extref_diff_sel**

Table 27: Ext_clk_term - Register Bits

Bit	Name	Function
[0]	Extref_diff_ sel	**Selects the termination for the extref lines** If this bit is set a differential termination is chosen and the clock is transmitted via the Extref_diff1..2 lines. If the bit is cleared a single ended termination is chosen and the clock is transmitted via the Extref_single1..4 lines.
[7..1]	-	**no function** write as 0 and ignore when read

11.3.18 HCSL Buffer Register

Register 0-8 of the HCSL Buffer are mirrored to the clock module registers 0x64 – 0x6C (100 – 108). Writes on these registers do directly affect the HCSL buffer register. Please refer to the manual [2] of the HCSL buffer for a register description. Table 28: shows a mapping between the buffer ports and the AMC slots.

Table 28: HCSL Buffer Port to AMC Slot Mapping

# AMC Slot CLK3	# HCSL Buffer Port
AMC1	0
AMC2	1
AMC3	2
AMC4	3
AMC5	4
AMC6	5
AMC7	11
AMC8	10
AMC9	9
AMC10	8
AMC11	7
AMC12	6

11.3.19 PCIe Reference Clock Generator Register

Register 0x00 – 0x0E of the PCIe reference clock generator are mirrored to the clock module registers 0x6E – 0x7C (110 – 124). Writes on these registers do directly affect the clock generator register. Please refer to the manual of the clock generator for a register description [3].

11.3.20 DS3102 PLL Register

Register 0x00 – 0x7F of the DS3102 PLL are mirrored to the clock module registers 0x80 – 0xFF. Writes on these registers do directly affect the PLL register. Please refer to the manual of the DS3102 PLL for a register description [1].

Known Bugs / Restrictions

[1] The M-LVDS Specification recommends a signal rise time of at least 1ns. The output of the used FPGA has a rise time of 0.3 ns.

Appendix A: Correlation between MicroTCA and AMC Clock Naming

The AMC.0 Rev.1.0 as well as the MicroTCA Rev.1.0 have defined three clock interfaces that can be used to for clock distribution purposes. These interfaces are named CLK1, CLK2 and CLK3. With the new AMC.0 V2.0 specification the clocks have been renamed as well as additional clocks were defined.

Which clock of an AMC is connected to which clock of the MCH depends on the connections that are made by the backplane. That means it must not necessarily be that TCLKA of an AMC is always connected to CLK1 of the MCH. Even though, this is the standard way for a non redundant MicroTCA Backplane.

Table 29: shows the correlation between the MicroTCA/AMC.0 Rev. 1.0 and the AMC.0 Rev. 2.0 naming.

Table 29: Correlation between MicroTCA and AMC Clock Naming

MicroTCA/ AMC.0 Rev. 1.0	AMC.0 Rev. 2.0	Description
CLK1	TCLKA	Telecom Clock A
CLK2	TCLKB	Telecom Clock B
CLK3	**FCLKA**	**Fabric Clock**
X	TCLKC	Telecom Clock C
X	TCLKD	Telecom Clock D

Please refer to the AMC.0 Rev. 2.0 specification for a more detailed description of the single clock signals and their intended purpose.

Since the MicroTCA specification defines the MCH this manual is using the names that are defined by the MicroTCA.

Appendix B: Reference Documentation

[1] Maxim DS3102 Stratum 2/3E/3 Timing Card IC, 05/09
http://datasheets.maxim-ic.com/en/ds/DS3102.pdf
[2] IDT ICS9DB1200CTwelve Output Differential Buffer for PCIe Gen1/Gen2, 09/08
http://www.idt.com/products/getDoc.cfm?docID=18459714
[3] IDT ICS9FG104 programmable FTG for differential P4™ CPU, PCIe Clocks, 02/07
http://timing.idt.com/datasheets/ics9FG104.pdf

Appendix C: Document's History

Revision	Date	Description	Author
0.9	03.08.2009	initial draft revision	ks
1.0	07.05.2010	- Added description of synchronous clock function - Added description of correlation between the MicroTCA and AMC.0 clock naming	ks
1.1	11.11.2010	- Moved detailed description of external reference clock transceiver modules to NAT-MCH Base Module reference manual.	ks