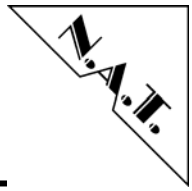
NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 2.1
Basic-PCB HW Revision 2.1



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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

Table of Contents

List of Figures

List of Tables

Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Introduction

The **NAT-MCH** consists of a **Basic-PCB**, which can be expanded with additional PCBs. The **Basic-PCB** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **Basic-PCB** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-PCB** and different **Hub-PCBs** are available. With the **Clock-PCB** the following functions can be enabled:

- generation and distribution of synchronised clock signals for up to 12 AMCs

Through the extension of the **NAT-MCH** with a **Hub-PCB**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **Hub-PCB** that fits best to their application. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
    - PCI Express
    - Serial Rapid IO
    - 10Gigabit Ethernet (XAUI)

The features of the individual extension PCBs are described in more detail in the corresponding Technical Reference Manuals.

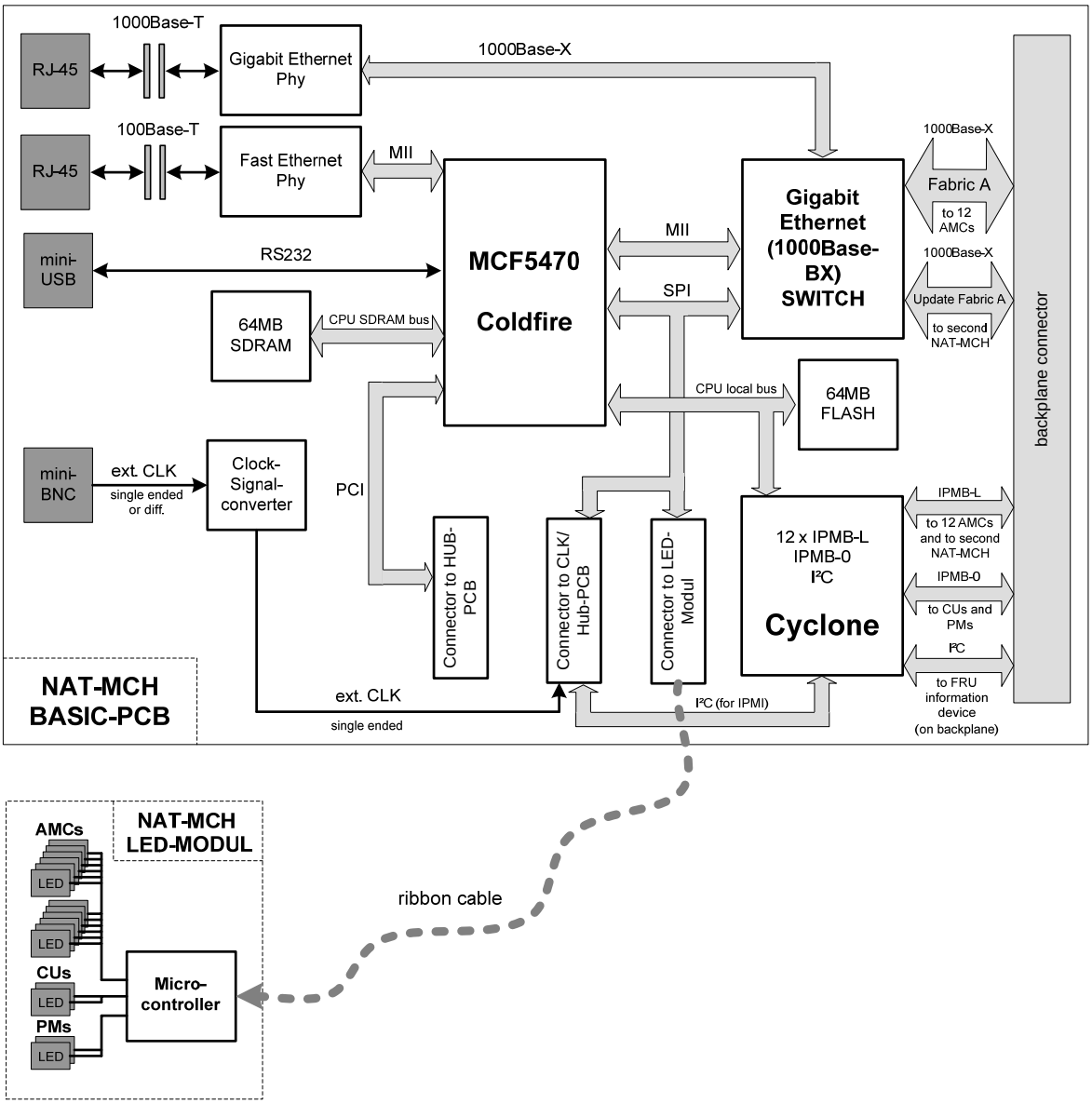
2 NAT-MCH Basics

The **NAT-MCH Basic-PCB** has the following major features implemented on-board:

- ColdFire MCF5470 32-bit CPU
- up to 64 MB main Memory (SDRAM)
- up to 64 MB FLASH
- real time clock
- serial debug port on faceplate
- 100BaseT Ethernet interface on front panel for:
  - communication with external Shelf or System Manager
  - software update
- 12 x IPMB-L interface for AMCs
- IPMB-L interface for a second **NAT-MCH**
- IPMB-0 interface for CUs and PMs
- I²C interface to FRU information device
- Gigabit Ethernet Hub function for fabric A
  - up to 12 AMCs
  - second MCH

  } 1000BaseX over Backplane
  - 1000BaseT channel on front panel
- interface for external clock signal (only usable with **CLK-PCB**)
- 12 bicolour LEDs for AMC status information
- 2 bicolour LEDs for CU status information
- 2 bicolour LEDs for PM status information

Figure 1: NAT-MCH Basic-PCB and LED Module Block Diagram



As it can be seen in 0, a LED-Module belongs to the **Basic-PCB** of the **NAT-MCH**, and is mounted on the front panel.

3 Board Features

- **CPU**

  The assembled 32-bit CPU ColdFire MCF5470 (Freescale) runs with a core clock frequency of 200 MHz.

- **Memory**

  SDRAM: The **NAT-MCH Basic-PCB** provides up to 64 MB SDRAM onboard. The SDRAM is 32 bit wide.

  FLASH PROM: The 16 bit wide Flash PROM provides a capacity of up to 64 MB.

- **Interfaces**

  IPMB: The **NAT-MCH Basic-PCB** implements IPMB interfaces which conform to the MicroTCA specification.
  IPMB-L interfaces are available for communication with up to 12 AMCs and a second **NAT-MCH**.
  An IPMB-0 interface is available for communication with CUs and PMs.

  I²C: The **NAT-MCH Basic-PCB** provides an I²C interface to access the dedicated FRU information device (resided on the backplane).

  Ethernet: The **NAT-MCH Basic-PCB** provides 1000BaseX interfaces for fabric A of 12 AMCs and the Update channel of fabric A. These interfaces are connected to a Broadcom BCM5396 Gigabit Ethernet Switch.

- **Front Panel I/O**

  Ethernet:
  - The 100 Mbit Ethernet interface supplied by the ColdFire (TSEC1) is connected to a 100BaseT interface through an Intel LXT972A physical layer device.
  - The 16th Gigabit Ethernet (1000BaseX) interface of the Broadcom switch is connected to a 1000BaseT interface through a Broadcom BCM5461 physical layer device (in GBIC mode).

  RS232: The front panel RS232 interface available on the **NAT-MCH Basic-PCB** is connected to the PSC0 UART of the ColdFire MCF5470.

- **Interface to Extension PCBs**

  CLK-PCB: - The **CLK-PCB** can be accessed by the ColdFire MCF5470 via an I²C bus.

  Hub-PCB: - the **Hub-PCB** is connected to the **Basic-PCB** over the same connector that connects the **CLK-PCB**. The **Hub-PCB** can also be accessed by the ColdFire via an I²C bus.

  - To interface the **Hub-PCB**, a SPI interface is also available. The SPI interface of the ColdFire is used for this purpose.

3.1 Board Specification

Table 2: NAT-MCH Basic-PCB Features

Processor	ColdFire MCF5470 (200 MHz)	
MCH-Module	standard MicroTCA MCH-Module, single width, double height	
Front-I/O	2 RJ45 connectors, 1 SMA and 1 Mini-USB connector	
Main Memory	32/64 MByte SDRAM	
Flash PROM	16/32/64 MByte Flash PROM, on board programmable	
Firmware	Linux	
Power consumption	12V 700mA typ. (only Basic-PCB)	
Environmental conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.2 Rev. 1.0	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	IPMI Specification V1.5 Rev. 1.0	
	PICMG µTCA.0 Rev. 1.0	

3.2 Installation

3.2.1 Safety Note

To ensure proper functioning of the **NAT-MCH Basic-PCB** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAT-MCH Basic-PCB** read this installation section
- Before installing or uninstalling the **NAT-MCH Basic-PCB**, read the Installation Guide and the User's Manual of the carrier board used, or of the MicroTCA system the board will be plugged into.
- Before installing or uninstalling the **NAT-MCH Basic-PCB** on a backplane:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAT-MCH Basic-PCB** is connected to the MicroTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

3.2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

3.2.2.1 Requirements

The installation requires only

- an µTCA backplane for connecting the **NAT-MCH Basic-PCB**
- power supply
- cooling devices

3.2.2.2 Power Supply

The power supply for the **NAT-MCH Basic-PCB** must meet the following specifications:

- required for the module:
  +12 V / 700mA typ. (only **Basic-PCB**)

3.2.2.3 Automatic Power Up

In the following situations the **NAT-MCH Basic-PCB** will automatically be reset and proceed with a normal power up.

Voltage sensor

The voltage sensor generates a reset

- when +12 V voltage level drops below 8 V

3.3 Statement on Environmental Protection

3.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that whereever and whenever possible RoHS components are used with N.A.T. hardware products already.

3.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly intergrated into larger and more complex envionments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

3.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

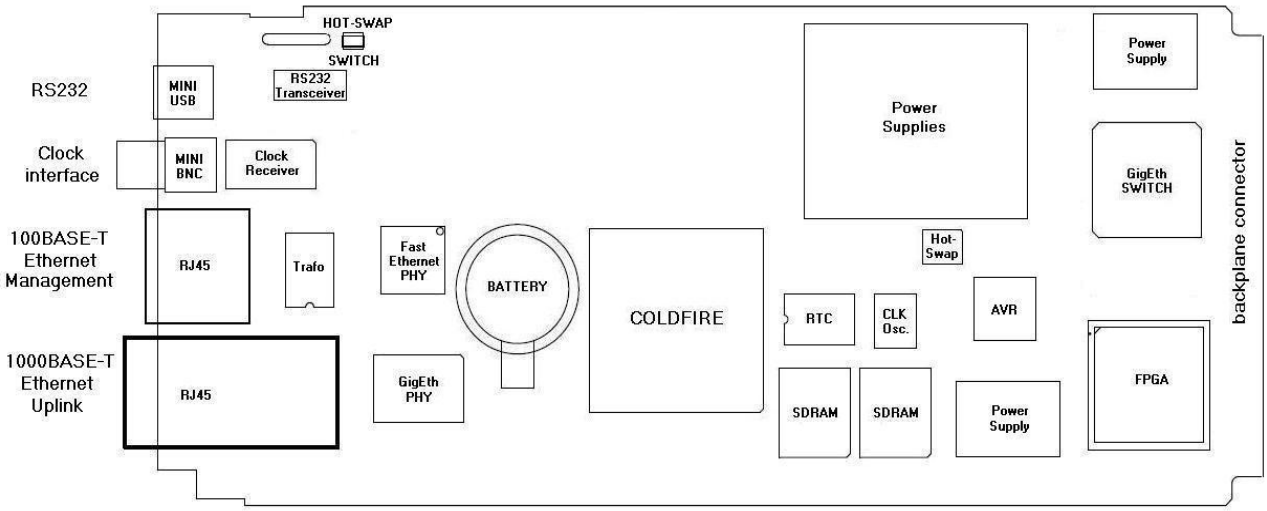
3.3.4 Product Safety

The board complies to EN60950 and UL1950.

4 Location Overview

Figure 3 "Location diagram of the **NAT-MCH Basic-PCB**" shows the position of important components. Depending on the board type it may be that the board does not include all components named in the location diagram.

Figure 2: Location Diagram of the NAT-MCH Basic-PCB (top-view)



5 Functional Blocks

The **NAT-MCH Basic-PCB** can be divided into a number of functional blocks, which are described in the following paragraphs.

5.1 Processor Core

The MCF5470 microprocessor is based on the V4e ColdFire core. The MCF5470 includes a memory management unit (MMU), a dual precision floating-point unit (FPU) and an enhanced multiply-accumulate unit (EMAC), delivering 308 (Drystone 2.1) MIPS at 200 MHz.
The processor has integrated a 32 KB I-Cache, a 32 KB D-Cache and 32 KB on-chip system SRAM. The MCF5470 is equipped with a 32-bit 133 MHz DDR/SDR-SDRAM Controller.

5.2 Processor – Integrated I/O

The MFC5470 ColdFire integrates the following interfaces:

- two 10/100 Ethernet Controllers (FECs)
- a 32-bit PCI interface
- DSPI – SPI with DMA capability
- a I²C interface
- a 16-channel DMA controller
- UART interfaces

5.3 Memory

5.3.1 SDRAM

The onboard SDRAM memory is 32 bit wide; its size is 32 or 64 MB (assembly option). The interface to the SDRAM is implemented in the ColdFire MCF5470. By programming several registers the SDRAM controller can be adapted to different RAM architectures.

5.3.2 FLASH

FLASH memory is connected to the demultiplexed upper 16 data bits D0 – 15 of the local bus and to the latched address lines. Its size is 16, 32, or 64 MB (assembly option).The FLASH on the **NAT-MCH Basic-PCB** can be programmed by the CPU (by appropriate software) or through the BDM port.

5.4 I²C Devices

There are three I²C Devices on the **NAT-MCH Basic PCB**, which are connected to the MCF5470 I²C bus; an EEPROM used for storage of board-specific information. A 24C08 device is used for this purpose; its address is 0x50.

Further more a LM75, which is located used to sense the board temperature is connected to that I²C bus, the address of the LM75 is 0x4A.

The third device is the real time clock with the address 0x68, described in more detail in the following chapter.

5.5 Real Time Clock

The DS1374 real time clock is a 32-bit binary counter designed to continuously count time in seconds. An additional counter generates a periodic alarm or serves as a watchdog timer. Separate outputs are provided for an interrupt and a square wave, both are connected to the FPGA.

The device is programmable through the I²C interface, for details refer to the DS1374 data sheet.

5.6 Ethernet Switch

The Broadcom BCM5396 Gigabit Ethernet Switch provides a layer 2, non-blocking, low-latency Gigabit Ethernet switch, supporting VPN as well as a port based rate control. The BCM5396 supports Fabric A switching according to MicroTCA.0 R1.0 and PICMG SFP.1 R1.0, serving up to 12 AMCs as well as the update channel from the second NAT-MCH in redundant environments. Also supported is an uplink port at the front panel of the NAT-MCH in order to interconnect to other carriers, shelves or systems. Refer to section 5.7.1 for the Uplink port.

The configuration register of the BMC5396 can be accessed through the MCF5470's PHY message channel interface.

For frame management the BMC5396 is connected to the MCF5470's TSEC0 through the MII interface.

5.7 Front Panel Interfaces

The **NAT-MCH Basic-PCB** is equipped with various interfaces, described in the following sections.

5.7.1 Ethernet Uplink Port

The 16th port of the BCM5396 Gigabit Ethernet Switch is wired to connector S2 via a Broadcom BCM5461 1000BaseT physical layer chip. By this external device the user may to access fabric A also from the front panel.

Configuration settings of the BCM5461 are done by CPU ports. Refer to Table 5: for the port pin mapping. The BCM5461 PHY has to be set up in GBIC mode (1000BaseT to 1000BaseX translation). Like all other I/O devices, the BCM5461 PHY is resetable by software by programming an FPGA register.

5.7.2 Ethernet Management Port

The Intel LXT972 Ethernet PHY is connected to the MCF5470's TSEC1 through the MII interface. It connects to the front panel connector S4. The line interface is 100BaseT.

Configuration settings of the LXT972 are done by CPU port pins. This applies to signals /MDINT, PAUSE, PWRDN, TxSLEW0, and TxSLEW1. The LXT972 PHY, like all other I/O devices, is resetable by software by programming an FPGA register.

5.7.3 RS232 Debug Port

The front panel RS232 interface available on the **NAT-MCH Basic-PCB** is connected to the PSC0 UART of the ColdFire MCF5470. It may be used for debug purposes.

5.7.4 Clock Interface

The SMA Connector S3 can be used as an input for an external reference clock, or as an output for a reference clock signal or it can be tri-stated. These functions are only available together with the **CLK-PCB**.

Connector S3 is connected to a receiver circuitry that accepts differential and single-ended input signals. The receiver transforms signals with low voltages (e.g. LVDS signals) as well as such with high voltages (e.g. 5V TTL) into a single ended 3.3V signal. For a more detailed specification refer to Table 3: . The output of that circuitry can be used by the **CLK-PCB** to synchronize clock signals to the AMCs. Whether the clock interface is used as an output, an

input, or is tri-stated, can be selected by programming a FPGA register. By default the interface is tri-stated.

Table 3: External Clock Receiver Circuit Specification

Parameter	Conditions	MIN	TYP	MAX	Units
Input Frequency	Duty Cycle: 40/60 or better	8		30 000	kHz
Input Voltage Peak to Peak	-	0.2		5	V
Input Impedance	-		50		Ohm

6 Hardware

6.1 Memory Map

All addresses are set up by programming the corresponding Chip-Select decoders of the ColdFire processor.

Table 4: Memory Map

Device	CS Line	Address	Function	Notes
FLASH	FBCS0	programmable	Boot, user code	16 bit wide
Registers	FBCS1	programmable	FPGA registers	32 bit wide
not used	FBCS2 - FBCS5	not used		FBCS2 used as I/O
SDRAM	MCS0	programmable	SDRAM	32 bit wide
not used	MCS1 - MCS3	not used		

FBCSx refers to the FlexBus, MCSx refers to the SDRAM controller.

6.2 Definition of MCF5470 ColdFire

Many MCF5470 port pins are used to set up some board configuration. In detail:

Table 5: MCF5470 ColdFire Port Pin Usage

MCF5470 ColdFire Signal Function	MCF5470 ColdFire Port Pin	used as	Description	used at Device
FBCS5-2	PFBCS5-2	not used	FlexBus CS	none
FBCS1	PFBCS1	FBCS1	FlexBus CS	FPGA
ALE	PFBCTL0	ALE	FlexBus ALE	FPGA, FLASH
TA	PFBCTL1	TA	FlexBus TA	none
R/W	PFBCTL2	R/W	FlexBus R/W	FPGA, FLASH
OE	PFBCTL3	OE	FlexBus OE	FPGA, FLASH
BWE3-0	PFBCTL7	not used	FlexBus R/W	none
PCIBG4	PPCIBG4	PPCIBG4	TxSL1	LXT972 PHY
PCIBG3	PPCIBG3	PPCIBG3	TxSL0	LXT972 PHY
PCIBG2	PPCIBG2	PPCIBG2	QUAL	BCM5461 PHY
PCIBG1	PPCIBG1	not used	not used	none
PCIBG0	PPCIBG0	PCIBG0	not used	none
PCIBR4	PPCIBR4	PPCIBR4	PAUSE	LXT972 PHY
PCIBR3	PPCIBR3	PPCIBR3	PWRDN	LXT972 PHY
PCIBR2	PPCIBR2	PPCIBR2	Reset Hub-PCB	AVR Controller Hub-PCB (CON2)
PCIBR1	PPCIBR1	PPCIBR1	Reset Clock-PCB	AVR Controller Clk-PCB (CON2)
PCIBR0	PPCIBR0	PCIBR0	not used	none
PCS0TXD	PPSC1PSC00	PCS0TXD	UART TXD	RS232 driver
PCS0RXD	PPSC1PSC01	PCS0RXD	UART RXD	RS232 driver
PCS0CTS	PPSC1PSC03	PCS0CTS	UART CTS	RS232 driver
PCS0RTS	PPSC1PSC02	PCS0RTS	UART RTS	RS232 driver
PCS1TXD	PPSC1PSC04	PPSC1PSC04	AUTO_POLL_DIS	BCM5396 Switch
PCS1RXD	PPSC1PSC05	PPSC1PSC05	MEM_CLK_FREQ0	BCM5396 Switch
PCS1CTS	PPSC1PSC07	PPSC1PSC07	MEM_CLK_FREQ1	BCM5396 Switch
PCS1RTS	PPSC1PSC06	PPSC1PSC06	ENFDXFLOW	BCM5396 Switch
PCS2TXD	PPSC1PSC20	PPSC1PSC20	ENHDXFLOW	BCM5396 Switch
PCS2RXD	PPSC1PSC21	PPSC1PSC21	EEPROM_EXT0	BCM5396 Switch
PCS2CTS	PPSC1PSC23	PPSC1PSC23	EEPROM_EXT1	BCM5396 Switch
PCS2RTS	PPSC1PSC22	PPSC1PSC22	HW_FWDG_EN	BCM5396 Switch

MCF5470 ColdFire Signal Function	MCF5470 ColdFire Port Pin	used as	Description	used at Device
PCS3TXD	PPSC1PSC24	PPSC1PSC24	QoS_EN	BCM5396 Switch
PCS3RXD	PPSC1PSC25	PPSC1PSC25	QoS_FC_OFF	BCM5396 Switch
PCS3CTS	PPSC1PSC27	PPSC1PSC27	RXC_DELAY	BCM5396 Switch
PCS3RTS	PPSC1PSC26	PPSC1PSC26	TXC_DELAY	BCM5396 Switch
DSPISOUT	PDSPI0	DSPISOUT	SPI MOSI	all SPI devices
DSPISIN	PDSPI1	DSPISIN	SPI MISO	all SPI devices
DSPISCK	PDSPI2	DSPISCK	SPI Clock	all SPI devices
DSPICS5	PDSPI6	DSPICS5	SPI Select	AVR Controller Basic-PCB
DSPICS3	PDSPI5	DSPICS3	SPI Select/Reset Clock-PCB	AVR Controller Clk-PCB (CON2)
DSPICS2	PDSPI4	DSPICS2	SPI Select	AVR Controller Hub-PCB (CON2)
DSPICS0	PDSPI3	DSPICS0	SPI Select	AVR Controller LED-PCB (JP2)
E0MDIO	PFECI2C3	E0MDIO	ETH CH. 0 MII	BCM5396 Switch
E0MDC	PFECI2C2	E0MDC	ETH CH. 0 MII	BCM5396 Switch
E0TXCLK	PFEC0H7	E0TXCLK	ETH CH. 0 MII	BCM5396 Switch
E0TXEN	PFEC0H6	E0TXEN	ETH CH. 0 MII	BCM5396 Switch
E0TXD0	PFEC0H5	E0TXD0	ETH CH. 0 MII	BCM5396 Switch
E0COL	PFEC0H4	E0COL	ETH CH. 0 MII	BCM5396 Switch
E0RXCLK	PFEC0H3	E0RXCLK	ETH CH. 0 MII	BCM5396 Switch
E0RXDV	PFEC0H2	E0RXDV	ETH CH. 0 MII	BCM5396 Switch
E0RXD0	PFEC0H1	E0RXD0	ETH CH. 0 MII	BCM5396 Switch
E0CRS	PFEC0H0	E0CRS	ETH CH. 0 MII	BCM5396 Switch
E0TXD3	PFEC0L7	E0TXD3	ETH CH. 0 MII	BCM5396 Switch
E0TXD2	PFEC0L6	E0TXD2	ETH CH. 0 MII	BCM5396 Switch
E0TXD1	PFEC0L5	E0TXD1	ETH CH. 0 MII	BCM5396 Switch
E0TXER	PFEC0L4	E0TXER	ETH CH. 0 MII	BCM5396 Switch
E0RXD3	PFEC0L3	E0RXD3	ETH CH. 0 MII	BCM5396 Switch
E0RXD2	PFEC0L2	E0RXD2	ETH CH. 0 MII	BCM5396 Switch
E0RXD1	PFEC0L1	E0RXD1	ETH CH. 0 MII	BCM5396 Switch
E0RXER	PFEC0L0	E0RXER	ETH CH. 0 MII	BCM5396 Switch
E1MDIO	None	E1MDIO	ETH CH. 1 MII	LXT972 PHY
E1MDC	None	E1MDC	ETH CH. 1 MII	LXT972 PHY
E1TXCLK	PFEC1H7	E1TXCLK	ETH CH. 1 MII	LXT972 PHY
E1TXEN	PFEC1H6	E1TXEN	ETH CH. 1 MII	LXT972 PHY
E1TXD0	PFEC1H5	E1TXD0	ETH CH. 1 MII	LXT972 PHY
E1COL	PFEC1H4	E1COL	ETH CH. 1 MII	LXT972 PHY

MCF5470 ColdFire Signal Function	MCF5470 ColdFire Port Pin	used as	Description	used at Device
E1RXCLK	PFEC1H3	E1RXCLK	ETH CH. 1 MII	LXT972 PHY
E1RXDV	PFEC1H2	E1RXDV	ETH CH. 1 MII	LXT972 PHY
E1RXD0	PFEC1H1	E1RXD0	ETH CH. 1 MII	LXT972 PHY
E1CRS	PFEC1H0	E1CRS	ETH CH. 1 MII	LXT972 PHY
E1TXD3	PFEC1L7	E1TXD3	ETH CH. 1 MII	LXT972 PHY
E1TXD2	PFEC1L6	E1TXD2	ETH CH. 1 MII	LXT972 PHY
E1TXD1	PFEC1L5	E1TXD1	ETH CH. 1 MII	LXT972 PHY
E1TXER	PFEC1L4	E1TXER	ETH CH. 1 MII	LXT972 PHY
E1RXD3	PFEC1L3	E1RXD3	ETH CH. 1 MII	LXT972 PHY
E1RXD2	PFEC1L2	E1RXD2	ETH CH. 1 MII	LXT972 PHY
E1RXD1	PFEC1L1	E1RXD1	ETH CH. 1 MII	LXT972 PHY
E1RXER	PFEC1L0	E1RXER	ETH CH. 1 MII	LXT972 PHY
SDA	PFECI2C1	SDA	I^2C data	all I^2C devices
SCL	PFECI2C0	SCL	I^2C clock	all I^2C devices
IRQ7	PIRQ7	not used	IRQ7	none
IRQ6	PIRQ6	not used	IRQ6	none
IRQ5	PIRQ5	IRQ5	INT_FPGA	all FPGA sources
DACK1	PDMA3	PDMA3	GFDX	BCM5461 PHY
DACK0	PDMA2	PDMA2	GF1000	BCM5461 PHY
DREQ1	PDMA1	PDMA1	GANEN	BCM5461 PHY
DREQ0	PDMA0	PDMA0	GSPD0	BCM5461 PHY
TIN3/IRQ3	PTIM7	IRQ3	GINTR	BCM5461 PHY
TIN2/IRQ2	PTIM5	IRQ2	MII_MDINT	LXT972 PHY

6.3 Interrupt Structure

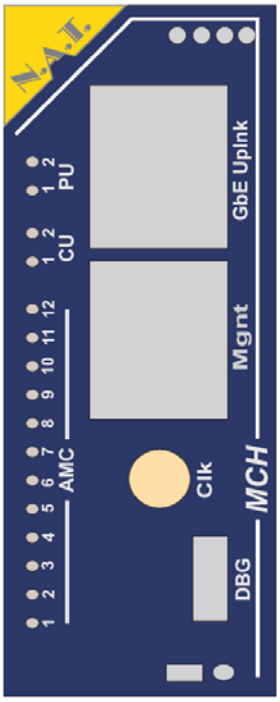
The **NMCH** has the following interrupt structure:

Table 6: Interrupt Structure

Interrupt Source	MCF5470 ColdFire Interrupt Level
NC	IRQ-Level 7 (highest level)
Router PCB (PCB 4)	IRQ-Level 6
FPGA (from various sources, e.g. Clock PCB (PCB 2)	IRQ-Level 5
NC	IRQ-Level 4 (used as I/O port pin)
BCM5461 PHY	IRQ-Level 3
LXT972 PHY	IRQ-Level 2
NC	IRQ-Level 1 (lowest level, used as I/O port pin)

6.4 Front Panel and LEDs

The **NAT-MCH Basic-PCB** module is equipped with 4 LEDs, which are integrated in the RJ45 connectors. Furthermore, there are LEDs residing on the front panel (mounted on the LED-Module), in order to indicate the status of 12 AMCs, 2 CUs, and 2 PMs. All these LEDs are completely software programmable.



Connectors:

GbE Uplnk — The RJ45 connector S2 connects a 1000BaseT Ethernet network (over a PHY chip) to the Gigabit Ethernet switch. The switch connects the network to fabric A.

Mgnt — The RJ45 connector S4 connects an 100BaseT Ethernet network to the ColdFire. This port can be used to update the ColdFire Software, and to permit communication with external shelf or system mangers.

Clk — the SMA connector S3 connects over a transformation circuit to the EXTREF_IN or EXTREF_OUT pin of the interface connector to the **CLK-PCB**.

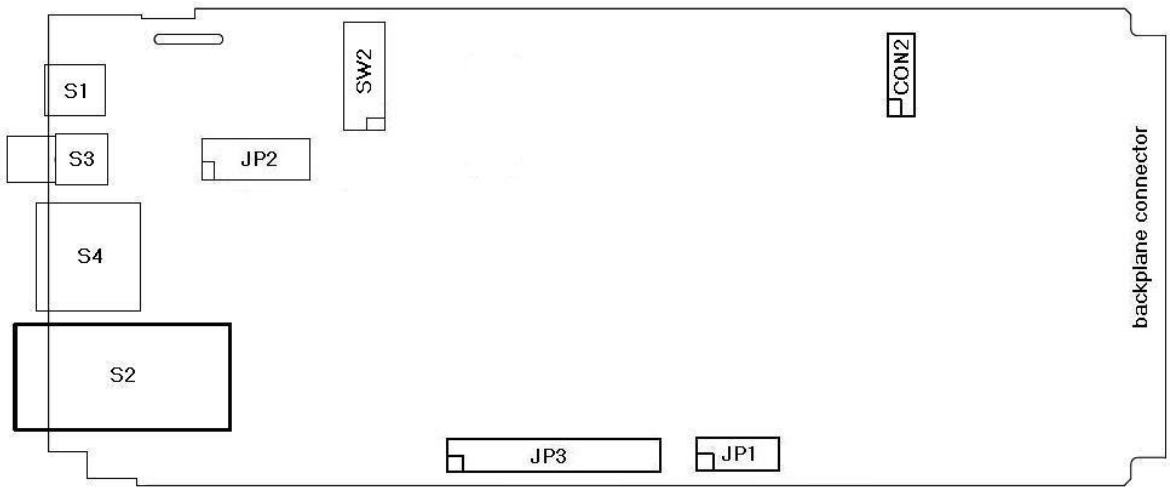
DBG — The Mini USB connector S1 connects to an RS232 debug interface of the ColdFire.

Please refer to Chapter 6.5.9 for details on front panel connectors.

6.5 Connectors

6.5.1 Connector Overview

Figure 3: Connectors of the NAT-MCH Basic-PCB



Please refer to the following tables to look up the pin assignment of the **NAT-MCH Basic-PCB**.

6.5.2 MCH Connector CON1

Table 7: MCH Edge Connector CON1

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	PWR_ON	170
2	PWR	NC	169
3	/PS1	NC	168
4	MP	NC	167
5	GA0	NC	166
6	RESVD	NC	165
7	GND	GND	164
8	RESVD	TxFA-1+	163
9	PWR	TxFA-1-	162
10	GND	GND	161
11	TxFUA+	RxFA-1+	160
12	TxFUA-	RxFA-1-	159
13	GND	GND	158
14	RxFUA+	TxFA-2+	157
15	RxFUA-	TxFA-2-	156
16	GND	GND	155
17	GA1	RxFA-2+	154
18	PWR	RxFA-2-	153
19	GND	GND	152
20	TxFA-3+	TxFA-4+	151
21	TxFA-3-	TxFA-4-	150
22	GND	GND	149
23	RxFA-3+	RxFA-4+	148
24	RxFA-3-	RxFA-4-	147
25	GND	GND	146
26	GA2	TxFA-6+	145
27	PWR	TxFA-6-	144
28	GND	GND	143
29	TxFA-5+	RxFA-6+	142
30	TxFA-5-	RxFA-6-	141
31	GND	GND	140
32	RxFA-5+	TxFA-8+	139
33	RxFA-5-	TxFA-8-	138
34	GND	GND	137
35	TxFA-7+	RxFA-8+	136
36	TxFA-7-	RxFA-8-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	RxFA-7+	/TMREQ	133
39	RxFA-7-	RSVD	132
40	GND	GND	131
41	/ENABLE	I2C_SCL	130
42	PWR	I2C_SDA	129
43	GND	GND	128
44	TxFA-9+	IPMB0-SCL-A	127
45	TxFA-9-	IPMB0-SDA-A	126
46	GND	GND	125
47	RxFA-9+	IPMB0-SCL-B	124
48	RxFA-9-	IPMB0-SDA-B	123
49	GND	GND	122
50	TxFA-10+	IPMBL-SCL-1	121
51	TxFA-10-	IPMBL-SDA-1	120
52	GND	GND	119
53	RxFA-10+	IPMBL-SCL-2	118
54	RxFA-10-	IPMBL-SDA-2	117
55	GND	GND	116
56	SCL_L	IPMBL-SCL-3	115
57	PWR	IPMBL-SDA-3	114
58	GND	GND	113
59	TxFA-11+	IPMBL-SCL-4	112
60	TxFA-11-	IPMBL-SDA-4	111
61	GND	GND	110
62	RxFA-11+	IPMBL-SCL-5	109
63	RxFA-11-	IPMBL-SDA-5	108
64	GND	GND	107
65	TxFA-12+	IPMBL-SCL-6	106
66	TxFA-12-	IPMBL-SDA-6	105
67	GND	GND	104
68	RxFA-12+	IPMBL-SCL-7	103
69	RxFA-12-	IPMBL-SDA-7	102
70	GND	GND	101
71	SDA_L	IPMBL-SCL-8	100
72	PWR	IPMBL-SDA-8	99
73	GND	GND	98
74	XOVER0+	IPMBL-SCL-9	97
75	XOVER0-	IPMBL-SDA-9	96
76	GND	GND	95
77	XOVER1+	IPMBL-SCL-10	94
78	XOVER1-	IPMBL-SDA-10	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	XOVER2+	IPMBL-SCL-11	91
81	XOVER2-	IPMBL-SDA-11	90
82	GND	GND	89
83	/PS0	IPMBL-SCL-12	88
84	PWR	IPMBL-SDA-12	87
85	GND	GND	86

6.5.3 Connector CON2: Interface to CLK-PCB

Connector CON2 connects the **NAT-MCH Basic-PCB** with the **CLK-PCB** and/or the **HUB-PCB**.

Table 8: Connector CON2 to CLK/HUB-PCB

Pin No.	Signal	Signal	Pin No.
1	+12V	+12V	2
3	+12V	+12V	4
5	EXTREF_OUT_P	+3.3V MP	6
7	EXTREF_OUT_N	SPICLK	8
9	GND	EXTREF_IN	10
11	MOSI	MISO	12
13	GND	/SPISEL_Hub-PCB	14
15	SCL	/Reset_Clk-PCB	16
17	SDA	/Reset_Hub-PCB	18
19	GND	GND	20

The I^2C- and SPI- interfaces of Connector CON2 are connected to the respective interfaces of the local Coldfire CPU.

6.5.4 Connector JP1: Altera FPGA Programming Port

Connector JP1 connects the JTAG- or programming-port of the Altera FPGA device.

Table 9: Connector JP1: Altera FPGA Programming Port

Pin No.	Signal	Signal	Pin No.
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATAO	/CSO	8
9	ASDI	GND	10

6.5.5 Connector JP2: Interface to the Led Module

Connector JP2 connects the LED-MODULE via a ribbon cable

Table 10: LED-MODULE Interface

Pin No.	Signal	Signal	Pin No.
1	nRESET_LED	+3.3V	2
3	nSPISEL_LED	+3.3V	4
5	MOSI	NC	6
7	MISO	NC	8
9	SPICLK	NC	10
11	NC	NC	12
13	NC	NC	14
15	NC	GND	16
17	NC	GND	18
19	NC	GND	20

6.5.6 Connector JP3: BDM and JTAG connector

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 11: Development Port / BDM Connector Pinout

Pin No.	Signal	Signal	Pin No.
1	NC	/BKPT	2
3	GND	/DSCLK	4
5	GND	TCK	6
7	/HRESET	DSI	8
9	+3.3V	DSO	10
11	GND	PST_D7	12
13	PST_D6	PST_D5	14
15	PST_D4	PST_D3	16
17	PST_D2	PST_D1	18
19	PST_D0	GND	20
21	NC	NC	22
23	GND	PST_CLK	24
25	NC	/TA	26

6.5.7 Hot Swap Switch SW1

Switch SW1 is used to support hot swapping of the module. It conforms to the PICMG AMC.0 specification.

6.5.8 General Purpose DIL Switch SW2

Switch SW2 is used for general purpose settings. It is an octal DIL switch and was implemented for future use. SW2 is connected to the FPGA, by which its status can be read.

6.5.9 The Front Panel Connectors

6.5.9.1 The RS232 Connector S1

Table 12: shows the pin assignment of the signals of the RS232 interface, which is wired to the Mini-USB connector S1.

Table 12: Pin Assignment of the Front-panel Connector S1 (RS232)

Pin No.	Signal	Signal	Pin No.
1	PSC0 RTS	PSC0 RXD	2
3	PSC0 TXD	PSC0 CTS	4
5	GND		

Front panel connector S1 is connected to PSC0 of the MCF5470 UART.

6.5.9.2 The Ethernet Connector S2

Table 13: shows the pin assignment of RJ45 connector S2. This connector carries the 1000BaseT signals of the Ethernet interface of the Gigabit Ethernet Switch.

Table 13: Pin Assignment of the Front-panel Connector S2 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	MDI0+	MDI0-	2
3	MDI1+	MDI2+	4
5	MDI2-	MDI1-	6
7	MDI3+	MDI3-	8

6.5.9.3 The Clock Connector S3

Table 14: shows the pin assignment of the signals of the external reference clock interface.

Table 14: Pin Assignment of the Clock Connector S3

Pin No.	Signal	Signal	Pin No.
Center	EXTREF_P	EXTREF_N	Shield

6.5.9.4 The Ethernet Connector S4

Table 15: shows the pin assignment of RJ45 connector S4. This connector carries the 100BaseT signals of the Ethernet interface of the ColdFire. Termination is the 100BaseT termination used for pins 4, 5, 7, and 8.

Table 15: Pin Assignment of the Front-panel Connector S4 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	TX+	TX-	2
3	RX+	Term.	4
5	Term.	RX-	6
7	Term.	Term.	8

7 NAT-MCH Basic-PCB Programming Notes

7.1 Setup of the Serial Interfaces

7.1.1 RS232 Interface on the Front Panel Connector S1

The programming of the RS232 serial interface is performed through UART PSC0.

7.1.2 I^2C Interfaces

The I^2C interface of the MCF5470 CPU connects to an EEPROM of 8 kBit size. The address of this EEPROM used for storage of board-specific parameters is 0x0. The control code (1st 4 bits of the 7 bit address) for the 24C08 EEPROM is 1010b, which results in address 0x50 for the parameter EEPROM.

Note:

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further assistance on programming **NAT-MCH BASIC-PCB** devices.

7.2 Programming the FPGA Interface

7.2.1 PCB Revision Register

Note:

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further assistance on revision register of the **NAT-MCH BASIC-PCB**.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Freescale, MCF5470 ColdFire® CF4e Core Users Manual, 06/2001, Rev. 0
[2] Altera, Cyclone Device Handbook, 02/2005
[3] Micron, MT48LC8M32B2 SDRAM Data Sheet, Rev. B, 10/2004
[4] Intel®, LXT972A Single-Port 10/100 Mbps PHY Transceiver, 10/2005
[5] Broadcom, BCM5461S 10/100/1000Base-T Gigabit Ethernet Transceiver, 12/2005
[6] Maxim, DS1374 RTC, Rev. 3 01/2006
[9] Traco Power DC/DC Converters, TOS Series, POL Converter, Rev. 10/2005

Appendix B: Document's History

Revision	Date	Description	Author
1.0	08.12.2006	initial revision	ks, ga
1.1	16.01.2007	reworked, adapted to HW Rev. 1.1	ga
1.2	20.03.2007	Reworked, adapted to CLK-PCB Rev. 1.2 and HUB-PCB Rev. 1.1	ks
2.0	04.05.2007	adapted to Basic-PCB Rev. 2.0, description reduced to Basic-PCB	ga
2.1	12.08.2008	Added specification of the external clock input circuit	ks