NAMC-QorIQ-P3x
NAMC-QorIQ-P4x
NAMC-QorIQ-P5x
CPU AMC Module
Technical Reference Manual V1.3
HW Revision 1.2

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
BDM	Background Debug Mode
COM	Communication Port
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
ECC	Error Correcting Code
EEPROM	Electrically Erasable PROM
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
H.110	Timeslot Interchange Bus
I²C	Inter-Integrated Circuit
ID	Identifier
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
Ipsec	Internet Protocol Security
iTDM	Internal TDM
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
µTCA/MTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MUX	Multiplexer
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PLL	Phase Locked Loop
PHY	Physical Layer Device
(P)ROM	(Programmable) Read Only Memory
PTP	Precision Time Protocol
RAM	Random Access Memory
RCW	Reset Configuration Word
RGMII	Reduced Gigabit Media Independent Interface
RNC	Radio Network Controller
RTC	Real Time Clock
RTP	Real Time Protocol
SATA	Serial Advanced Technology Attachment
SGMII	Serial Gigabit Media Independent Interface
SerDes	Serializer/Deserializer

Abbreviation	Description
SFP	Small Form-Factor Pluggable
SRIO	Serial Rapid I/O
SPI (FLASH)	Serial Peripheral Interface (FLASH)
TCKL	Telecom Clock
TDM	Time Division Multiplex
UART	Universal Asynchronous Receiver/Transmitter
U-Boot	Universal Bootloader
USB	Universal Serial Bus
VoIP	Voice over IP
WAN	Wide Area Network
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

The **NAMC-QorIQ-Pxxx** is a packet processing engine in AMC (Advanced Mezzanine Card) form factor based on a Freescale's QorIQ communications processor, designed for packet oriented telecom applications such as LTE or VoIP.

Please note:
The board can be equipped with several QorIQ-CPUs, such as a P4080, P5020 or P3041 processor. For reasons of simplification this manual refers to the notation **NAMC-QorIQ-Pxxx** if common functionality of all CPU types is described. If the behaviour differs on the variants, differences are described for each CPU type separately. For detailed information refer to Table 2:

All of these CPUs provide security and pattern match engines, sophisticated buffer and queue management and additionally various high-speed serial data links. Thus, the board is ideally suited for applications in ATCA and MTCA environments.
The QorIQ processors are designed for combined control and dataplane processing enabling high-performance Layer 2-7 processing.

The CPU is accompanied by a set of supporting hardware blocks for time keeping/tracking as well as for external protocol processing/conversion and acceleration.
The powerful QorIQ processor in combination with the Lattice ECP3-FPGA architecture results in an unrivalled power engine for data and packet processing as well as protocol acceleration.
The board can be equipped with an on-board Real Time Clock and precision oscillator to support time keeping and time tracking for protocols like RTP (Real Time Protocol) or PTP (Precision Time Protocol, IEEE 1588).
The low jitter PLL allows telecom clocks to be derived from onboard sources and to be provided to the system by the MTCA clock distribution network.

As an option, each of the PowerPC cores features its own load indicator LED at the front panel. The load indicators provide a visual feed-back of the current load balancing between the individual CPU cores.

Due to the unique combination of the powerful and feature-rich packet processor and the FPGA, the **NAMC-QorIQ-Pxxx** is ideally suited to any voice/data application with requirements like deep packet inspection, encryption, protocol conversion or Layer 2-7 routing. The **NAMC-QorIQ-Pxxx** is the optimal choice for applications like multi-service switches, edge routers, radio network controllers (RNCs), VoIP/VoP gateways and routers as well as mobile network equipment.

2 Overview

2.1 Major Features

- CPU - Freescale QorIQ P4080
  - Packet processor featuring 8x e500mc PowerPC Cores @ 1.5 GHz
  - 18x SerDes – 2x XAUI, 3x PCIe, 2x SRIO, 8x SGMII
  - Dual 64 bit Memory Interfaces
- CPU – Freescale QorIQ P5020
  - Packet processor featuring 2x e5500 PowerPC Cores @ 2 GHz
  - 18x SerDes – 1x XAUI, 3x PCIe, 2x SRIO, 8x SGMII, 2x SATA
  - Dual 64 bit Memory Interfaces
- CPU – Freescale QorIQ P3041
  - Packet processor featuring 4x e500mc PowerPC Cores @ 1.5 GHz
  - 18x SerDes – 1x XAUI, 3x PCIe, 2x SRIO, 8x SGMII, 2x SATA
  - Single 64 bit Memory Interfaces
- All Freescale QorIQ CPUs feature:
  - Security Engine
  - Pattern Match Engine
  - Queue and Buffer Managers
- FPGA from Lattice ECP3 family
- 2x 1 GB or 2x 2 GB 64 bit DDR3 DRAM
- 2x 1 GB NAND Flash memory
- 1x 128 MB NOR Flash memory
- Backplane interfaces:
  - XAUI, SRIO and PCIe to AMC fat pipe region
  - 2x Gigabit Ethernet to AMC Ports 0/1
  - 2x SATA to AMC Ports 2/3 (P3041, P5020)
- Front Panel interfaces:
  - XAUI via SFP+ (P4080)
  - Gigabit Ethernet
  - USB
  - RS232

For detailed description see the following chapter.

2.2 Block Diagram

The following figures show block diagrams of the different **NAMC-QorIQ-Pxxx** variants. The blocks framed with dashed lines show parts which are – deviating from standard – available as assembly option.

Figure 1: NAMC-QorIQ-P3041 – Block Diagram – Overview

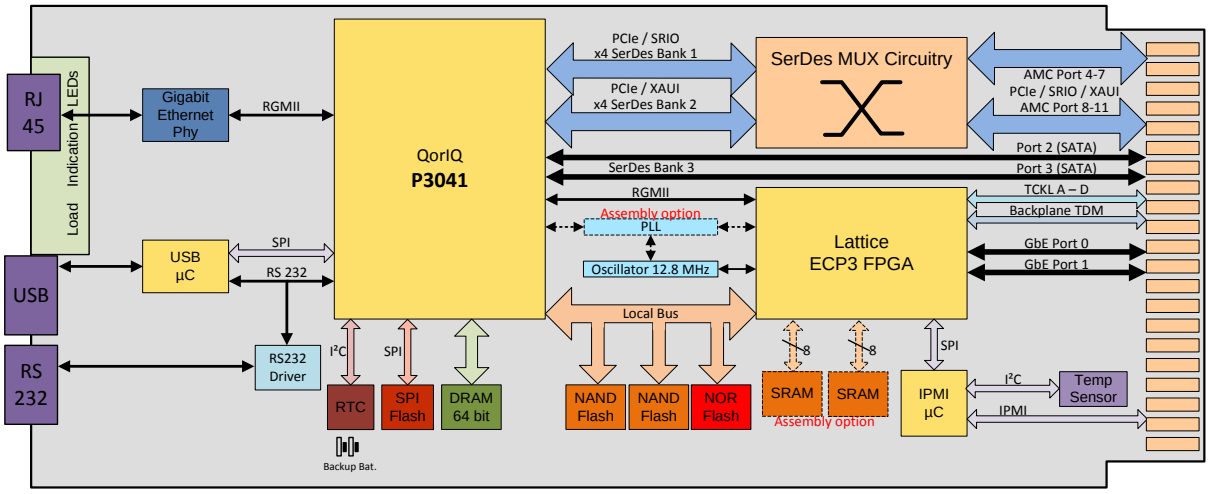


Figure 2: NAMC-QorIQ-P4080 – Block Diagram – Overview

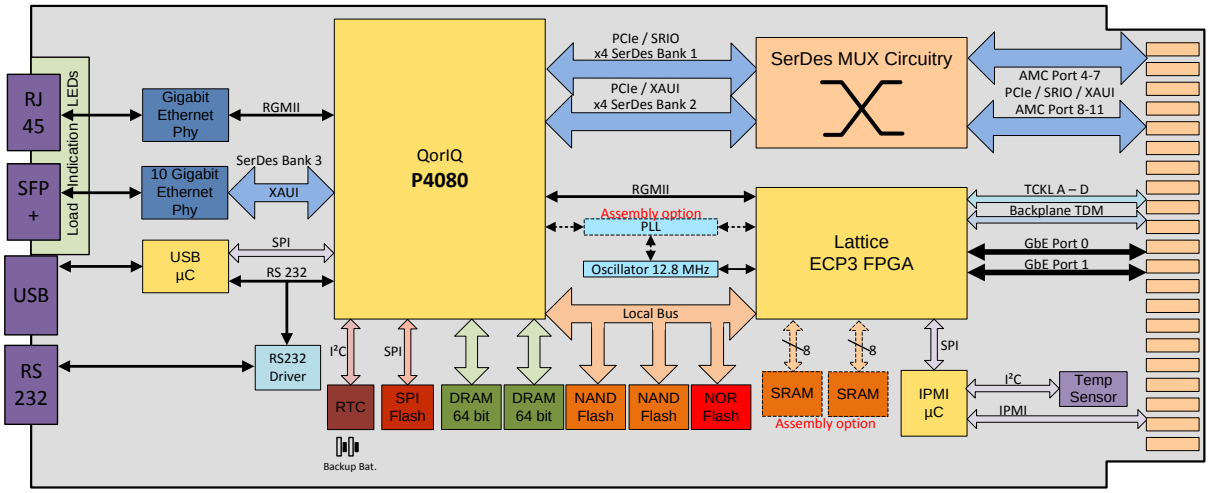


Figure 3: NAMC-QorIQ-P4080-ECO – Location Diagram – Overview

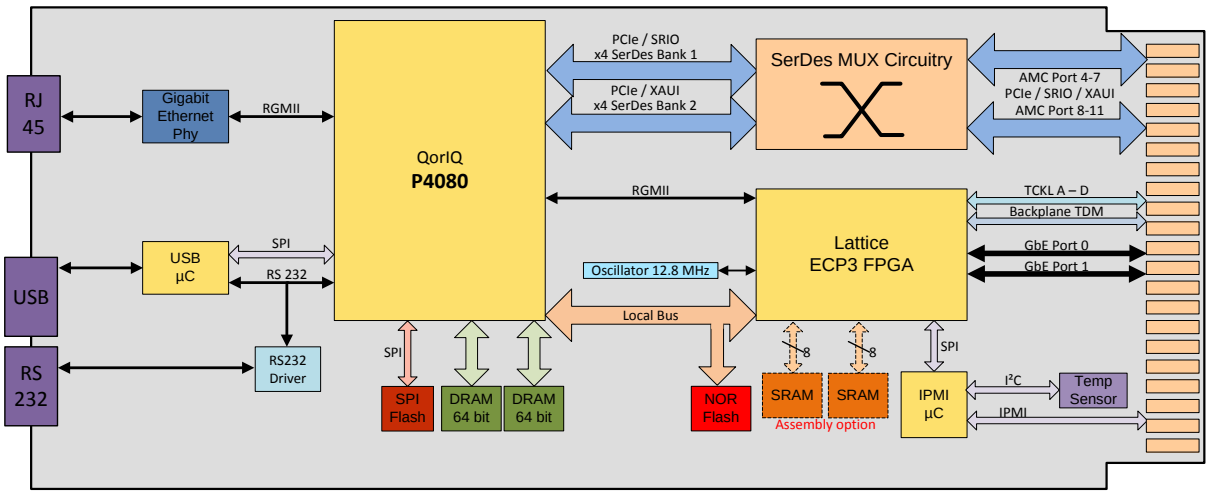
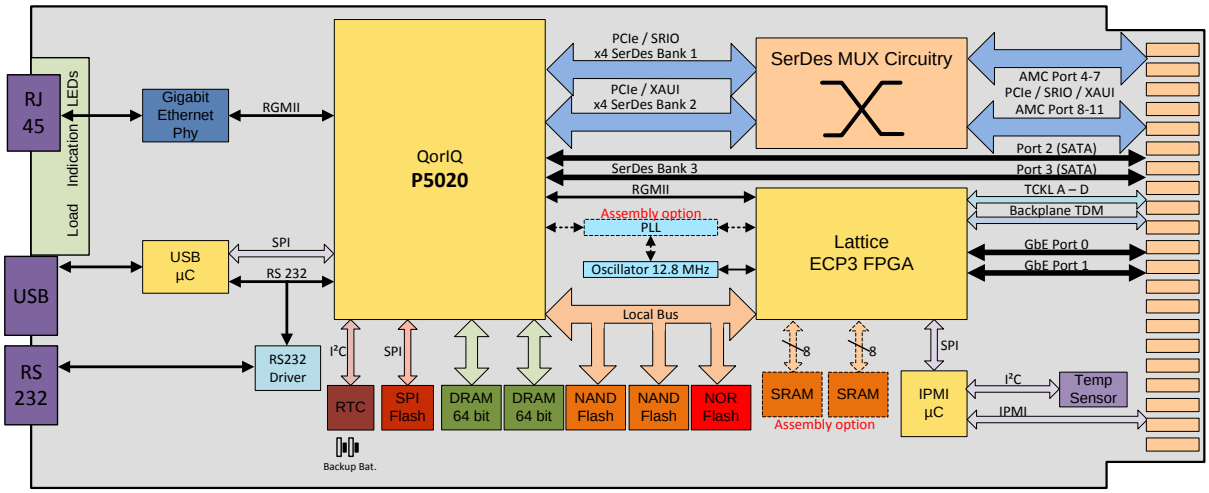


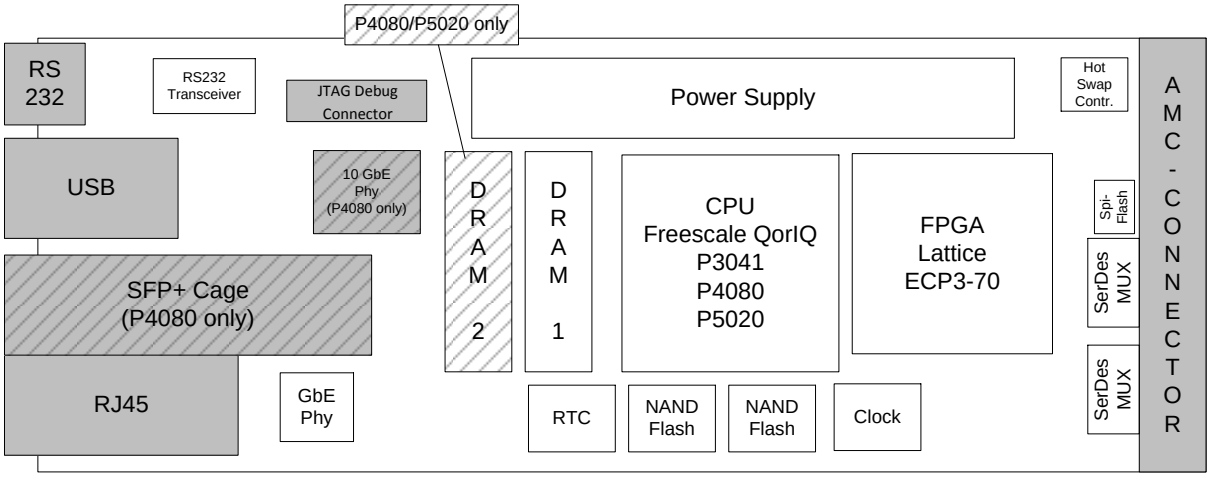
Figure 4: NAMC-QorIQ-P5020 – Block Diagram – Overview



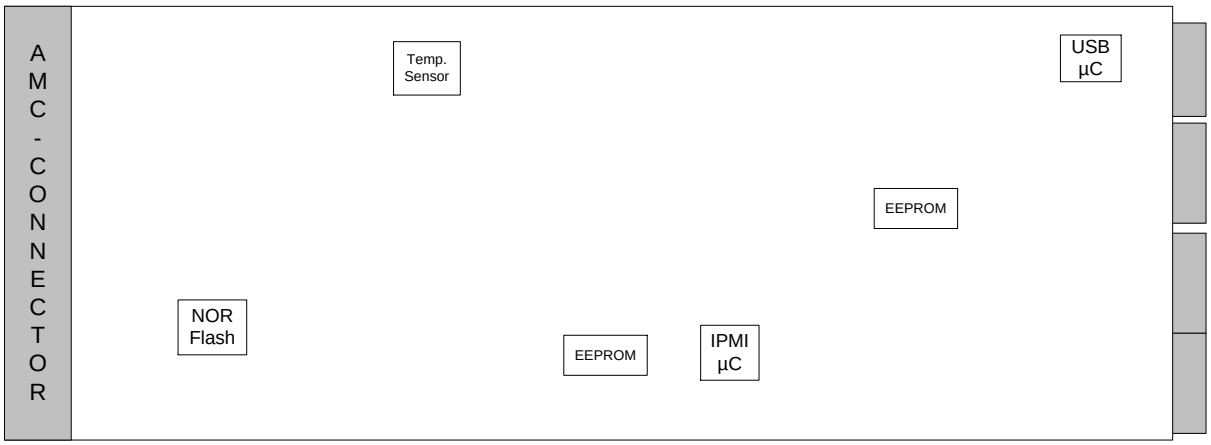
2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 5: NAMC-QorIQ-Pxxx – Location Diagram – Overview



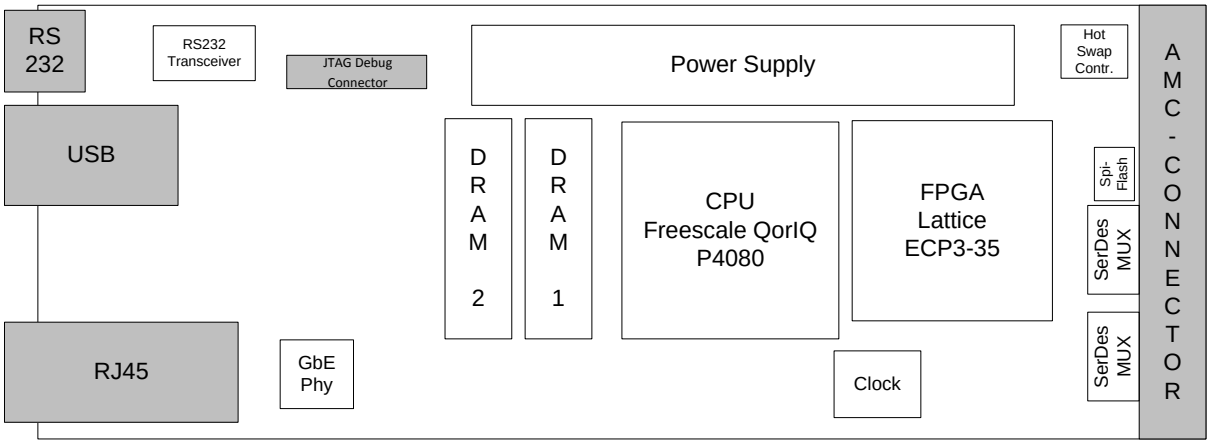
Top View



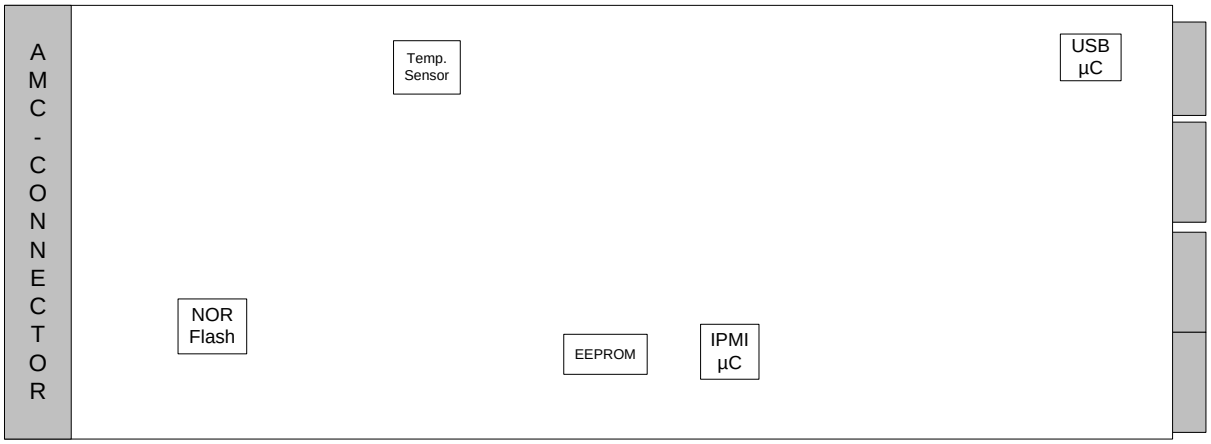
Bottom View

The following diagram shows important components on the **NAMC-QorIQ-P4080-ECO** version.

Figure 6: NAMC-QorIQ-P4080-ECO – Location Diagram – Overview



Top View



Bottom View

3 Board Features

The **NAMC-QorIQ-Pxxx** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 CPU

The Freescale QorIQ-CPU is a powerful packet processor which features Security and Pattern Match Engines to offload these functions from the CPU cores using sophisticated Buffer- and Queue Managers as additional hardware acceleration elements.
With its 64 bit memory interfaces it is able to support fast DDR3 DRAM. The 18 SerDes lanes offer flexible interface connectivity. IPv4 forwarding is supported at up to 20 Gbps or 18 Mpps (packets per second). IPsec Decap/Encap is supported at up to 5 Mpps.

Optionally, indicator LEDs for each processor core on the front plate provide a visual feedback of the current load balancing between the individual CPU cores.

The **NAMC-QorIQ-Pxxx** can be equipped with different CPU types. The following table gives an overview of the main differences of the modules.

Table 2: NAMC-QorIQ-Pxxx – CPU types and differences in modules

	NAMC-QorIQ-P3041	NAMC-QorIQ-P4080	NAMC-QorIQ-P5020
CPU core	4x e500mc PowerPC	8x e500mc PowerPC	2x e5500 Power PC
Core operating frequency	1.2 GHz, 1.333 GHz, 1.5 Ghz	1 GHz, 1.2 GHz, 1.333 GHz, 1.5 GHz	1.2 GHz, 1.6 GHz, 1.8 GHz, 2 GHz
Max. Power Consumption (CPU only)	15.4 W, 17.5 W, 19.9 W	20.5 W, 22 W, 28 W, 30 W	18 W, 23 W, 28 W, 30 W
L1 Cache I/D	32 KB/core	32 KB/core	32 KB/core
L2 Cache	128 KB/core	128 KB/core	512 KB/core
L3 Shared Platform Cache	1 MB	2 MB	2 MB
DDR I/F	1x 64 bit DDR3/3L with ECC	2x 64 bit DDR2/3 with ECC	2x 64 bit DDR2/3 with ECC
PCI Express	PCIe x4 on port 4-7 or 8-11	PCIe x4 on port 4-7 or 8-11	PCIe x4 on port 4-7 or 8-11
GbE	5x GbE	8x GbE	5x GbE
XAUI (10GbE)	1x 10GbE (via backplane only)	2x 10GbE	1x 10GbE (via backplane only)
Front-XAUI	-	1x Front-XAUI	-
SRIO	2x SRIO	2x SRIO	2x SRIO
SerDes Lanes	18 lanes	18 lanes	18 lanes
SATA	2x SATA 2.0	-	2x SATA 2.0

Other compatible QorIQ CPUs possible upon request (e.g. P4040, P5010).

3.2 FPGA

The FPGA used on the **NAMC-QorIQ-Pxxx** originates from the Lattice ECP3 family; the following devices, which mainly differ in logic, memory and clock resources, are supported: ECP3-70 (standard) and ECP3-35 (optional for cost reduction).

3.3 SerDes multiplexing circuit

The CPU SerDes lanes can be operated either as XAUI, SRIO, PCIe interface, or a combination of them.
The SerDes-MUX offers a flexible SerDes interconnect between backplane and CPU. The default configuration delivered with the **NAMC-QorIQ-Pxxx** implements a connection between the CPU's SerDes Bank 1/2 and the AMC ports 4-7/8-11 via a multiplexing circuit. For detailed information regarding the SerDes-Connectivity of the different CPU types refer to chapter 3.6.1.

3.4 Memory

3.4.1 DDR3 DRAM

The onboard DDR3 DRAM memories are 64-bit wide for each bank. The two banks (P3041: one bank only) can be equipped with 1 or 2 GB DRAM. The interface to the DDR3 DRAM is implemented directly in the CPU.
By programming several registers the DDR3 RAM controller can be adapted to different RAM architectures (P4080/P5020 only): the two memory banks can either be operated independently, which means mapped to different memory locations or they can be used in interleaved mode where they represent one memory.

3.4.2 NAND-Flash

The two NAND flash memory items on the **NAMC-QorIQ-Pxxx** are connected via local bus to the CPU. They provide a capacity of 2x 1 GB.
The NAND flash memory can be used for boot memory (NOR is preferred here) and general data storage.

3.4.3 NOR-Flash

The 16-bit-wide NOR flash memory item on the **NAMC-QorIQ-Pxxx** is connected via local bus to the CPU. It provides a capacity of 128 MB.
The NOR flash memory can be used for boot memory and general data storage. It is the default primary boot source.

3.4.4 FPGA SPI Flash

On power up the FPGA configures itself from a serial attached SPI Flash device. Beside the FPGA configuration file this memory can optionally be used to store the CPU's power up configuration (RCW) and/or boot code for the CPU. In this case the FPGA emulates an 8-bit wide parallel memory device attached via the local bus towards the CPU.

3.4.5 CPU SPI Flash

The CPU also has a 4MB SPI Flash connected to its first SPI chip select that is intended to hold the CPU's power up configuration (RCW, default sourced from this memory on **NAMC-QorIQ-Pxxx**). In addition it can be used as general purpose non-volatile memory.

3.5 WAN PLL (optional)

The WAN PLL takes the recovered clock information either from the iTDM interface or from protocols like RTP or IEEE1588 and derives standard clock frequencies as used in WAN applications and provides these clocking information to the standard AMC clock interface lines, further FPGA internal blocks and the QorIQ-CPU.

3.6 Backplane Interfaces

3.6.1 Flexible Fat Pipe Connectivity

In cooperation with a multiplexing unit the full Fat Pipe Region from Ports 4 – 11 is made accessible. The following figures give a detailed view on the SerDes connections of the **NAMC-QorIQ-Pxxx**.

Figure 7: NAMC-QorIQ-P4080 – SerDes Connectivity – Overview

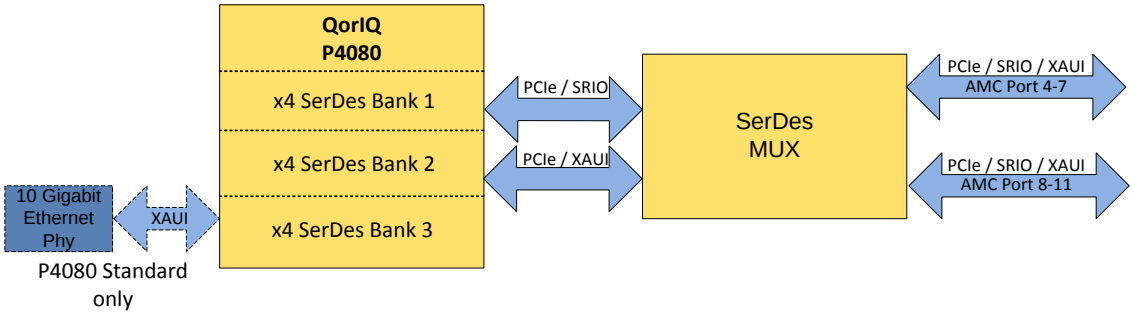
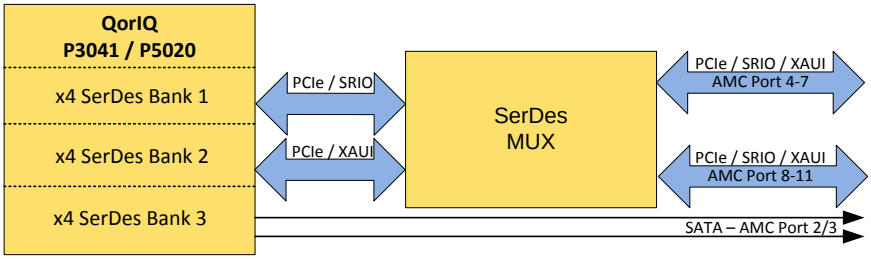


Figure 8: NAMC-QorIQ-P3041/P5020 – SerDes Connectivity - Overview



A summary of feasible SerDes options is given in the following tables:

Table 3: NAMC-QorIQ-P3041 – SerDes Connectivity – Details

Configuration Options										
SRDS PRTCL	**AMC Port 2**	**AMC Port 3**	**AMC Port 4**	**AMC Port 5**	**AMC Port 6**	**AMC Port 7**	**AMC Port 8**	**AMC Port 9**	**AMC Port 10**	**AMC Port 11**
0x14	-		***PCIe x4*** (2.5G/5G)				***PCIe x4*** (2.5G/5G)			
0x15 ***0x22*** ***0x34*** ***0x35***	***SATA*** (1.5G/3G)		***PCIe x4*** (2.5G/5G)				***XAUI*** (10GEC)			
			XAUI (10GEC)				***PCIe x4*** (2.5G/5G)			
0x1B	***SATA*** (1.5G/3G)		***SRIO x4*** (2.5G/3.125G/5G)				***XAUI*** (10GEC)			
			XAUI (10GEC)				***SRIO x4*** (2.5G/3.125G/5G)			
0x1D	***SATA*** (1.5G/3G)		***SRIO x4*** (3.125G)				***PCIe x4*** (2.5G)			
			PCIe x4 (2.5G)				***SRIO x4*** (3.125G)			

Table 4: NAMC-QorIQ-P4080 – SerDes Connectivity – Details

Configuration Options									
SRDS PRTCL	**Front XAUI**	**AMC Port 4**	**AMC Port 5**	**AMC Port 6**	**AMC Port 7**	**AMC Port 8**	**AMC Port 9**	**AMC Port 10**	**AMC Port 11**
0x05 ***0x0D*** ***0x22***	***XAUI*** (10GEC)	***PCIe x4*** (2.5G/5G)				***XAUI*** (10GEC)			
		XAUI (10GEC)				***PCIe x4*** (2.5G/5G)			
0x13	***XAUI*** (10GEC)	***SRIO x4*** (2.5G)				***XAUI*** (10GEC)			
		XAUI (10GEC)				***SRIO x4*** (2.5G)			
0x19	**-**	***SRIO x4*** (3.125G)				***PCIe x4*** (2.5G/5G)			
		PCIe x4 (2.5G/5G)				***SRIO x4*** (3.125G)			

Table 5: NAMC-QorIQ-P5020 – SerDes Connectivity – Details

Configuration Options										
SRDS PRTCL	**AMC Port 2**	**AMC Port 3**	**AMC Port 4**	**AMC Port 5**	**AMC Port 6**	**AMC Port 7**	**AMC Port 8**	**AMC Port 9**	**AMC Port 10**	**AMC Port 11**
0x14	-		***PCIe x4*** (2.5G/5G)				***PCIe x4*** (2.5G)			
0x21			***PCIe x4*** (2.5G)				***PCIe x4*** (2.5G/5G)			
0x15	***SATA*** (1.5G/3G)		***PCIe x4*** (2.5G/5G)				***XAUI*** (10GEC)			
0x22										
0x34			***XAUI*** (10GEC)				***PCIe x4*** (2.5G/5G)			
0x35										
0x1B	***SATA*** (1.5G/3G)		***SRIO x4*** (2.5G/5G)				***XAUI*** (10GEC)			
			XAUI (10GEC)				***SRIO x4*** (2.5G/5G)			
0x1D	***SATA*** (1.5G/3G)		***SRIO x4*** (3.125G)				***PCIe x4*** (2.5G)			
			PCIe x4 (2.5G)				***SRIO x4*** (3.125G)			

For details on the SerDes-MUX-Configuration, please refer to chapter 5.1.8.

3.6.1.1 XAUI

The most likely interface protocol to be used with the **NAMC-QorIQ-Pxxx** is the 10Gb/s Ethernet transmitted via 4 parallel 3.125Gbaud/s lines (XAUI). This protocol fits perfectly the CPU's dedicated frame processing acceleration units, the frame managers. While the P3041/P5020 CPUs run one XAUI interface from SerDes Bank 2 towards the backplane, the P4080 can operate two of these 10Gb/s Ethernet interfaces, with one operating via SFP+ to the front (Bank 3) and the other (Bank 2) through the SerDes MUX towards the backplane.
At this point the SerDes MUX can be used to select whether to operate the backplane XAUI via ports 4-7 or ports 8-11.

3.6.1.2 SRIO

The **NAMC-QorIQ-Pxxx** can be configured to implement one x4 SRIO interface. If configured this way, similar to the XAUI operation the SerDes MUX can be used as multiplexer to select whether the SRIO interface is connected to AMC ports 4-7 or ports 8-11.

3.6.1.3 PCIe

The FPGA on the **NAMC-QorIQ-Pxxx** can be configured to implement a PCIe (Gen2) interface operating on ports 4-7. Although not foreseen by the AMC specification, the PCIe interface could also be switched to ports 8-11 using the SerDes MUX. Functionality here depends on the customer's application and demands.

3.6.2 Gigabit Ethernet

The **NAMC-QorIQ-Pxxx** is equipped with two Gigabit Ethernet paths connecting to the backplane AMC ports 0 and 1. The 1000BaseX physical layer device is realized using the FPGA SerDes units.

One Gigabit Ethernet interface of the QorIQ-CPU is connected to the FPGA via RGMII while the other one is connected to the front panel interface. Depending on the user's application the FPGA logic can either just put through port 0 or 1 between backplane and CPU, it can realize hub- or switching functionality, or it can participate in data processing.

3.6.3 SATA on AMC port 2/3 (P3041/P5020 only)

SerDes Bank 3 of the QorIQ-CPUs supporting SATA (P3041/P5020) is connected to AMC ports 2 and 3. These CPU Types do not support the front 10G Ethernet via SFP+ as the respective SerDes lanes hold the SATA interfaces.

3.7 Front Panel Interfaces

3.7.1 XAUI (P4080 only)

SerDes Bank 3 of the P4080 is directly connected to a SFP+ PHY device (Netlogic AEL2005). By equipping different SFP+ transceivers the physical standard of this interface is adjustable. Please note, that this option is only available on the **NAMC-QorIQ-P4080** module.

3.7.2 Gigabit Ethernet

On its face plate the **NAMC-QorIQ-Pxxx** is equipped with one RJ45 jack, which offers a 10/100/1000-BaseT Ethernet interface, handled by a Broadcom PHY device (BCM5461). The PHY's MAC side interface is then further connected to the first of the CPU's RGMII Ethernet MAC controllers.

3.7.3 USB

The **NAMC-QorIQ-Pxxx** features an USB Type A Jack on its face plate which connects to an Atmel AVR USB controller (ATmega16U2). It can be used to implement various USB functionality, covering host or device behaviour. The standard application is the usage of the USB connection as a console interface. The first CPU UART interface is connected to the USB and thus all serial input/output is available at the USB interface.
On the host side the device is treated as a standard COM device.

If the host system runs a Linux operating system (or a derivate) the standard tty driver is sufficient. On Windows operating systems a configuration file for the standard serial driver is provided by N.A.T.

3.7.4 RS232

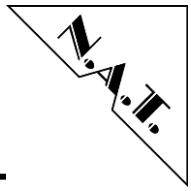
As alternative to the USB console interface the first CPU UART interface is also accessible via standard RS232, physically represented by a Mini-USB jack. Please note that only either RS232 or USB can be used to access the CPU UART.

3.8 iTDM

The **NAMC-QorIQ-Pxxx** optionally implements a serial iTDM backplane interface within the FPGA, the physical layer of which is 1000BaseX. The iTDM interface connects to port 0/1 of the Common Options Region of the AMC backplane connector and shares the ports with the CPU Ethernet path by doing arbitration for iTDM packets and CPU Ethernet packets to be sent. The iTDM interface is implemented in FPGA logic and conforms to the SFP.0 and SFP.1 specifications.

3.9 TDM

The **NAMC-QorIQ-Pxxx** implements an 8-bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz. Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. Similar to iTDM the TDM data path between FPGA and CPU is application specific and can be realized using the CPU's local bus. The TDM interface connects to ports 12, 13 (data) and port 14 (Sync) of the Common Options Region of the AMC connector.



3.10AMC Clock Interface

The **NAMC-QorIQ-Pxxx** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D.

All TCLK ports are connected directly to the FPGA; they can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from a packet stream or to synchronize the **NAMC-QorIQ-Pxxx** to an external clock.

3.11I²C-Devices and IPMB

The **NAMC-QorIQ-Pxxx** owns several I²C-Devices on different busses. Please note that the 7-bit I²C-Address is left aligned in the notation below, meaning that in the most-right bit (LSB) the I²C R/W bit resides.

3.11.1CPU Local I²C-Bus

Two I²C-Devices connect to the CPUs local bus:

- AT24C256 – EEPROM used for storage of board-specific information – I²C-Address: 0xA0
- DS1339 – Real-Time-Clock device – I²C-Address: 0xD0

The RTC can be supplied by a backup battery to keep information even in unpowered state.

3.11.2IPMB

To the IPMI-Controller (ATmega1284) connect several I²C-Devices:

- LM95241 – Temperature sensor device for measuring CPU and FPGA temperature – I²C-Address: 0x56
- LTC4215 – Hot Swap Controller – I²C-Address: 0x96

Additionally, the IPMB-Bus of the AMC connector is attached to the IPMI-Controller.

The IPMI-Controller manages the geographical address as requested by the AMC specification.

3.11.3SFP+-EEPROM

- AT24C08 – Configuration EEPROM of 10GbE-PHY – I²C-Address: 0xA0

3.12SPI Devices

A SPI Flash which is connected to the QorIQ-CPU is intended to hold power-up configuration for the CPU.
Also the USB-Microcontroller, an Atmel device as well, is connected to the FPGA via SPI, as the CPU's internal USB interface is blocked by alternative pin usage (RGMII).

The IPMI controller described in the previous paragraph connects to the FPGA via SPI. This part is used for microcontroller update as well as interaction between IPMI software and the board's main firmware.

3.13 Debug I/O

3.13.1RS232

The CPU's first UART interface is physically presented in a Mini-USB jack on the front panel that is meant to be used with an adapter cable; it offers standard RS232 in DSUB-9 (included in standard delivery). It is normally used for debugging purpose along with a standard terminal program (default baud rate: 19200).

3.13.2USB

The front panel USB interface offers comfortable access to the CPU's first UART by emulating a standard USB-connected COM device towards a connected PC. This is the preferred debug path for PC or notebooks that no longer feature native RS232 interfaces.

4 Hardware

4.1 AMC Port Definition

Table 6: AMC Port Mapping Strategy

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and CPU Ethernet), default
	1		1000BaseX Ethernet Channel 2 (iTDM and CPU Ethernet), redundant
	2		SATA (P3041, P5020)
	3		SATA (P3041, P5020)
	4	Fat Pipes	SerDes Mux Lane 0
	5		SerDes Mux Lane 1
	6		SerDes Mux Lane 2
	7		SerDes Mux Lane 3
Extended Connector	8	Region	SerDes Mux Lane 4
	9		SerDes Mux Lane 5
	10		SerDes Mux Lane 6
	11		SerDes Mux Lane 7
	12	Extended Options Region	TDM Bus D0-3 (H.110 extended)
	13		TDM Bus D4-7 (H.110 extended)
	14		optional clock lines (H.110 extended)/ unassigned
	15		Unassigned
	16		TCLKC / TCLKD
	17		unassigned
	18		unassigned
	19		unassigned
	20		unassigned

4.2 Front Panel and LED

The **NAMC-QorIQ-Pxxx** module is equipped with 2 bicolored LEDs integrated in the RJ45 interface jack. They are driven by the Ethernet PHY and can be programmed to various link indication modes.

Additionally the module contains the standard AMC LEDs, consisting of a fault indication LED controlled by the IPMI controller and a general purpose status LED controlled by the FPGA/CPU.

The fault indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Figure 9: NAMC-QorIQ-P4080 – Front Panel View

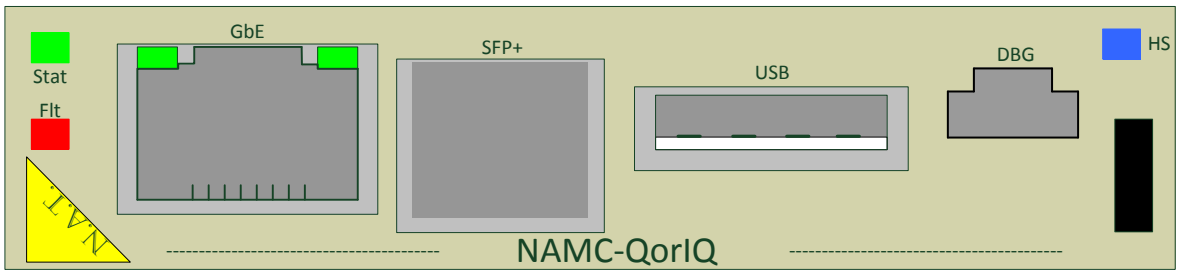
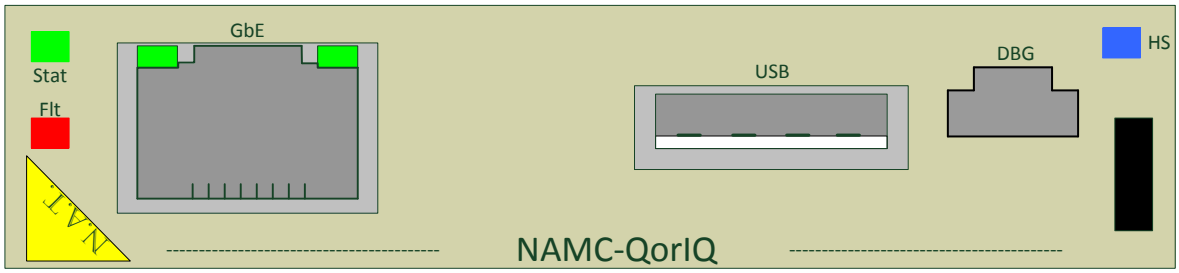
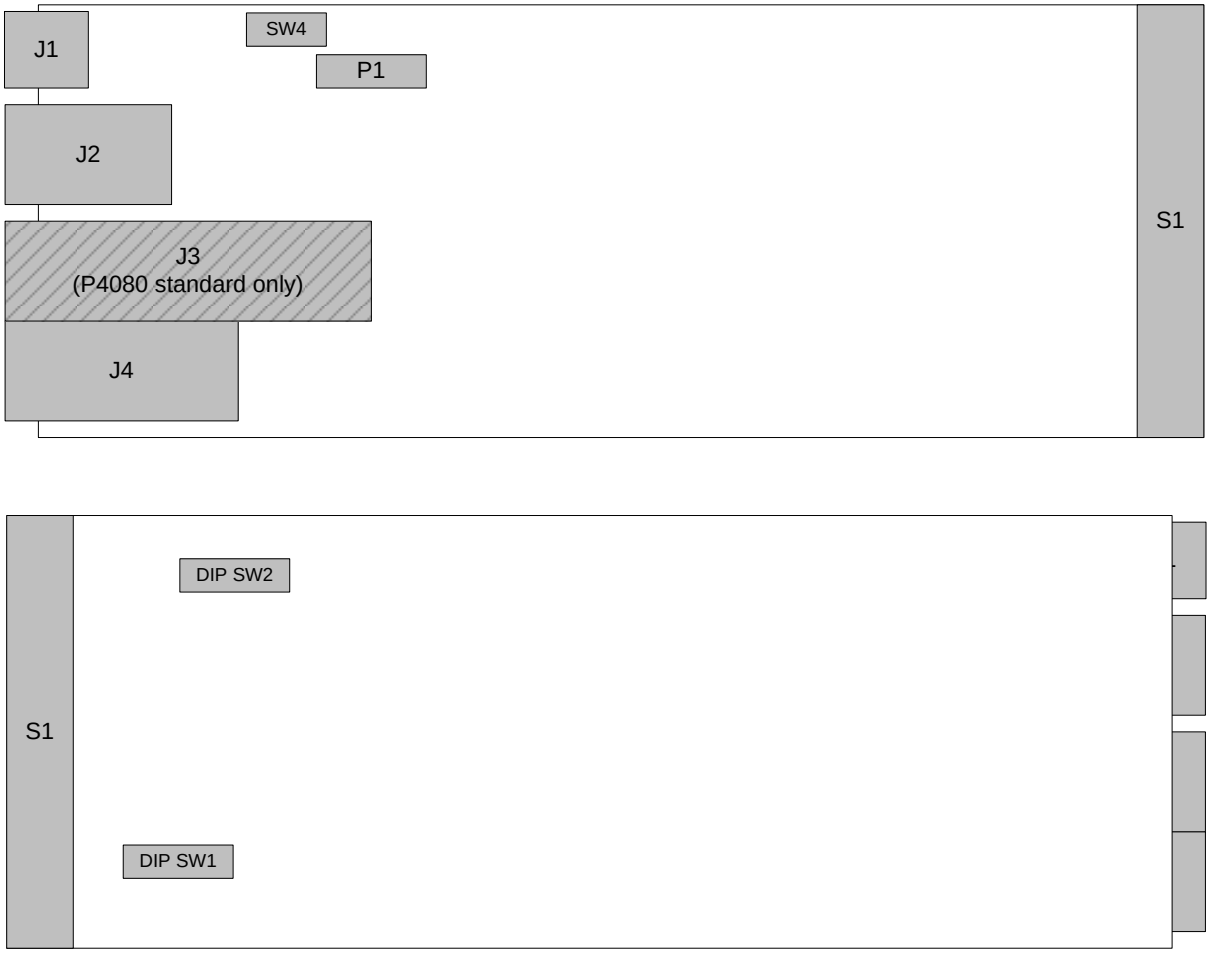


Figure 10: NAMC-QorIQ-P3041/P5020 and NAMC-QorIQ-P4080-ECO – Front Panel View



4.3 Connectors and Switches

Figure 11: NAMC-QorIQ-Pxxx – Connector und Switch Location – Overview



Please refer to the following tables to look up the connector and switch pin assignment of the **NAMC-QorIQ-Pxxx**.

4.3.1 S1: AMC Connector

Table 7: S1: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	NC	163
9	PWR	NC	162
10	GND	GND	161
11	PORT0_TX_P	NC	160
12	PORT0_TX_N	NC	159
13	GND	GND	158
14	PORT0_RX_P	NC	157
15	PORT0_RX_N	NC	156
16	GND	GND	155
17	GA1	NC	154
18	PWR	NC	153
19	GND	GND	152
20	PORT1_TX_P	NC	151
21	PORT1_TX_N	NC	150
22	GND	GND	149
23	PORT1_RX_P	NC	148
24	PORT1_RX_N	NC	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	PORT2_TX_P	NC	142
30	PORT2_TX_N	NC	141
31	GND	GND	140
32	PORT2_RX_P	TCLKD_P	139
33	PORT2_RX_N	TCLKD_N	138
34	GND	GND	137
35	PORT3_TX_P	TCLKC_P	136
36	PORT3_TX_N	TCLKC_N	135
37	GND	GND	134
38	PORT3_RX_P	NC	133
39	PORT3_RX_N	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PORT4_TX_P	RESVD	127

Pin #	AMC-Signal	AMC-Signal	Pin #
45	PORT4_TX_N	TDM_REF	126
46	GND	GND	125
47	PORT4_RX_P	TDM_FS	124
48	PORT4_RX_N	TDM_CLK	123
49	GND	GND	122
50	PORT5_TX_P	TDM7	121
51	PORT5_TX_N	TDM6	120
52	GND	GND	119
53	PORT5_RX_P	TDM5	118
54	PORT5_RX_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	PORT6_TX_P	TDM1	112
60	PORT6_TX_N	TDM0	111
61	GND	GND	110
62	PORT6_RX_P	PORT11_TX_P	109
63	PORT6_RX_N	PORT11_TX_N	108
64	GND	GND	107
65	PORT7_TX_P	PORT11_RX_P	106
66	PORT7_TX_N	PORT11_RX_N	105
67	GND	GND	104
68	PORT7_RX_P	PORT10_TX_P	103
69	PORT7_RX_N	PORT10_TX_N	102
70	GND	GND	101
71	IPMB_SDA	PORT10_RX_P	100
72	PWR	PORT10_RX_N	99
73	GND	GND	98
74	TCLKA_P	PORT9_TX_P	97
75	TCLKA_N	PORT9_TX_N	96
76	GND	GND	95
77	TCLKB_P	PORT9_RX_P	94
78	TCLKB_N	PORT9_RX_N	93
79	GND	GND	92
80	FCLKA_P	PORT8_TX_P	91
81	FCLKA_N	PORT8_TX_N	90
82	GND	GND	89
83	/PS0	PORT8_RX_P	88
84	PWR	PORT8_RX_N	87
85	GND	GND	86

4.3.2 J1: RS232 Connector

The RS232 connector J1 offers access to the UART1 of the CPU to realize a serial terminal interface.

Table 8: J1: RS232 Mini-USB Jack – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	NC	RxD	2
3	TxD	NC	4
5	GND		

4.3.3 J2: USB Connector

Connector J2 offers access to the USB microcontroller which is connected to the CPU via SPI.

Table 9: J2: USB Front-Panel Connector– Pin-Assignment

Pin #	Signal	Signal	Pin #
1	VBUS	USB_D_N	2
3	USB_D_P	GND	4

4.3.4 J3: SFP+ Cage (P4080 standard only)

Connector J3 offers access to the front XAUI interface of the **NAMC-QorIQ-P4080**.

Table 10: J3: SFP+ Front-Panel Cage (P4080 standard only) – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	GND	TX FAULT	2
3	TX DISABLE	SFP SDA	4
5	SFP SCL	MODDET	6
7	FPGA SFP0 RS0	RX LOS	8
9	FPGA SFP0 RS1	GND	10
11	GND	C HSRX N	12
13	C HSRX P	GND	14
15	+3.3V	+3.3V	16
17	GND	C HSTX P	18
19	C HSTX N	GND	20

4.3.5 J4: RJ45 Ethernet

Connector J4 offers access to a 10/100/1000-BaseT Ethernet interface.

Table 11: S2: RJ45 Front-Panel Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	TRD0+	TRD0-	2
3	TRD1+	TRD2+	4
5	TRD2-	TRD1-	6
7	TRD3+	TRD3-	8

4.3.6 P1: CPU BDM Header

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 12: P1: Development Port / BDM Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	TDO	nc	2
3	TDI	/TRST	4
5	10K PU to +3.3V	2K PU to+3.3V	6
7	TCK	/CKSTP_IN	8
9	TMS	nc	10
11	/SRESET	nc	12
13	/HRESET	nc	14
15	/CKSTP_OUT	GND	16

4.3.7 DIP SW1: Reserved / Reserved

The table below gives an overview of the operating parameters configurable via DIP SW1. Details are given in the following subchapters.

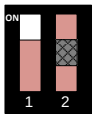
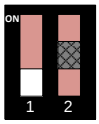
Table 13: DIP SW1 – Pin-Assignment – Overview

Switch #	Function
1	reserved
2	reserved

4.3.7.1 DIP SW1: Switch 1 – Reserved

This switch is not used yet, please do not alter it.

Table 14: DIP SW1: Switch 1 – Reserved

DIP SW1 – Switch 1	Function
	reserved
	reserved

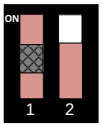
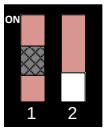
Default:

Switch 1 of DIP SW1 is toggled to OFF.

4.3.7.2 DIP SW1: Switch 2 – Reserved

This switch is not used yet, please do not alter it.

Table 15: DIP SW1: Switch 2 – Reserved

DIP SW1 – Switch 2	Function
	reserved
	reserved

Default:

Switch 2 of DIP SW1 is toggled to OFF.

4.3.8 DIP SW2: SerDes CLK1 Select / Reserved

The table below gives an overview of the operating parameters configurable via DIP SW2. Details are given in the following subchapters.

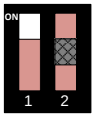
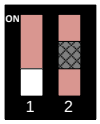
Table 16: DIP SW2 – Pin-Assignment – Overview

Switch #	Function
1	SerDes CLK1 select
2	reserved

4.3.8.1 DIP SW2: Switch 1 – SerDes CLK1 Select

By operating switch 1 of DIP SW2 to ON, the CPU SerDes Clock 1 is configured to 125MHz. If switch 1 of DIP SW2 is turned to OFF, the CPU SerDes Clock 1 is configured to 100MHz.

Table 17: DIP SW2: Switch 1 – SerDes CLK1 Select

DIP SW2 – Switch 1	Function
	SerDes CLK1 is 125MHz
	SerDes CLK1 is 100MHz

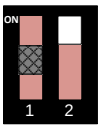
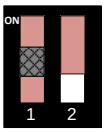
Default:

Switch 1 of DIP SW2 is toggled to OFF.

4.3.8.2 DIP SW2: Switch 2 – Reserved

This switch is not yet used, please do not alter it.

Table 18: DIP SW2: Switch 2 – Reserved

DIP SW2 – Switch 2	Function
	reserved
	reserved

Default:

Switch 2 of DIP SW2 is toggled to OFF.

4.3.9 SW4: Hot Swap Switch

Switch SW4 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

5 Programming Notes

5.1 FPGA Register Description 0x000..0x010

Table 19: FPGA Register Description

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	Reserved								PCB_VERS							
0x002	DEV_VERS								FPGA_VERS							
0x004	TEST_VAL_1															
0x006	TEST_VAL_2															
0x008	BOARD_ID															
0x010	CARRIER_ID								GEO_ADDRESS							
0x10A	GBE_PHY_CONFIG															
0x10C	SERDES_MUX_CONFIG															

5.1.1 0x000 – Reserved / PCB_VERS – Register Description

Table 20: 0x000 – Reserved / PCB_VERS

Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read Only
7..0	PCB_VERS	PCB version determined by level of unused pins hardcoded on PCB	HW init	Read Only

5.1.2 0x002 – DEV_VERS / FPGA_VERS – Register Description

Table 21: 0x002 – DEV_VERS / FPGA_VERS

Bit	Name	Description	Default	Access
15..8	DEV_VERS	Development version	na	Read Only
7..0	FPGA_VERS	FPGA version	na	Read Only

5.1.3 0x004 – TEST_VAL_1 – Register Description

Table 22: 0x004 – TEST_VAL_1

Bit	Name	Description	Default	Access
15..0	TEST_VAL_1	Random number for testing purposes	0xAA55	Read Only

5.1.4 0x006 – TEST_VAL_2 – Register Description

Table 23: 0x006 – TEST_VAL_2

Bit	Name	Description	Default	Access
15..0	TEST_VAL_2	Random number for testing purposes	0xDEAD	Read Only

5.1.5 0x008 – BOARD_ID – Register Description

Table 24: 0x008 – BOARD_ID

Bit	Name	Description	Default	Access
15..0	BOARD_ID	Holds internal Board-ID	0x0B33	Read Only

5.1.6 0x010 – CARRIER_ID / GEO_ADDRESS – Register Description

Table 25: 0x010 – CARRIER_ID / GEO_ADDRESS

Bit	Name	Description	Default	Access
15..8	CARRIER_ID	Carrier Manager ID 0x80 + 2*Carrier Number	0x00	Read Only
7..0	GEO_ADDRESS	Geographical Address (Slot ID) 0x72: AMC1 0x74: AMC2 0x76: AMC3 0x78: AMC4 0x7A: AMC5 0x7C: AMC6 0x7E: AMC7 0x80: AMC8 0x82: AMC9 0x84: AMC10 0x86: AMC11 0x88: AMC12	na	Read Only

5.1.7 0x10A – GBE_PHY_CONFIG – Register Description

Table 26: 0x10A – GBE_PHY_CONFIG

Bit	Name	Description	Default	Access
15..12		Reserved	0000	Read/Write
11	GBE_PHY_CONFIG_11	PHY_GFDX	1	Read/Write
10	GBE_PHY_CONFIG_10	PHY_GLOWPWR	0	Read/Write
9	GBE_PHY_CONFIG_9	PHY_GMANMS	0	Read/Write
8	GBE_PHY_CONFIG_8	PHY_GRGEN	1	Read/Write
7	GBE_PHY_CONFIG_7	PHY_GHUB	0	Read/Write
6	GBE_PHY_CONFIG_6	PHY_GER	0	Read/Write
5	GBE_PHY_CONFIG_5	PHY_GANEN	1	Read/Write
4	GBE_PHY_CONFIG_4	PHY_GAUTODET	0	Read/Write
3	GBE_PHY_CONFIG_3	PHY_GF1000	0	Read/Write
2	GBE_PHY_CONFIG_2	PHY_GSPD0	1	Read/Write
1	GBE_PHY_CONFIG_1	PHY_GI2CDIS	1	Read/Write
0	GBE_PHY_CONFIG_0	PHY_GQUAL	1	Read/Write

Default Power-Up-Configuration: auto-negotiate and clock shift on RGMII-Interface; Gigabit speed is restricted because several U-Boot-Configurations allow 100 Mbit/s as maximum.
For further information please refer to the documentation of the Broadcom PHY device BCM5461.

5.1.8 0x10C – SERDES_MUX_CONFIG – Register Description

Table 27: 0x10C – SERDES_MUX_CONFIG

Bit	Name	Description	Default	Access
15..3		Reserved	na	Read/Write
2..0	SERDES_MUX_CONFIG	111 – **straight** connection: => **SerDes-Bank 1** connected to **AMC ports 4-7** => **SerDes-Bank 2** connected to **AMC ports 8-11** 110 – **cross** connection: => **SerDes-Bank 1** connected to **AMC ports 8-11** => **SerDes-Bank 2** connected to **AMC ports 4-7**	110	Read/Write

6 Board Specification

Table 28: NAMC-QorIQ-Pxxx Specification – Overview

Processor	P3041/P4080/P5020 based Embedded PowerPC Architecture
AMC-Module	Standard Advanced Mezzanine Card, single width
Front-I/O	1x RJ45 Ethernet, USB Type A, RS232 (Mini-USB), 10GbE SFP+ (P4080 standard only)
Main Memory	1024 - 2048 MByte DDR3 SDRAM
FLASH PROM	2GB NAND Flash
Firmware	OK1, QNX BSP and LINUX BSP (on request)
Power Consumption	12V 5.0A max.
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG AMC.2 Rev. 1.0 (Type E2) PCI Express Base Specification Rev. 1.1 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0

Installation

6.1 Safety Note

To ensure proper functioning of the **NAMC-QorIQ-Pxxx** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-QorIQ-Pxxx** read this installation section
- Before installing or uninstalling the **NAMC-QorIQ-Pxxx**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-QorIQ-Pxxx** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary
    - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-QorIQ-Pxxx** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

6.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

6.2.1 Requirements

The installation requires only:

- an ATCA carrier board or a µTCA backplane for connecting the **NAMC-QorIQ-Pxxx**
- power supply
- cooling devices

6.2.2 Power supply

The power supply for the **NAMC-QorIQ-Pxxx** must meet the following specifications:

- required for the module: +12V / 5.0A max.

6.2.3 Automatic Power Up

In the following situations the **NAMC-QorIQ-Pxxx** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
- when +12V voltage level drops below 10V
- when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe-Reset.

6.3 Statement on Environmental Protection

6.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.3.4 Product Safety

The board complies with EN60950 and UL1950.

6.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] P3041 Reference Manual, Rev. 3, 06/2013
[2] P4080 Reference Manual, Rev. 1, 01/2012
[3] P5020 Reference Manual, Rev. 4, 07/2013
[4] Lattice ECP3-Family Data Sheet DS1021 Version 02.6EA, March 2014
[5] Broadcom PHY 5461 Product Brief 5461-PB05-R 04/17/06

Appendix B: Document's History

Revision	Date	Description	Author
1.0	25.04.2013	initial revision	se
1.1	26.04.2013	Adaption to standard version of NAMC-QorIQ-P40	se/te
1.2	10.07.2013	Adapted to new layout	se
1.3	11.12.2013	Module naming / Manual title updated SerDes-related contents reworked Added overview of different CPU types Added/updated block diagrams for all CPU types New front plate figures Minor changes	se
	22.01.2014	Added chapter "Programming Notes"	se
	02.04.2014	Adapted to HW-Rev. 1.2 Added ECO-Version Reworked Diagrams Minor changes, e.g. typos Reworked chapter 3.11: I²C-Devices and IPMB	se
	23.09.2014	Update chapter 6.3 RoHS-Directive / REACH Update Abbreviation List Added chapter 5.1.7 – Register 0x10A and 5.1.8 – Register 0x10C	se