NAMC-QorIQ-P204x
CPU AMC Module
Technical Reference Manual V1.2
HW Revision 1.0

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

Table 1: **List of used abbreviations**

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
BDM	Background Debug Mode
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
ECC	Error Correction Code
FCLK	Fabric Clock
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GMII	Gigabit Media Independent Interface
I²C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
iTDM	Internal TDM
LSB	Least Significant Bit
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MRAM	Magnetoresistive RAM
MSB	Most Significant Bit
MUX	Multiplexing Unit
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PHY	Physical Layer Device
R/W	Read/Write
RAM	Random Access Memory
(P)ROM	(Programmable) Read Only Memory
RCW	Reset Configuration Word
RGMII	Reduced GMII
SATA	Serial Advanced Technology Attachment
SD-Card	Secure Digital Memory Card
SerDes	Serializer/Deserializer
SFP	Small Form-Factor Pluggable
SGMII	Serial GMII
SRIO	Serial Rapid I/O
SPI	Serial Peripheral Interface
TCKL	Telecom Clock
TDM	Time Division Multiplex

Abbreviation	Description
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

The **NAMC-QorIQ-P204x** is a multi-service quad-core CPU board featuring various Ethernet interfaces, PCIe Gen2 and SRIO connectivity. If equipped with a P2041 CPU it even offers a 10Gbit/s Ethernet interface.

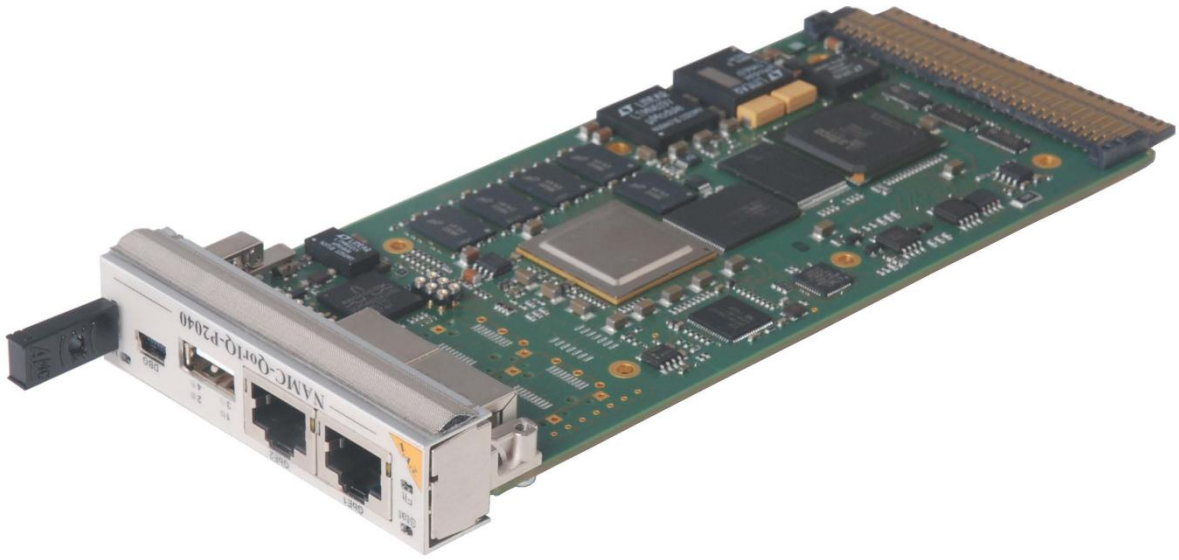
It is equipped with both software-based processing resources in the form of the Freescale QorIQ P2041/2040 CPU and hardware-based resources featured by a Lattice ECP3-17 FPGA.

The board offers a low power and a low cost Power PC based multi-core computing platform with extension options for adaptation to the particular application needs.

Form factor for this board is the Advanced Mezzanine Card (AMC) standard, offering access to the flexible and powerful system standards ATCA and µTCA.

The following figure shows a picture of the **NAMC-QorIQ-P204x:**

Figure 1: **NAMC-QorIQ-P204x**



2 Overview

2.1 Major Features

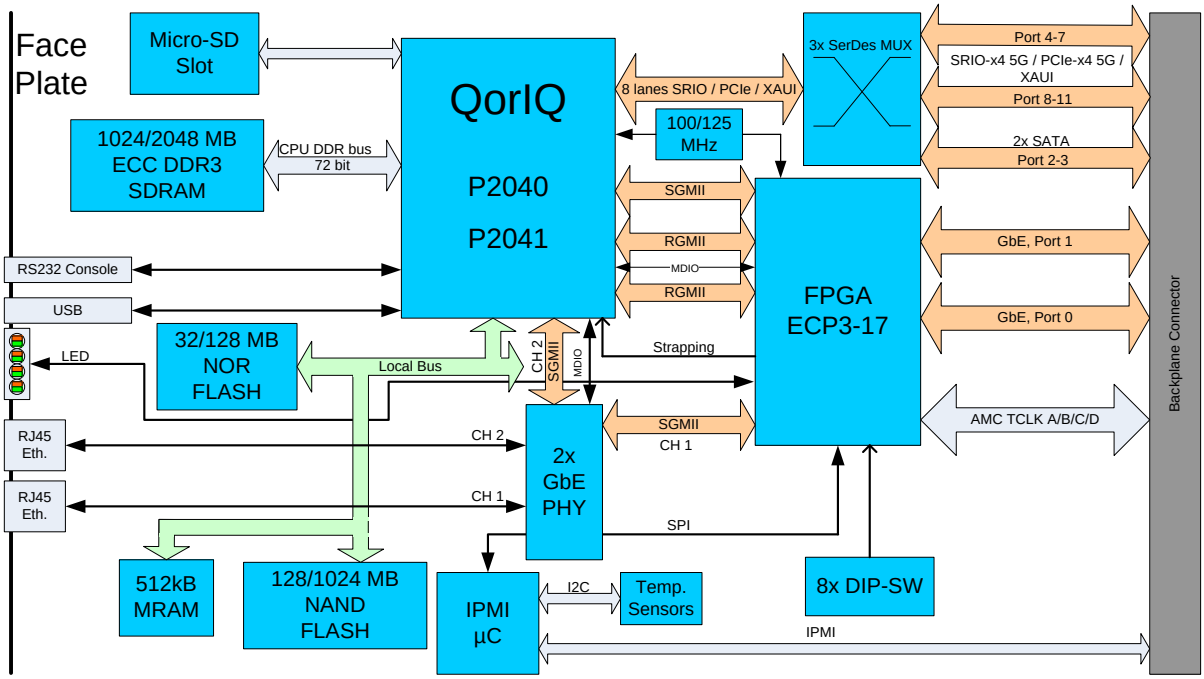
- CPU – Freescale QorIQ P2041
  - Packet processor featuring 4x e500mc PowerPC Cores @ up to 1.5 GHz
  - 10x SerDes
  - 128 kb/core L2 cache
  - 10 GbE-Interface (XAUI) via backplane
- CPU - Freescale QorIQ P2040
  - Packet processor featuring 4x e500mc PowerPC Cores @ up to 1.2 GHz
  - 10x SerDes
- FPGA: Lattice ECP3-17
- 1024 – 4096 MB DDR3 DRAM – 64 bit wide, ECC as option
- 128 – 1024 MB NAND Flash memory
- 32 – 128 MB NOR Flash memory
- 512 kB MRAM
- Micro SD-Card Slot
- Backplane Interfaces:
  - XAUI (P2041 only), SRIO and PCIe to AMC fat pipe region
  - 2x Gigabit Ethernet to AMC Ports 0/1
  - 2x SATA to AMC Ports 2/3
- Front Panel Interfaces:
  - 2x Gigabit Ethernet via RJ45 or SFP (assembly option)
  - USB
  - RS232

For detailed description see the following chapter.

2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-QorIQ-P204x**.

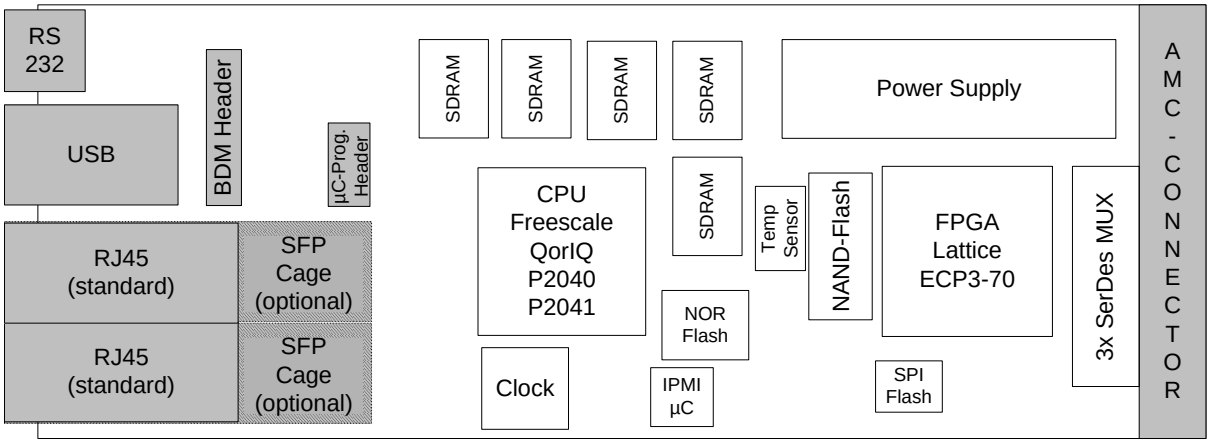
Figure 2: **NAMC-QorIQ-P204x – Block Diagram – Overview**



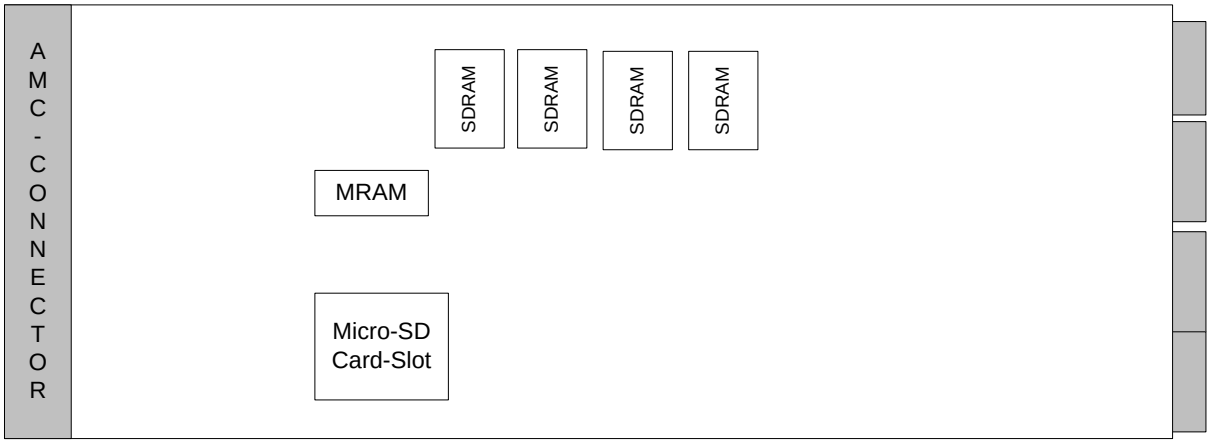
2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: **NAMC-QorIQ-P204x – Location Diagram – Overview**



Top View



Bottom View

3 Board Features

The **NAMC-QorIQ-P204x** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 CPU

The **NAMC-QorIQ-P204x** can be equipped with the Freescale QorIQ P2041/P2040 CPU. This chapter describes the common features of both CPUs. For the differences between these CPU types please refer to the table below.

The CPU either boots its firmware from NOR Flash, from the onboard NAND Flash chip or from the Micro SD-Card slot; the boot source is selectable by DIP switches with the default boot location being the NOR Flash.
Operating memory consists of 64-bit wide DDR3 SDRAM; a 512kB MRAM chip can be used to store changing data in non-volatile memory permanently.

10 SerDes lanes offer flexible interface connectivity (see chapter 3.4 for details). Two Gigabit Ethernet ports of the CPU are connected to the FPGA and can be connected either to operate via the second front panel Ethernet jack or the two backplane Ethernet lines. One Gigabit Ethernet port of the CPU is connected directly to the front Ethernet PHY.

All QorIQ-CPUs feature Security and Pattern Match Engines to offload these functions from the CPU cores and sophisticated Buffer and Queue Managers as additional hardware acceleration elements.

An indicator LED is supported for each processor core to provide a visual feedback of the current load balancing between the individual CPU cores (option).

Table 2: **Freescale QorIQ P2041/P2040 – Main Differences**

Feature	QorIQ P2041	QorIQ P2040
Core Frequency	1.5 GHz	1.2 GHz
L2 Cache	128 kb/core	-
10 GbE Interfaces (XAUI)	1	-
Max. power consumption	19.3 W	14.8 W

3.2 FPGA

The **NAMC-QorIQ-P204x** is equipped with a Lattice ECP3-17 FPGA which implements several interconnecting blocks.

It performs the Ethernet multiplexing and switching between the two CPU RGMII ports, one CPU SGMII port, one of the two front panel Ethernet interfaces and the two backplane GbE lines.

All clocking relevant signals are present at the FPGA to provide maximum flexible clocking structure for the board.

3.3 Memory

3.3.1 DDR3 DRAM

The onboard DDR3 DRAM memory is 64-bit wide and can be equipped with 1 or 2 GB DRAM. The interface to the DDR3 DRAM is implemented directly in the CPU.

As an assembly option, the **NAMC-QorIQ-P204x** supports ECC (Error Correction Code): in addition to the data width of 64 bit another 8 bit wide interface for error correction is assembled.

3.3.2 NAND-Flash

The NAND flash memory on the **NAMC-QorIQ-P204x** is connected via local bus to the CPU. It provides a capacity of 128-1024 MB.
The NAND flash memory can be used for boot memory (NOR is preferred here) and general data storage.

3.3.3 NOR-Flash

The 16 bit wide NOR flash memory item on the **NAMC-QorIQ-P204x** is connected via local bus to the CPU. It provides a capacity of 32-128 MB.
The NOR flash memory can be used for boot memory and general data storage. It is the default primary boot source.

3.3.4 FPGA SPI Flash

On power up the FPGA configures itself from a serial attached SPI Flash device. Beside the FPGA configuration file this memory can optionally be used to store the CPU's power up configuration (RCW) and/or boot code for the CPU. In this case the FPGA emulates an 8-bit wide parallel memory device attached via the local bus towards the CPU.

3.3.5 CPU SPI Flash

The CPU also has a 4MB SPI Flash connected to its first SPI chip select that is intended to hold the CPU's power up configuration (RCW, default sourced from this memory on **NAMC-QorIQ-P204x**). In addition it can be used as general purpose non-volatile memory.

3.3.6 MRAM

The non-volatile 512kB MRAM is used for storing data permanently. It can be accessed like an SRAM, without having any limitation in the number of allowed write cycles like known from EEPROM or Flash memories.

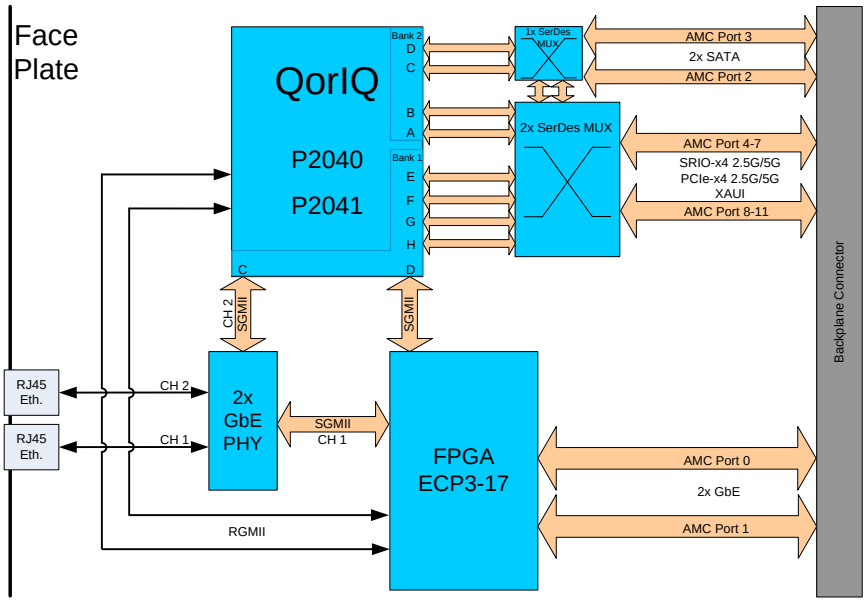
3.3.7 Micro SD-Card Slot

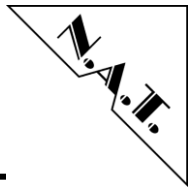
The SD-Card inserted in the Micro SD-Card Slot can be chosen as boot source.

3.4 SerDes multiplexing circuit

The **NAMC-QorIQ-P204x** offers 10 SerDes lanes; in cooperation with a multiplexing unit the full Fat Pipe Region from Ports 4 – 11 is made accessible.
As shown below three SerDes-MUX offer a flexible SerDes interconnect between backplane and CPU. They connect 8 SerDes lanes of the CPU to the AMC Ports 4-11; 2 SerDes lanes are directly connected to the FPGA and the GbE-PHY.

Figure 4: **NAMC-QorIQ-P204x – Block Diagram – SerDes Block**





The CPU SerDes lanes can be operated either as XAUI (P2041 only), SRIO, PCIe interface or a combination of them. The following table shows the most important feasible combinations.

Table 3: **NAMC-QorIQ-P204x – Flexible SerDes Connectivity**

Configuration Options										
SRDS PRTCL	**AMC Port 2**	**AMC Port 3**	**AMC Port 4**	**AMC Port 5**	**AMC Port 6**	**AMC Port 7**	**AMC Port 8**	**AMC Port 9**	**AMC Port 10**	**AMC Port 11**
0x08	***SATA*** (1.5G/3G)	***SATA*** (1.5G/3G)	***PCIe x4*** (2.5G/5G)				-	-	-	-
	SATA (1.5G/3G)	***SATA*** (1.5G/3G)	-	-	-	-	***PCIe x4*** (2.5G/5G)			
0x09	-	-	***PCIe x4*** (2.5G/5G)				***XAUI*** (10GEC – P2041 only)			
	-	-	***XAUI*** (10GEC – P2041 only)				***PCIe x4*** (2.5G/5G)			
0x0A	-	-	***PCIe x4*** (2.5G/5G)				***PCIe x4*** (2.5G/5G)			
0x0D	***SATA*** (1.5G/3G)	***SATA*** (1.5G/3G)	***SRIO x4*** (2.5G/5G)				-	-	-	-
	SATA (1.5G/3G)	***SATA*** (1.5G/3G)	-	-	-	-	***SRIO x4*** (2.5G/5G)			
0x0E	-	-	***PCIe x4*** (2.5G/5G)				***SRIO x4*** (2.5G/5G)			
	-	-	***SRIO x4*** (2.5G/5G)				***PCIe x4*** (2.5G/5G)			

For detailed information on how to select the desired SerDes combination, see chapter 4.3.10.

3.5 Ethernet Mapping

The following table describes the default Ethernet mapping.

Table 4: **NAMC-QorIQ-P204x – Default Ethernet Mapping**

CPU Interface	Protocol	Destination	Supported Speed	Device name in UBoot
dTSEC1	Direct SGMII	Front PHY BCM5482S – channel 2 RJ45 jack – GbE2	10/100/1000 Mbit/s	FM1@DTSEC1
dTSEC2	SGMII through FPGA	Front PHY BCM5482S – channel 1 RJ45 jack – GbE1	1000 Mbit/s	FM1@DTSEC2
dTESC4	RGMII through FPGA	AMC Port0 GbE	1000 Mbit/s	FM1@DTSEC4
dTESC5	RGMII through FPGA	AMC Port1 GbE	1000 Mbit/s	FM1@DTSEC5

3.6 Backplane Interfaces

3.6.1 XAUI (P2041 only)

The most likely interface protocol to be used with the P2041-CPU is the 10Gb/s Ethernet transmitted via 4 parallel 3.125Gbaud/s lanes (XAUI). This protocol fits perfectly the CPU's dedicated frame processing acceleration unit, the frame manager. The P2041-CPU can operate one 10Gb/s Ethernet interface through the SerDes MUX towards the backplane.
At this point the SerDes MUX can be used to select whether to operate the backplane XAUI via ports 4-7 or ports 8-11.

3.6.2 SRIO

The **NAMC-QorIQ-P204x** can be configured to implement one x4 SRIO interface. If configured this way, similar to the XAUI operation the SerDes MUX can be used as multiplexer to select whether the SRIO interface is connected to AMC ports 4-7 or ports 8-11.

3.6.3 PCIe

The **NAMC-QorIQ-P204x** can be configured to implement one or two PCIe x4 interfaces operating on ports 4-7 and/or ports 8-11.

3.6.4 Gigabit Ethernet

The **NAMC-QorIQ-P204x** is equipped with two Gigabit Ethernet paths connecting to the backplane AMC ports 0 and 1. The 1000BaseX physical layer device is realized using the FPGA SerDes units.
Per default these two Ethernet interfaces are connected to the two RGMII ports of the CPU. Depending on the user's application the FPGA logic can either just put through port 0 and 1 between backplane and CPU or its functionality could later be extended to realize hub- or switching functionality or to participate in data processing.

3.6.5 SATA

AMC ports 2 and 3 can be connected via SerDes-MUX to the SATA SerDes lanes of the CPU.

3.7 Front Panel Interfaces

3.7.1 Gigabit Ethernet

On its face plate the **NAMC-QorIQ-P204x** is equipped with two RJ45 jacks, which offer a 10/100/1000-BaseT Ethernet interface each, handled by a Broadcom PHY device (BCM5461). The PHY's MAC side interface of channel 2 is then further connected to the first of the CPU's SGMII Ethernet MAC controllers.

As an assembly option the RJ45 jacks can be replaced by two SFP jacks which offer an optical GbE-Interface.

3.7.2 USB via Type-A jack

The **NAMC-QorIQ-P204x** features an USB Type-A jack on its face plate which connects to the USB interface of the CPU. It acts as host interface and features common USB functionality e.g. operating an USB-Flash memory.

3.7.3 RS232 via Mini-USB jack

The first CPU UART interface is accessible via standard RS232. This interface is physically presented by a Mini-USB jack that is meant to be used with an adapter cable; it offers standard RS232 in DSUB-9 (included in standard delivery). It is normally used for debugging purpose along with a standard terminal program (default baud rate: 115200).

3.8 AMC Clock Interface

The **NAMC-QorIQ-P204x** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D and FCLKA.

All TCLK ports are connected directly to the FPGA and can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from a packet stream or to synchronize the **NAMC-QorIQ-P204x** to an external clock.

3.9 I²C-Devices and IPMB

The **NAMC-QorIQ-P204x** owns several I²C-Devices on different busses. Please note that the 7-bit I²C-Address is left aligned in the notation below, meaning that in the most-right bit (LSB) the I²C R/W bit resides.

3.9.1 CPU Local I²C-Bus

One I²C-Device connects to the CPUs local bus:

- AT24C256 – EEPROM used for storage of board-specific information
  – I²C-Address: 0xA0

3.9.2 IPMB

To the IPMI-Controller (ATmega1284) connect several I²C-Devices:

- LM95241 – Temperature sensor device for measuring CPU on-die temperature and power supply's DC/DC converter temperature – I²C-Address: 0x56
- LTC4215 – Hot Swap Controller – I²C-Address: 0x96

Additionally, the IPMB-Bus of the AMC connector is attached to the IPMI-Controller.

The IPMI-Controller manages the geographical address as requested by the AMC specification.

3.10 SPI Devices

The CPU and the FPGA on the **NAMC-QorIQ-P204x** are connected to their own SPI Flash (2x W25X32) which is intended to hold power-up configuration for the respective device.

The IPMI controller described in the previous paragraph connects to the FPGA via SPI. This part is used for both microcontroller update and interaction between IPMI software and the board's main firmware.

4 Hardware

4.1 AMC Port Definition

Table 5: **AMC Port Mapping Strategy**

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and CPU Ethernet), default
	1		1000BaseX Ethernet Channel 2 (iTDM and CPU Ethernet), redundant
	2		SATA
	3		SATA
	4	Fat Pipes	SerDes Mux Lane 0
	5		SerDes Mux Lane 1
	6		SerDes Mux Lane 2
	7		SerDes Mux Lane 3
Extended Connector	8	Region	SerDes Mux Lane 4
	9		SerDes Mux Lane 5
	10		SerDes Mux Lane 6
	11		SerDes Mux Lane 7
	12	Extended Options Region	unassigned
	13		unassigned
	14		unassigned
	15		Unassigned
	16		TCLKC / TCLKD
	17		unassigned
	18		unassigned
	19		unassigned
	20		unassigned

4.2 Front Panel and LEDs

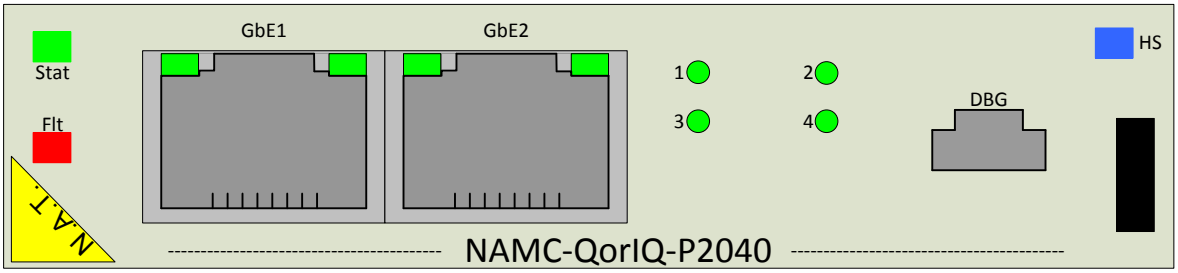
The **NAMC-QorIQ-P204x** module is equipped with 2 bicoloured-LEDs integrated in the RJ45 interface jacks. They are driven by the Ethernet PHY and can be programmed to various link indication modes.

Additionally the module contains the standard AMC LEDs, consisting of a fault indication LED controlled by the IPMI controller and a general purpose status LED controlled by the FPGA/CPU.
The Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the General Purpose LED physically consists of two LEDs (green and orange) sharing the same hole in the Front Plate.

Four green LEDs are controlled by the FPGA. See chapter 5.1.10 for the different states they can take.

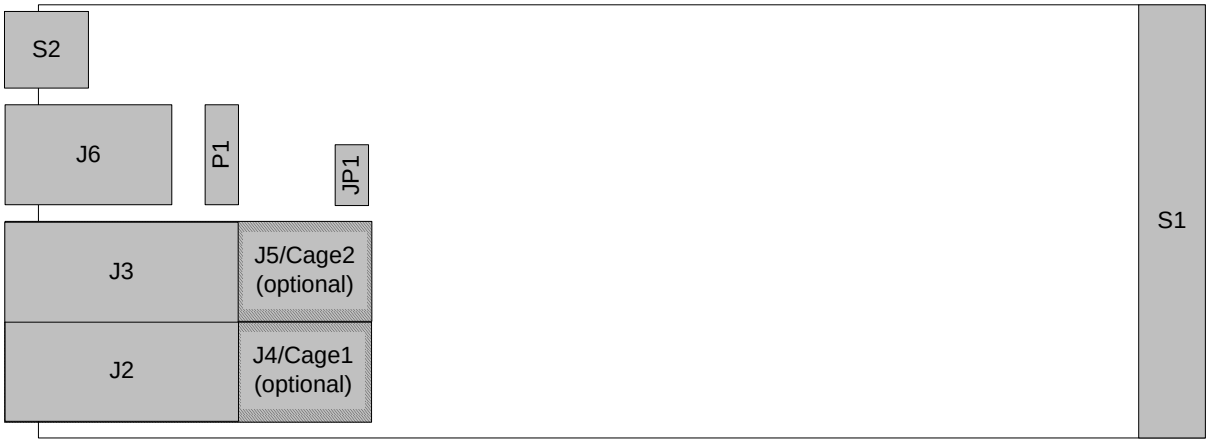
Figure 5: **NAMC-QorIQ-P204x – Front Panel View**



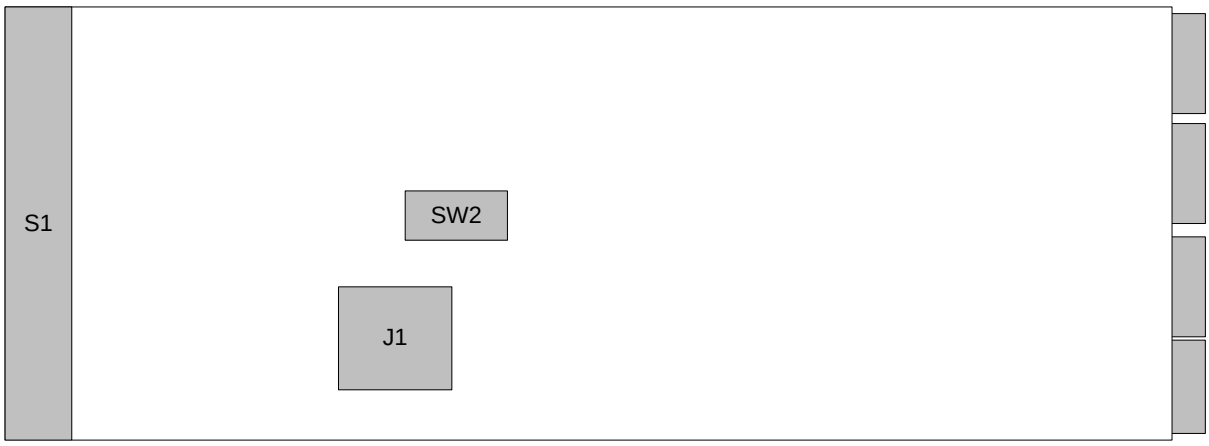
NOTE:
This figure shows the **NAMC-QorIQ-P204x** Low Cost variant; the front USB-interface is missing here.

4.3 Connectors and Switches

Figure 6: **NAMC-QorIQ-P204x – Connector and Switch Location – Overview**



Top View



Bottom View

Please refer to the following tables to look up the connector and switch pin assignment of the **NAMC-QorIQ-P204x**.

4.3.1 S1: AMC Connector

Table 6: **S1: AMC Connector – Pin-Assignment**

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	NC	163
9	PWR	NC	162
10	GND	GND	161
11	PORT0_TX_P	NC	160
12	PORT0_TX_N	NC	159
13	GND	GND	158
14	PORT0_RX_P	NC	157
15	PORT0_RX_N	NC	156
16	GND	GND	155
17	GA1	NC	154
18	PWR	NC	153
19	GND	GND	152
20	PORT1_TX_P	NC	151
21	PORT1_TX_N	NC	150
22	GND	GND	149
23	PORT1_RX_P	NC	148
24	PORT1_RX_N	NC	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	PORT2_TX_P	NC	142
30	PORT2_TX_N	NC	141
31	GND	GND	140
32	PORT2_RX_P	TCLKD_P	139
33	PORT2_RX_N	TCLKD_N	138
34	GND	GND	137
35	PORT3_TX_P	TCLKC_P	136
36	PORT3_TX_N	TCLKC_N	135
37	GND	GND	134
38	PORT3_RX_P	NC	133
39	PORT3_RX_N	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PORT4_TX_P	RESVD	127

Pin #	AMC-Signal	AMC-Signal	Pin #
45	PORT4_TX_N	NC	126
46	GND	GND	125
47	PORT4_RX_P	NC	124
48	PORT4_RX_N	NC	123
49	GND	GND	122
50	PORT5_TX_P	NC	121
51	PORT5_TX_N	NC	120
52	GND	GND	119
53	PORT5_RX_P	NC	118
54	PORT5_RX_N	NC	117
55	GND	GND	116
56	IPMB_SCL	NC	115
57	PWR	NC	114
58	GND	GND	113
59	PORT6_TX_P	NC	112
60	PORT6_TX_N	NC	111
61	GND	GND	110
62	PORT6_RX_P	PORT11_TX_P	109
63	PORT6_RX_N	PORT11_TX_N	108
64	GND	GND	107
65	PORT7_TX_P	PORT11_RX_P	106
66	PORT7_TX_N	PORT11_RX_N	105
67	GND	GND	104
68	PORT7_RX_P	PORT10_TX_P	103
69	PORT7_RX_N	PORT10_TX_N	102
70	GND	GND	101
71	IPMB_SDA	PORT10_RX_P	100
72	PWR	PORT10_RX_N	99
73	GND	GND	98
74	TCLKA_P	PORT9_TX_P	97
75	TCLKA_N	PORT9_TX_N	96
76	GND	GND	95
77	TCLKB_P	PORT9_RX_P	94
78	TCLKB_N	PORT9_RX_N	93
79	GND	GND	92
80	FCLKA_P	PORT8_TX_P	91
81	FCLKA_N	PORT8_TX_N	90
82	GND	GND	89
83	/PS0	PORT8_RX_P	88
84	PWR	PORT8_RX_N	87
85	GND	GND	86

4.3.2 S2: RS232 Connector

The RS232 connector S2 offers access to the UART1 of the CPU to realize a serial terminal interface.

Table 7: **S2: RS232 Mini-USB Jack – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	NC	RxD	2
3	TxD	NC	4
5	GND		

4.3.3 J1: Micro SD-Card Slot

Micro SD-Card Slot J1 offers ability to use a removable Flash-Memory.

Table 8: **J1: Micro SD-card Slot – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	DAT2/RSV_	CD/DAT3/CS	2
3	CMD/DI	VDD	4
5	CLK/SCLK	VSS	6
7	DAT0/D0	DAT1/RSV	8

4.3.4 J2/J3: RJ45 Ethernet Connectors (Standard)

Connector J2/J3 offer access to a 10/100/1000-BaseT Ethernet interface. As an assembly option, these connectors can be replaced by two SFP-Connectors J4/J5 (see the following subchapter for details).

Table 9: **J2/J3: RJ45 Ethernet Connectors – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	TRD0+	TRD0-	2
3	TRD1+	TRD2+	4
5	TRD2-	TRD1-	6
7	TRD3+	TRD3-	8

4.3.5 J4/J5 and Cage 1/2: SFP-Connectors (Assembly option)

Connector J4/J5 offer access to an optical GbE-Interface. As an assembly option they replace RJ45-Connectors J2/J3.

Table 10: **J4/J5: SFP-Connectors – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	GND	TX FAULT	2
3	TX DISABLE	SFP SDA	4
5	SFP SCL	MODDET	6
7	FPGA SFP0 RS0	RX LOS	8
9	FPGA SFP0 RS1	GND	10
11	GND	C HSRX N	12
13	C HSRX P	GND	14
15	+3.3V	+3.3V	16
17	GND	C HSTX P	18
19	C HSTX N	GND	20

4.3.6 J6: USB-Connector Type-A

Connector J6 offers common USB functionality e.g. operating an USB-Flash memory.

Table 11: **J6: USB-Connector– Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	VBUS	USB_D_N	2
3	USB_D_P	GND	4

4.3.7 JP1: Atmel Programming Connector

The Atmel Programming Connector JP1 allows updating the Atmel Microcontroller. It is not assembled and for development use only.

Table 12: **JP1: Atmel Programming Connector – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	ATMEL MISO	3.3V_MP	2
3	ATMEL SCK	ATMEL MOSI	4
5	/RST IPMI	GND	6

4.3.8 P1: CPU BDM Header

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 13: **P1: Development Port / BDM Connector – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	TDO	nc	2
3	TDI	/TRST	4
5	10K PU to +3.3V	2K PU to+3.3V	6
7	TCK	/CKSTP_IN	8
9	TMS	nc	10
11	/SRESET	nc	12
13	/HRESET	nc	14
15	/CKSTP_OUT	GND	16

4.3.9 HS1: Hot Swap Switch

Switch HS1 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

4.3.10DIP SW2: SerDes Mode Select / MUX Mode Select / Reserved

The table below gives an overview of the operating parameters configurable via DIP SW2. Details are given in the following subchapters.

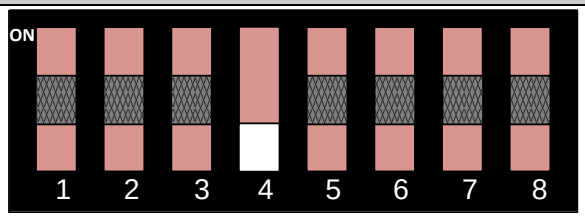
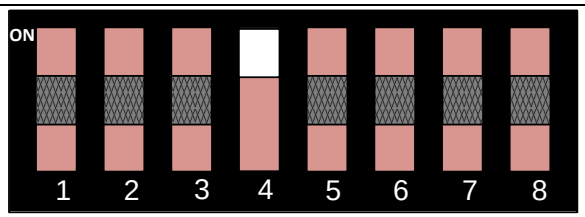
Table 14: **DIP SW2 – Pin-Assignment – Overview**

Switch #	Function
1-3	Reserved
4	Enable 125MHz Ref-Clk
5	Enable P2041 mode
6	Enable SATA routing to backplane
7	Enable Fat Pipe crossover
8	Enable fall-back RCW HARD18

4.3.10.1 DIP SW2: Switch 4 – Enable 125MHz Ref-Clk

By operating switch 4 of DIP SW2 the frequency on the CPU SerDes reference clock is changed according to the table below.

Table 15: **DIP SW2: Switch 4 – Enable 125MHz Ref-Clk**

DIP SW2 – Switch 4	Function
	OFF: 100MHz SerDes Reference Clock
	ON: 125MHz SerDes Reference Clock

Default:

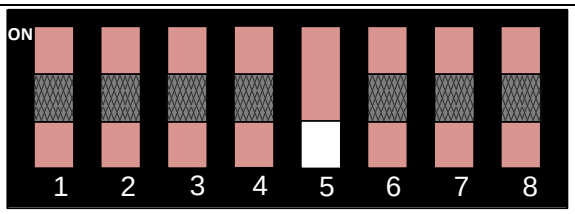
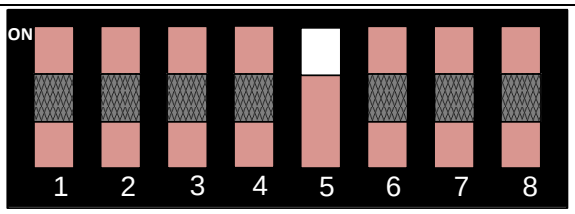
Switch 4 of DIP SW2 is toggled to OFF, SerDes reference clock is 100MHz.

4.3.10.2 DIP SW2: Switch 5 – Enable P2041 mode

Switch 5 of DIP SW2 can be used to enable the P2041 mode for the case a P2041 CPU is assembled instead of a P2040 CPU.

Table 16: **DIP SW2: Switch 5 – Enable P2041 mode**

DIP SW2 – Switch 5	Function

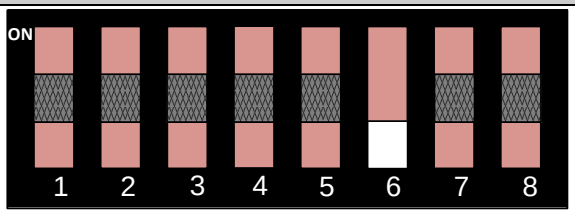
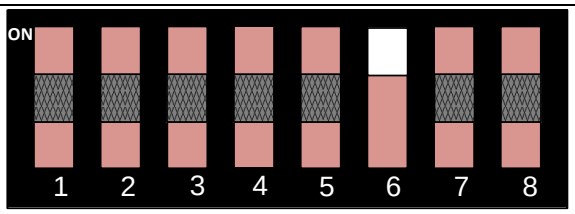
	OFF : P2040 mode
	ON : P2041 mode

Default:
Switch 5 of DIP SW2 is toggled to OFF.

4.3.10.3 DIP SW2: Switch 6 – Enable SATA routing to backplane

Switch 6 of DIP SW2 can be used to configure the onboard SerDes multiplexers that way that the CPU can operate SATA on backplane port 2+3 via its SerDes lanes C+D.

Table 17: **DIP SW2: Switch 6 – Enable SATA routing to backplane**

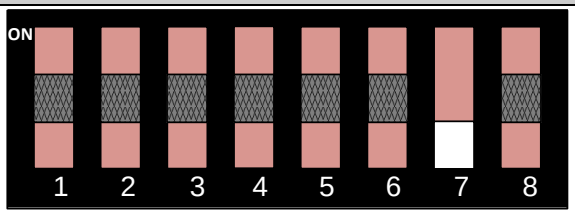
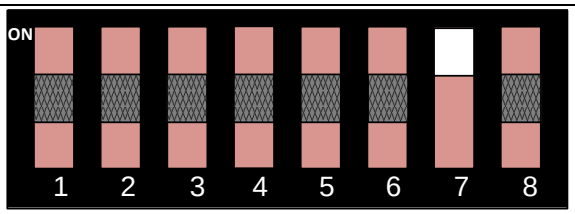
DIP SW2 – Switch 6	Function
	OFF : No SATA on ports 2+3
	ON : CPU SerDes Lanes C+D routed to backplane ports 2+3

Default:
Switch 6 of DIP SW2 is toggled to OFF.

4.3.10.4 DIP SW2: Switch 7 – Enable Fat Pipe crossover

Via switch 7 of DIP SW2 the SerDes Connectivity is changed between backplane ports 4-7 and 8-11.

Table 18: **DIP SW2: Switch 7 – Enable Fat Pipe crossover**

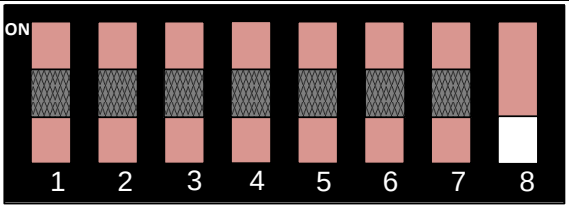
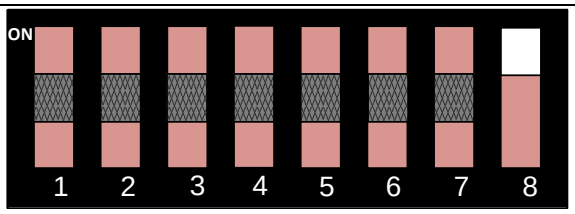
DIP SW2 – Switch 7	Function
	OFF - MUX Mode *Straight:* CPU-Bank *1* is connected to *AMC 4-7* CPU-Bank *2* is connected to *AMC 8-11*
	ON - MUX Mode *Crossover:* CPU-Bank *1* is connected to *AMC 8-11* CPU-Bank *2* is connected to *AMC 4-7*

Default:
Switch 7 of DIP SW2 is toggled to OFF.

4.3.10.5 DIP SW2: Switch 8 – Enable fall-back RCW HARD18

Via switch 8 of DIP SW2 the CPU can be configured to use a hard coded RCW (power-up configuration) instead of fetching it from SPI Flash memory.

Table 19: **DIP SW2: Switch 8 – Enable fall-back RCW HARD18**

DIP SW2 – Switch 8	Function
	OFF : Fetch RCW from SPI Flash memory.
	ON : Use hard coded RCW HARD18.

Default:
Switch 8 of DIP SW2 is toggled to OFF.

5 Programming Notes

5.1 FPGA Register Description 0x000..0x104

Table 20: **FPGA Register Description**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	Reserved								PCB_VERS							
0x002	FPGA_VERS															
0x004	TEST_VAL_1															
0x006	TEST_VAL_2															
0x008	BOARD_ID															
0x00A	ASSBLY_OPT								DIP_SW							
0x010	CARRIER_ID								GEO_ADDRESS							
0x100	RST_SC															
0x102	RST_PERM															
0x104	LED4_CTRL				LED3_CTRL				LED2_CTRL				LED1_CTRL			

5.1.1 0x000 – Reserved / PCB_VERS – Register Description

Table 21: **Register 0x000 – Reserved / PCB_VERS**

Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read Only
7..4	PCB_MAJ_VERS	PCB Major Version (**x**.y) 4 bit unsigned number	HW init	Read Only
3..0	PCB_MIN_VER	PCB Minor Version (x.**y**) 4 bit unsigned number	HW init	Read Only

Note: The PCB Version is determined by the level of unused pins hardcoded on the PCB.

5.1.2 0x002 – FPGA_VERS – Register Description

Table 22: **0x002 – FPGA_VERS**

Bit	Name	Description	Default	Access
15..8	FPGA_SUB_VERS	FPGA Sub Version (x.y.**z**); 8 bit unsigned number	n/a	Read Only
7..4	FPGA_MAJ_VERS	FPGA Major Version (**x**.y.z) 4 bit unsigned number	n/a	Read Only
3..0	FPGA_MIN_VERS	FPGA Minor Version (x.**y**.z) 4 bit unsigned number	n/a	Read Only

5.1.3 0x004 – TEST_VAL_1 – Register Description

Table 23: **0x004 – TEST_VAL_1**

Bit	Name	Description	Default	Access
15..0	TEST_VAL_1	Random number for testing purposes	0xAA55	Read Only

5.1.4 0x006 – TEST_VAL_2 – Register Description

Table 24: **0x006 – TEST_VAL_2**

Bit	Name	Description	Default	Access
15..0	TEST_VAL_2	Random number for testing purposes	0xDEAD	Read Only

5.1.5 0x008 – BOARD_ID – Register Description

Table 25: **0x008 – BOARD_ID**

Bit	Name	Description	Default	Access
15..0	BOARD_ID	Holds the internal Board-ID	0x0B22	Read Only

5.1.6 0x00A – ASSBLY_OPT / DIP_SW – Register Description

Table 26: **0x00A – ASSBLY_OPT / DIP_SW**

Bit	Name	Description	Default	Access
15..12	ASSBLY_OPT_	Reserved	HW init	Read Only
11	ASSBLY_OPT_4	SD-Card	HW init	Read Only
10	ASSBLY_OPT_3	MRAM	HW init	Read Only
9	ASSBLY_OPT_2	Fatpipe MUX	HW init	Read Only
8	ASSBLY_OPT_1	USB	HW init	Read Only
7..0	DIP_SW	Reflects current DIP SW status; switching to ON reads "0"	HW init	Read Only

Register Bits [15..8] reflect the assembly options; "0" means item is present

5.1.7 0x010 – CARRIER_ID / GEO_ADDRESS – Register Description

Table 27: **0x010 – CARRIER_ID / GEO_ADDRESS**

Bit	Name	Description	Default	Access
15..8	CARRIER_ID	Carrier Manager ID 0x80 + 2*Carrier Number	0x00	Read Only
7..0	GEO_ADDRESS	Geographical Address (Slot ID) 0x72: AMC1 0x74: AMC2 0x76: AMC3 0x78: AMC4 0x7A: AMC5 0x7C: AMC6 0x7E: AMC7 0x80: AMC8 0x82: AMC9 0x84: AMC10 0x86: AMC11 0x88: AMC12	na	Read Only

5.1.8 0x100 – RST_SC – Register Description

Table 28: **0x0100 – RST_SC**

Bit	Name	Description	Default	Access
15	BOARD_RS	Board Reset	0	Read/Write
14..8	-	Reserved	0x00	Read/Write
7	ETH_PHY_RES	Ethernet PHY Reset	0	Read/Write
6	-	Reserved	0	Read/Write
5	ETH_CTRL_RES	Ethernet FPGA Logic Reset	0	Read/Write
4..2	-	Reserved	000	Read/Write
1	IPMI_MC_RES	Microcontroller Reset	0	Read/Write
0	-	Reserved	0	Read/Write

All bits in this register are self-clearing.

5.1.9 0x102 – RST_PERM – Register Description

Table 29: **0x0102 – RST_PERM**

Bit	Name	Description	Default	Access
15..8	-	Reserved	0x00	Read/Write
7	ETH_PHY_RES	Ethernet PHY Reset	0	Read/Write
6	-	Reserved	0	Read/Write
5	ETH_CTRL_RES	Ethernet FPGA Logic Reset	0	Read/Write
4..2	-	Reserved	000	Read/Write
1	IPMI_MC_RES	Microcontroller Reset	0	Read/Write
0	-	Reserved	0	Read/Write

All bits in this register hold their value until changed manually.

5.1.100x104 – LED[1..4]_CTRL – Register Description

Table 30: **0x104 – LED[1..4]_CTRL**

Bit	Name	Description	Default	Access
15..12	LED4_CTRL	Each nibble can take one of the following values: 0x0: OFF 0x1: solid green ON 0x2: solid red ON 0x3: green slow BLINK 0x4: red slow BLINK 0x5: green fast BLINK 0x6: red fast BLINK 0x7: green fast double FLASH 0x8: red fast double FLASH 0x9: solid orange ON 0xa: orange slow BLINK 0xb: orange fast BLINK 0xc: orange fast double FLASH 0xd: green/red ALTERNATE slow BLINK 0xe: green/red ALTERNATE fast BLINK 0xf: tbd	0xF	Read/Write
11..8	LED3_CTRL		0xF	Read/Write
7..4	LED2_CTRL		0xF	Read/Write
3..0	LED1_CTRL		0xF	Read/Write

6 Board Specification

Table 31: **NAMC-QorIQ-P204x Specification – Overview**

Processor	P204x based Embedded PowerPC Architecture
AMC-Module	Standard Advanced Mezzanine Card, single width
Front-I/O	2x RJ45 Ethernet or 2x 1GbE SFP, USB Type A, RS232 (Mini-USB),
Main Memory	1024 - 4096 MByte DDR3 SDRAM
FLASH PROM	128 – 1024 MB NAND Flash 32 – 128 MB NOR Flash
Firmware	OK1, QNX BSP and LINUX BSP (on request)
Power Consumption (P2041 / 1.5 GHz)	12V, 2.5A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG AMC.2 Rev. 1.0 (Type E2) PCI Express Base Specification Rev. 1.1 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAMC-QorIQ-P204x** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-QorIQ-P204x** read this installation section
- Before installing or uninstalling the **NAMC-QorIQ-P204x**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-QorIQ-P204x** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary
    - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-QorIQ-P204x** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires only:

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-QorIQ-P204x**
- power supply
- cooling devices

7.2.2 Power supply

The power supply for the **NAMC-QorIQ-P204x** must meet the following specifications:

- required for the module: +12V / 2.5A max.

7.2.3 Automatic Power Up

In the following situations the **NAMC-QorIQ-P204x** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
- when +12V voltage level drops below 10V
- when +3.3V voltage level drops below 3.00V
- The carrier board / backplane signals a PCIe-Reset.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] P2040RM Reference Manual, Rev. 3
[2] LatticeECP3 Family Data Sheet DS1021 Version 02.6EA, March 2014

Appendix B: Document's History

Revision	Date	Description	Author
1.0	11.09.2013	initial release	se
1.1	22.01.2014 13.02.2014	Registers 0x0A/0x10 update Minor changes	se
	07.04.2014	Reworked Chapter 3.9 "I²C-Devices and IPMB"	se
	21.05.2014	Reworked Table 1: Abbreviations Update chapter 7.3 RoHS-Directive / REACH Update chapter 5.1 Register Descriptions	se
1.2	26.11.2014	Added photo (Figure 1)	se
1.2	23.06.2016	Modified DIP-Switch documentation to reflect state of current implementation	te