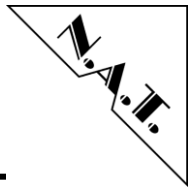
NAMC-ODSP-W
AMC Module
Technical Reference Manual V1.0
HW Revision 1.x



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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*. Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
3G / 5G	3rd / 5th generation wireless systems
AMC	Advanced Mezzanine Card
ARM	Processor Architecture with reduced instruction set
CPRI	Common Public Radio Interface
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
DPD	Digital Pre-Distortion
DSP	Digital Signal Processor
ECI	Ethernet Control Interface
EEPROM	Electrically Erasable PROM
FLASH	Non-Volatile Memory
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GPO	General Purpose Output
GPS	Global Positioning System
HS	Hot Swap
I²C	Inter-Integrated Circuit
I/O	Input / Output
IPMB	Intelligent Platform Management Bus
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MIMO	Multiple-Input and Multiple-Output
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PHY	Physical Layer Device
PROM	Programmable Read-Only Memory
PIF	Parallel Interface
PLL	Phase Locked Loop
Rx	Receiver
R/W	Read/Write
RAM	Random Access Memory
RF	Radio Frequency
SD-Card	Secure Digital Memory Card
SDRAM	Synchronous Dynamic RAM
SerDes	Serializer/Deserializer
SRAM	Static RAM

Abbreviation	Description
SRIO	Serial Rapid I/O
SoC	System On A Chip
SPI (FLASH)	Serial Peripheral Interface (FLASH)
TCKL	Telecom Clock
Tx	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

The **NAMC-ODSP-W** is aimed at LTE, LTE Advanced and 5G systems that require MIMO technologies and enables complete RF to Layer 3 wireless basestation functionality to be implemented on a compact, single-wide AdvancedMC module.

Combining four RF channels with DSP, FPGA and ARM based processing, this module includes a comprehensive range of software including a Linux operating system, L2/L3 stack, virtualized core network software and software defined radio PHY firmware.

A GPS antenna input on the front panel connects to GPS receiver circuitry for GPS clock synchronization. The front panel also features a control connector for an external power amplifier.
The standard variant of the **NAMC-ODSP-W** comes in combination with the daughter board **NMEZ-RF-AD9361**, which features dual AD9361 RF-SoC devices, so two channels of any cellular standard can run independently from each other.

The following figure shows a photo of the **NAMC-ODSP-W** with attached mezzanine board**.**

Figure 1: NAMC-ODSP-W with attached NMEZ-RF-AD9361

2 Overview

2.1 Major Features

- Two OCT2224W DSPs
- Xilinx Kintex-7 XC7k160T FPGA
- Two NXP LS1043A CPUs
- Memory
- Four RF-Interfaces via two AD9361 RF-SoCs
- Broadcom BCM5396
- On-board GPS receiver circuitry
- Control connector to external power amplifier
- Supports up to
  - 20 km range for all cellular standards
  - 130/50 Mbps LTE throughput
  - 64 3G users

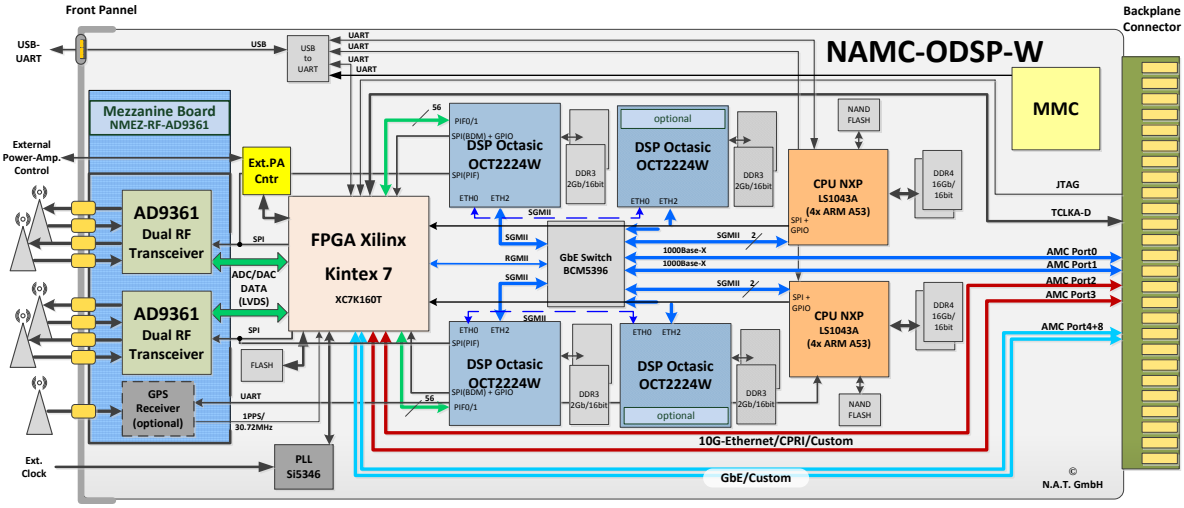
2.2 Applications

- LTE
- LTE Advanced
- 5G Network testing
- MIMO and Massive MIMO Applications

2.3 Block Diagram

The following figure shows a detailed block diagram of the **NAMC-ODSP-W** and the daughter board **NMEZ-RF-AD9361**.

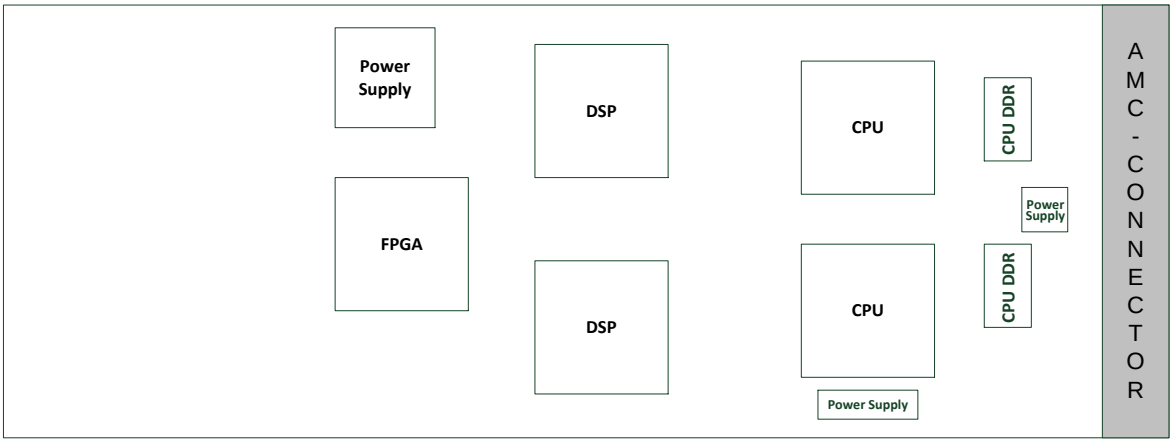
Figure 2: NAMC-OSDP-W and NMEZ-RF-AD9361 – Block Diagram



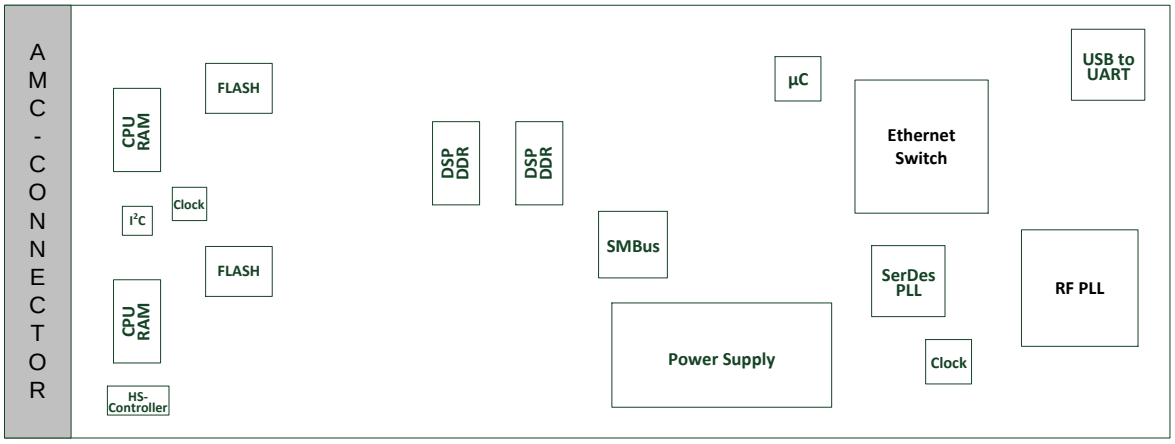
2.4 Location Diagrams

The following figures show detailed location diagrams of the **NAMC-ODSP-W** baseboard and the **NMEZ-RF-AD9361** mezzanine board.

Figure 3: NAMC-ODSP-W – Location Diagram

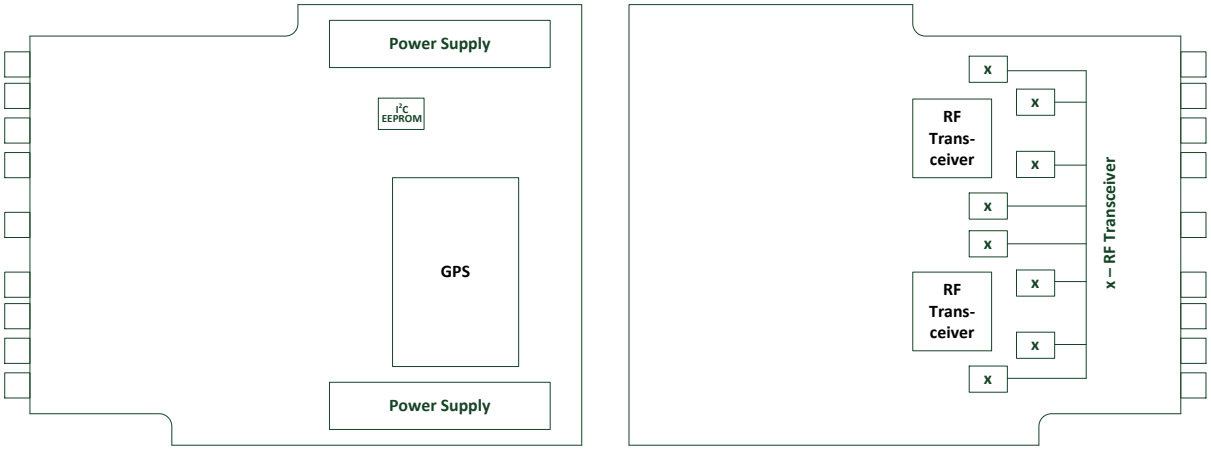


Top View



Bottom View

Figure 4: NMEZ-RF-AD9361 – Location Diagram



3 Board Features

The **NAMC-ODSP-W** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 DSP

The **NAMC-ODSP-W** is equipped with two Octasic OCT2224W DPSs, each with 24 cores, providing the specialized power needed for PHY processing. Each DSP is equipped with its own private external memory.

The DSPs connect to the FPGA by a dual 12-Bit PIF-Interface, parallel control and GPO signals.

For further information, please refer to Appendix A: Reference Documentation.

3.2 FPGA

The Xilinx Kintex-7 FPGA provides pre-DSP data manipulation while also giving headroom for further extension and customization. This includes efficient linearization, i.e. using a signal digital pre-distortion (DPD) per user instead of per power amplifier, and other data pre-processing capabilities.

The FPGA interacts with the CPUs via Ethernet, a SPI-Bus, and parallel I/Os. Further SerDes-Interfaces are connected to the backplane (AMC-Ports 0-4 and 8).

For further information, please refer to Appendix A: Reference Documentation.

3.3 CPU

The **NAMC-ODSP-W** features two NXP QorIQ LS1043A processors for L2/L3 and core processing. These quad-core 64-bit ARM-based processors are each supported by DDR4 memory and feature dedicated data path acceleration architecture.

For further information, please refer to Appendix A: Reference Documentation.

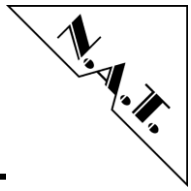
3.4 Memory

3.4.1 DSP-Memory

Each DSP connects to two 16-bit wide DDR3 memory slots with 512 MB own private external memory.

3.4.2 FPGA-memory

The FPGA features 256 Mbit internal SRAM and is supported by an external FLASH PROM.



3.4.3 CPU – Memory

Both QorIQ-CPUs are equipped with an external NAND FLASH PROM (up to 1024 MB) and 4GB 32bit wide DDR4 SDRAM. A MicroSD-Card interface is supported for development and lab-use.

3.5 RF-Interface (located on NMEZ-RF-AD9361)

The **NAMC-ODSP-W** features two Analog Devices AD9361 RF-SoCs located on the **NMEZ-RF-AD9361** mezzanine board, which offer four Rx and Tx antennas operating between 70MHz and 6GHz with up to 56MHz analogue bandwidth. As the RF-Interface is implemented on the mezzanine module, it can easily be adapted to new technologies or different RF frontends.

Both RF-SoCs connect to the FPGA via a dual 12-Bit data interface and a SPI-based configuration and register interface towards the FPGA or the DSPs. They receive a CLK-OUT from the FPGA and a low jitter reference clock from the PLL.

For further information, please refer to Appendix A: Reference Documentation.

3.6 Switching

A Broadcom BCM5396 device establishes a full-non-blocking Ethernet interconnect between the DSPs, CPUs, FPGA, and backplane. Furthermore it provides an individual data and control path access to these devices.

For further information, please refer to Appendix A: Reference Documentation.

3.7 GPS (located on NMEZ-RF-AD9361)

The **NAMC-ODSP-W** is equipped with an UBLOX LEA-M8F-0 GPS-Receiver located on the daughter board **NMEZ-RF-AD9361** which supports a GPS locked clock and a 1pps output that is connected to the FPGA. Frequency calibration inputs which are connected to the FPGA are supported as well.

For further information, please refer to Appendix A: Reference Documentation.

3.8 Clock

The **NAMC-ODSP-W** offers different clock sources: an on-board Stratum-3 oscillator, a TCLKA-D interface towards the backplane, and a reference clock input (via GPS) at the front panel.

3.9 External Interfaces

3.9.1 Front Panel Connectivity

The **NAMC-ODSP-W** features four antenna interfaces (4x Rx, 4x Tx) and an GPS antenna input which is connected to the on-board GPS circuitry for high precision

clock synchronization via the **NMEZ-RF-AD9361** daughter board, realized as SMP connectors. Beside that, a control connector to an external power amplifier is located on the baseboard.
A micro USB jack offers serial terminal access to both CPU, the IPMI µC and the FPGA.

For LED description, please see 4.2 Front Panel and LEDs.

3.9.2 Backplane Connectivity

The **NAMC-ODSP-W** offers full TCKLA-D connectivity towards the backplane.

Two GbE-Connections can be established between AMC ports 0 and 1 and the Broadcom GbE-Switch. AMC ports 2 and 3 offer CPRI or custom SerDes protocol to the FPGA and AMC ports 4 and 8 feature GbE or custom SerDes protocol connectivity towards the FPGA as well.

4 Hardware

4.1 AMC Port Definition

Table 2: AMC Port Definition

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1/TCLKA	Clocks	Reference Clock 1
	CLK2/TCLKB		Reference Clock 2
	CLK3/FCLKA		Fabric Clock
	0	Common Options Region	1000BaseX Ethernet Channel 0
	1		1000BaseX Ethernet Channel 1
	2		CPRI / Custom Protocol
	3		CPRI / Custom Protocol
	4	Fat Pipes Region	1000BaseX Ethernet / Custom
	5		unassigned
	6		unassigned
	7		unassigned
Extended Connector	8		1000BaseX Ethernet / Custom
	9		unassigned
	10		unassigned
	11		unassigned
	12	Extended Options Region	unassigned
	13		unassigned
	14		unassigned
	15		unassigned
	TCLKC/D		Reference Clock 3/4
	17		unassigned
	18		unassigned
	19		unassigned
	20		unassigned

4.2 Front Panel and LEDs

The **NAMC-ODSP-W** module is equipped with several Status-LEDS. Additionally it features the standard AMC LEDs, with the red and blue LED being controlled by the IPMB-µC and the green and orange one being controlled via FPGA registers.

Figure 5: NAMC-ODSP-W – Front Panel

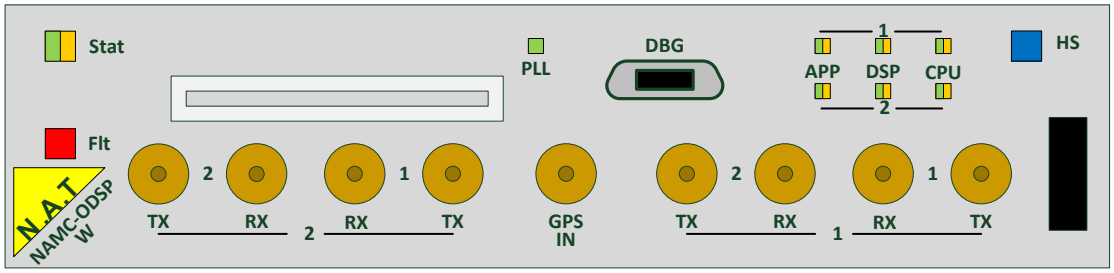


Table 3: NAMC-ODSP-W - LED Functionality

LED	Function	Color
CPU 1/2	CPU Status LED	green / red
DSP 1/2	DSP Status LED	green / red
APP 1/2	Application Status LED	green / red
PLL	PLL Status LED	green
Stat	AMC General Purpose LED	green / yellow
Flt	AMC Fault Indication	red
HS	Hot Swap LED	blue

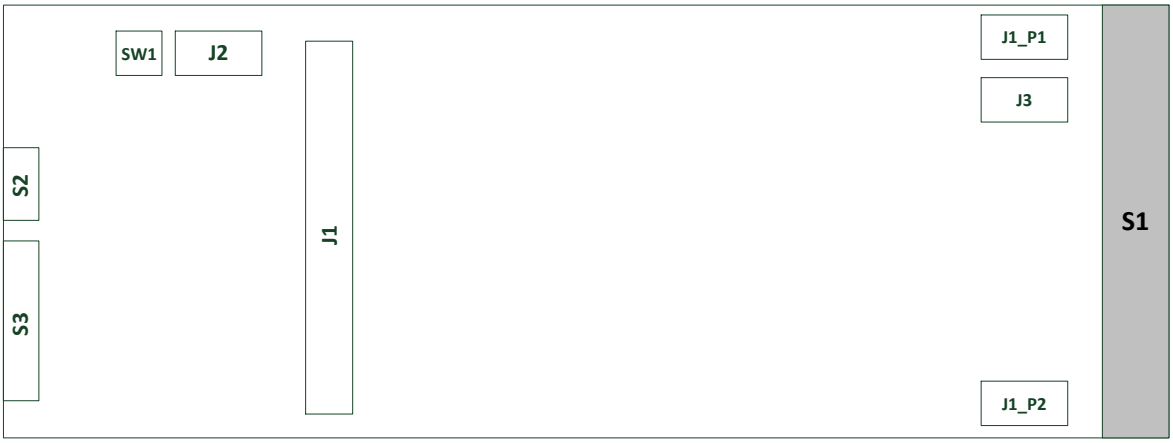
The Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the General Purpose LED physically consists of two LEDs (green and yellow) sharing the same hole in the Front Plate.

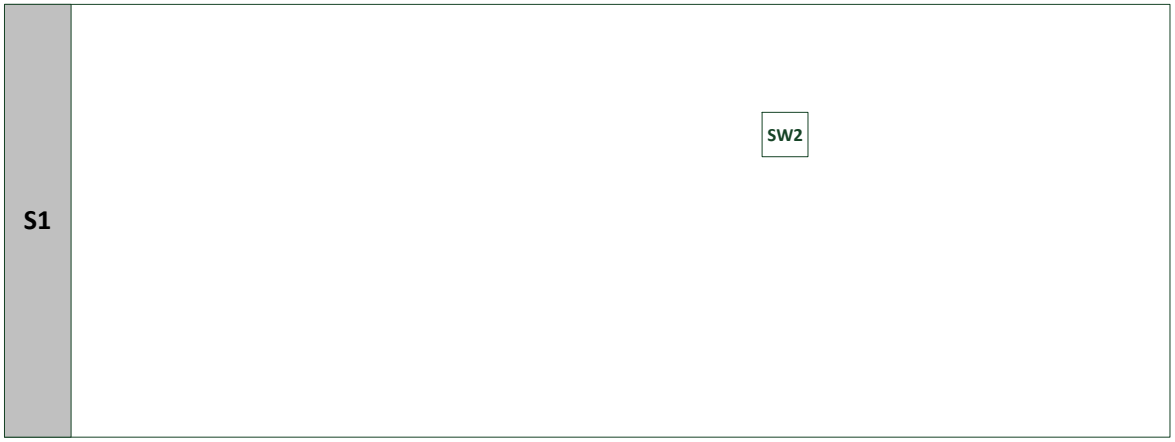
4.3 Connectors and Switches

The following figures show detailed connector and switch diagrams of the **NAMC-ODSP-W** baseboard and the **NMEZ-RF-AD9361** mezzanine board.

Figure 6: NAMC-ODSP-W – Connector and Switch Location – Overview

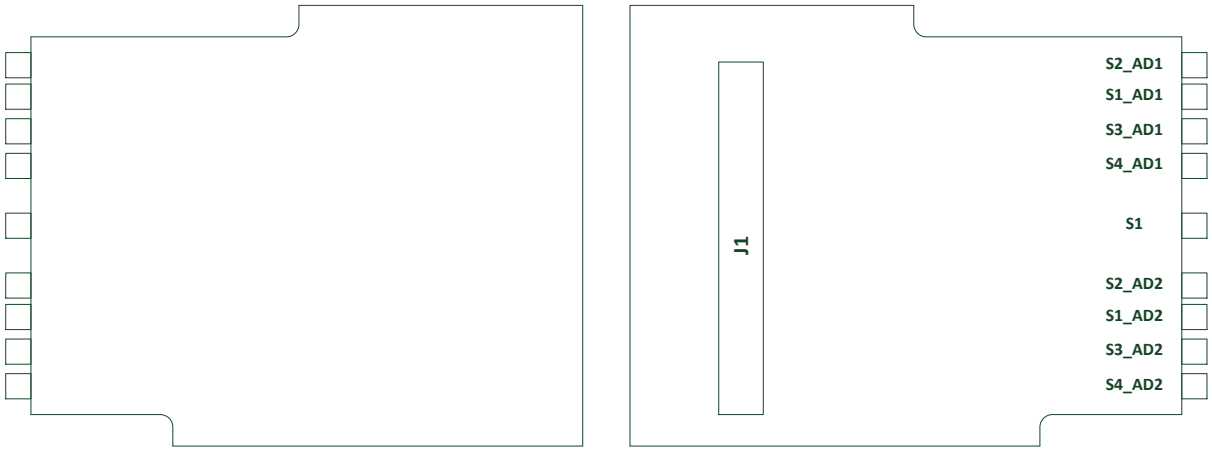


Top View



Bottom View

Figure 7: NMEZ-RF-AD9361 – Connector Location – Overview



Please refer to the following tables to look up the connector pin assignment of the **NAMC-ODSP-W** and the **NMEZ-RF-AD9361**.

4.3.1 S1 (Baseboard) – AMC Connector

Table 4: S1 (Baseboard) – AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	/SPISEL	163
9	PWR	SPICLK	162
10	GND	GND	161
11	XLINK1_P	SPIMOSI	160
12	XLINK1_N	SPIMISO	159
13	GND	GND	158
14	RLINK1_P	PORT19TX_P	157
15	RLINK1_N	PORT19TX_N	156
16	GND	GND	155
17	GA1	PORT19RX_P	154
18	PWR	PORT19RX_N	153
19	GND	GND	152
20	XLINK2_P	PORT18TX_P	151
21	XLINK2_N	PORT18TX_N	150
22	GND	GND	149
23	RLINK2_P	PORT18RX_P	148
24	RLINK2_N	PORT18RX_N	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128

Pin #	AMC-Signal	AMC-Signal	Pin #
44	PET0_P_P4	RESVD	127
45	PET0_N_P4	TDM_REF	126
46	GND	GND	125
47	PER0_P_P4	TDM_FS	124
48	PER0_N_P4	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	PER1_P	TDM5	118
54	PER1_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	CLK_1_P	NC	97
75	CLK_1_N	NC	96
76	GND	GND	95
77	CLK_2_P	NC	94
78	CLK_2_N	NC	93
79	GND	GND	92
80	CLK_3_P	PET0_P_P8	91
81	CLK_3_N	PET0_N_P8	90
82	GND	GND	89
83	/PS0	PER0_P_P8	88
84	PWR	PER0_N_P8	87
85	GND	GND	86

4.3.2 S1 (Mezzanine) – GPS Connector

S1 features a GPS antenna input to the GPS receiver circuitry for GPS clock synchronization.

Table 5: S1 (Mezzanine) – GPS Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GPS_RF_SIG	GND	2
3	GND	-	-

4.3.3 S1-4_AD1 – RF Connectors

S1-4_AD1 connect the RF-Channels of RF-Transceiver 1 to the front plate.

4.3.4 S1-4_AD2 – RF Connectors

S1-4_AD2 connect the RF-Channels of RF-Transceiver 2 to the front plate.

4.3.5 S2 – Debug Connector

S2 offers a serial interface (UART) via USB-Connector towards the front panel for debugging purpose.

Table 6: S2 – Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC	D-	2
3	D+	ID	4
5	GND	GND	6
7	GND	GND	8
9	GND	GND	10
11	GND	-	-

4.3.6 S3 – External PA Connector

Connector S3 features an option to attach an external power amplifier.

Table 7: S3 – External PA Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SCL_CPU1	SDA_CPU1	2
3	RF_CTRL_IN0_DSP1_3V3	RF_CTRL_IN1_DSP1_3V3	4
5	RF_CTRL_IN2_DSP1_3V3	SOM_INT_PA1	6
7	CLK_PA1	GND	8
9	SCL_CPU2	SDA_CPU2	10
11	RF_CTRL_IN0_DSP2_3V3	RF_CTRL_IN1_DSP2_3V3	12

13	RF_CTRL_IN2_DSP2_3V3	SOM_INT_PA2	14
15	CLK_PA2	GND	16
17	PA_3V3	-	-

4.3.7 J1_P1/P2 – CPU Programming Header

Connector J1_P1/P2 connects to the programming-port CPU 1 and 2.

Table 8: J1_P1/P2 – CPU Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	+3.3V	SD_CLK_CPU	2
3	SD_DAT0_CPU	SD_DAT1_CPU	4
5	SD_DAT2_CPU	SD_DAT3_CPU	6
7	SD_CMD_CPU	GND	8

4.3.8 J1 (Baseboard/Mezzanine) – Baseboard-/Mezzanine-Board Connector

J1 connects the **NAMC-ODSP-W** baseboard to the **NMEZ-RF-AD9361** mezzanine board.

Table 9: J1 A/B (Baseboard/Mezzanine)– Baseboard-/Mezzanine-Board Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	AD1_RX_D4_P	AD1_RX_D2_P	B1
A2	AD1_RX_D4_N	AD1_RX_D2_N	B2
A3	GND	GND	B3
A4	AD1_RX_D5_P	AD1_RX_D3_P	B4
A5	AD1_RX_D5_N	AD1_RX_D3_N	B5
A6	GND	GND	B6
A7	AD1_TX_FRAME_N	AD1_FB_CLK_N	B7
A8	AD1_TX_FRAME_P	AD1_FB_CLK_P	B8
A9	GND	GND	B9
A10	AD1_TX_D5_P	AD1_TX_D4_N	B10
A11	AD_TX_D5_N	AD1_TX_D4_P	B11
A12	GND	GND	B12
A13	AD1_SPI_MOSI	CLK_OUT_AD1	B13
A14	AD1_SPI_ENn	GND	B14
A15	PIPF_SPI_MISO_DSP1	AD1_SPI_CLK	B15
A16	AD1_GPO0	AD1_GPO1	B16
A17	AD1_ENABLE	AD1_EN_AGC	B17
A18	GPS_CLK_OUT	RESETB_AD1	B18
A19	GPS_FREQ_IN0 (TP7)	GPS_1PPS	B19
A20	GPS_RxD	GPS_TxD	B20
A21	AD2_SPI_CLK	AD2_SPI_MOSI	B21
A22	GPS_FREQ_IN1 (TP8)	RESETB_AD2	B22
A23	AD_GPO3	AD2_GPO2	B23
A24	GND	GND	B24
A25	+3.3V	CLK_OUT_AD2	B25
A26	GND	GND	B26
A27	AD2_RX_D4_P	AD2_RX_D2_P	B27
A28	AD2_RX_D4_N	AD2_RX_D2_N	B28
A29	AD2_RX_D5_P	AD2_RX_D3_P	B29
A30	AD2_RX_D5_N	AD2_RX_D3_N	B30
A31	GND	GND	B31
A32	AD2_TX_FRAME_N	AD2_FB_CLK_N	B32
A33	AD2_TX_FRAME_P	AD2_FB_CLK_P	B33
A34	GND	GND	B34
A35	AD2_TX_D5_P	AD2_TX_D4_N	B35
A36	AD2_TX_D5_N	AD2_TX_D4_P	B36
A37	GND	GND	B37
A38	+V-VAR	AD2_ENABLE	B38
A39	+V-VAR	AD2_EN_AGC	B39
A40	+V-VAR	GND	B40

Table 10: J1 A/B – Connector to RF-Board – Pin Assignment

Pin #	Signal	Signal	Pin #
C1	AD1_RX_D1_N	AD1_RX_D0_N	D1
C2	AD1_RX_D1_P	AD1_RX_D0_P	D2
C3	GND	GND	D3
C4	AD1_DATA_CLK_P	AD1_RX_FRAME_P	D4
C5	AD1_DATA_CLK_N	AD1_RX_FRAME_N	D5
C6	GND	GND	D6
C7	AD1_TX_D1_N	AD1_TX_D0_N	D7
C8	AD1_TX_D1_P	AD1_TX_D0_P	D8
C9	AD1_TX_D3_N	AD1_TX_D2_N	D9
C10	AD1_TX_D3_P	AD1_TX_D2_P	D10
C11	GND	GND	D11
C12	GND	REF_CLK_AD1	D12
C13	GND	GND	D13
C14	AD1_CTRL_IN3	AD1_CTRL_IN2	D14
C15	AD1_CTRL_IN1	AD1_CTRL_IN0	D15
C16	AD1_GPO2	AD1_GPO3	D16
C17	AD1_SYNC_IN	AD1_TXNRX	D17
C18	MISC-CON1_AD1	MISC-CON0_AD1	D18
C19	SMB_ALERTn	SDA_INT	D19
C20	GPS_RSTn	SCL_INT	D20
C21	AD2_SPI_ENn	PIF_SPI_MISO_DSP2	D21
C22	MISC-CON1_AD2	MISC-CON0_AD2	D22
C23	AD2_GPO1	AD2_GPO0	D23
C24	GND	GND	D24
C25	GND	REF_CLK_AD2	D25
C26	GND	GND	D26
C27	AD2_RX_D1_N	AD2_RX_D0_N	D27
C28	AD2_RX_D1_P	AD2_RX_D0_P	D28
C29	GND	GND	D29
C30	AD2_DATA_CLK_P	AD2_RX_FRAME_P	D30
C31	AD2_DATA_CLK_N	AD2_RX_FRAME_N	D31
C32	GND	GND	D32
C33	AD2_TX_D1_N	AD2_TX_D0_N	D33
C34	AD2_TX_D1_P	AD2_TX_D0_P	D34
C35	AD2_TX_D3_N	AD2_TX_D2_N	D35
C36	AD2_TX_D3_P	AD2_TX_D2_P	D36
C37	GND	GND	D37
C38	AD2_CTRL_IN3	AD2_CTRL_IN2	D38
C39	AD2_CTRL_IN1	AD2_CTRL_IN0	D39
C40	AD2_TXNRX	AD2_SYNC_IN	D40

4.3.9 J2 – Atmel Programming Header

Connector J3 connects to the programming-port of the Atmel µC device.

Table 11: J3 – Atmel Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V_MP	2
3	PDI_CLK	GND	4
5	MMC_RXD	MMC_TXD	6

4.3.10 J3 – JTAG Header

Connector J3 is used as JTAG header.

Table 12: J3 – JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	+1.8V	JTAG_TRSTn_COP	2
3	JTAG_TDI_COP	JTAG_TDO_COP	4
5	JTAG_TMS_COP	JTAG_TCK_COP	6
7	JTAG_CPU_SEL	DEBUG_DETn	8

4.3.11 SW1 – Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

4.3.12 DIP SW2 – tbd

The function of DIP SW2 is tbd.

Table 13: DIP SW2 – Pin-Assignment – Overview

Switch #	Function
1	tbd
2	tbd
3	tbd
4	tbd
5	tbd
6	tbd

5 NAMC-ODSP-W Programming Notes

The FPGA on the **NAMC-ODPS-W** implements various logical blocks. The table below shows the memory map for the logical sub-blocks of the design. Refer to the following sub-chapters for detailed information.
All devices shown in this memory map can be accessed via SPI. This Interface uses a N.A.T. proprietary protocol based on a structure consisting of command/address/data to perform memory mapped accesses via SPI.

Table 14: FPGA Memory Map

Address Offset	Logical Block
0x00	General Purpose Status
0x200	Eth-Switch MDIO Access

Table 15: FPGA Register Description – Overview

General Purpose	
0x00	PCB_VERS
0x01	FPGA_VERS
0x02	DEV_VERS
0x03	FUNC_TYPE
0x04	BOARD_ID[15..8]
0x05	BOARD_ID[7..0]
0x06	SN_LSB
0x07	SN_MSB
0x08	RESET_CPU_1
0x09	RESET_CPU_2
0x0A	RESET
0x0B	SPI_CNTR
0x0C	LED_CPU_1
0x0D	LED_CPU_2
0x0E	LED_APP_1
0x0F	LED_APP_2
0x10	LED_DSP_1
0x11	LED_DSP_2
0x12	LED_AMC
0x13	LED_PLL

Eth-Switch MDIO Access	
0x18	MC_INFO_0
0x19	MC_INFO_1
0x1A	MC_INFO_2
0x1B	MC_INFO_3
0x1C	MC_INFO_4
0x1D	MC_INFO_5
0x1E	MC_INFO_6
0x1F	MC_INFO_7
0x200	MDIO_TX
0x201	MDIO_TX
0x202	MDIO_TX
0x203	MDIO_TX
0x210	MDIO_RX
0x211	MDIO_RX
0x212	MDIO_RX
0x213	MDIO_RX

5.1 General Purpose

5.1.1 0x00 – PCB_VERS

Bit	Name	Description	Default	Access
7..0	PCB_VERS	PCB version determined by level of unused pins hardcoded on PCB	HW init	Read Only

5.1.2 0x01 – FPGA_VERS

Bit	Name	Description	Default	Access
7..0	FPGA_VERS	FPGA version	na	Read Only

5.1.3 0x02 – DEV_VERS

This read-only register can be used by the device driver to probe register access.

Bit	Name	Description	Default	Access
7..0	DEV_VERS	FPGA Subversion during development	na	Read Only

5.1.4 0x03 – FUNC_TYPE

Bit	Name	Description	Default	Access
7..0	FUNC_TYPE	FUNC_TYPE	na	Read Only

5.1.5 0x04 – BOARD_ID[15..8]

Bit	Name	Description	Default	Access
7..0	BOARD_ID[15..8]	holds BOARD_ID MSB	0x0b	Read Only

5.1.6 0x05 – BOARD_ID[7..0]

Bit	Name	Description	Default	Access
7..0	BOARD_ID[7..0]	holds BOARD_ID LSB	0x46	Read Only

5.1.7 0x06 – SN_LSB

Bit	Name	Description	Default	Access
7..0	SN_LSB	SN_LSB	na	Read Only

5.1.8 0x07 – SN_MSB

Bit	Name	Description	Default	Access
7..0	SN_MSB	MSB	na	Read Only

5.1.9 0x08 – RESET_CPU_1

Bit	Name	Description	Default	Access
7..1	tbd	tbd	tbd	Read/Write
0	RESET_CPU_1	Resets CPU 1	0x0	Read/Write

5.1.10 0x09 – RESET_CPU_2

Bit	Name	Description	Default	Access
7..1	tbd	tbd	tbd	Read/Write
0	RESET_CPU_2	Resets CPU 2	0x0	Read/Write

5.1.11 0x0A – RESET

Bit	Name	Description	Default	Access
7	DSP_S2_RST	Resets DSP_S2	0x0	Read/Write
6	DSP_S1_RST	Resets DSP_S1	0x0	Read/Write
5	DSP_P2_RST	Resets DSP_P2	0x0	Read/Write
4	DSP_P1_RST	Resets DSP_P1	0x0	Read/Write
3	AD2_RST	Resets AD_2	0x0	Read/Write
2	AD1_RST	Resets AD_1	0x0	Read/Write
1	SW_RST	Resets SW	0x0	Read/Write
0	BOARD_RST	Resets board	0x0	Read/Write

5.1.12 0x0B – SPI_CNTR

Bit	Name	Description	Default	Access
7..5	tbd	tbd	tbd	Read/Write
4	DSP2_ACC_SEL	tbd	0x0	Read/Write
3	DSP1_ACC_SEL	tbd	0x0	Read/Write
2	CPU_MSTR_SEL	tbd	0x0	Read/Write
1	PLL_SPI2CPU_EN	tbd	0x0	Read/Write
0	AD_SPI2CPU_EN	tbd	0x0	Read/Write

5.1.13 0x0C – LED_CPU_1

Bit	Name	Description	Default	Access
7..0	LED_CPU_1	holds LED_CPU_1 value, see table LED-Values	0x0	Read/Write

5.1.14 0x0D – LED_CPU_2

Bit	Name	Description	Default	Access
7..0	LED_CPU_2	holds LED_CPU_2 value, see table LED-Values	0x0	Read/Write

5.1.15 0x0E – LED_APP_1

Bit	Name	Description	Default	Access
7..0	LED_APP_1	holds LED_APP_1 value, see table LED-Values	0x0	Read/Write

5.1.16 0x0F – LED_APP_2

Bit	Name	Description	Default	Access
7..0	LED_APP_2	holds LED_APP_2 value, see table LED-Values	0x0	Read/Write

5.1.17 0x10 – LED_DSP_1

Bit	Name	Description	Default	Access
7..0	LED_DSP_1	holds LED_DSP_1 value, see table LED-Values	0x0	Read/Write

5.1.18 0x11 – LED_DSP_2

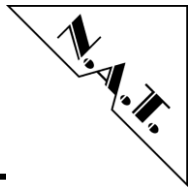
Bit	Name	Description	Default	Access
7..0	LED_DSP_2	holds LED_DSP_2 value, see table LED-Values	0x0	Read/Write

5.1.19 0x12 – LED_AMC

Bit	Name	Description	Default	Access
7..0	LED_AMC	holds LED_AMC value, see table LED-Values	0x0	Read/Write

5.1.20 0x13 – LED_PLL

Bit	Name	Description	Default	Access
7..0	LED_PLL	holds LED_PLL value, see table LED-Values	0x0	Read/Write



5.1.21 LED-Values

LED Values	
0x0	OFF
0x1	green on
0x2	red on
0x3	green slow blink
0x4	red slow blink
0x5	green fast blink
0x6	red fast blink
0x7	green fast double flashing (error)
0x8	red fast double flashing (error)
0x9	orange (green and red) ON
0xa	orange (green and red) slow blink
0xb	orange (green and red) fast blink
0xc	orange (green and red) double flashing (error)
0xd	green and red alternate slow blink
0xe	green and red alternate fast blink
0xf	green gps_1pps

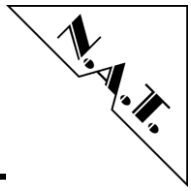
5.2 Eth-Switch MDIO Access

5.2.1 0x18 – MC_INFO_0

Bit	Name	Description	Default	Access
7..0	MC_INFO_0	MC_INFO_0	na	Read Only

5.2.2 0x19 – MC_INFO_1

Bit	Name	Description	Default	Access
7..0	MC_INFO_1	MC_INFO_1	na	Read Only



5.2.3 0x1A – MC_INFO_2

Bit	Name	Description	Default	Access
7..0	MC_INFO_2	MC_INFO_2	na	Read Only

5.2.4 0x1B – MC_INFO_3

Bit	Name	Description	Default	Access
7..0	MC_INFO_3	MC_INFO_3	na	Read Only

5.2.5 0x1C – MC_INFO_4

Bit	Name	Description	Default	Access
7..0	MC_INFO_4	MC_INFO_4	na	Read Only

5.2.6 0x1D – MC_INFO_5

Bit	Name	Description	Default	Access
7..0	MC_INFO_5	MC_INFO_5	na	Read Only

5.2.7 0x1E – MC_INFO_6

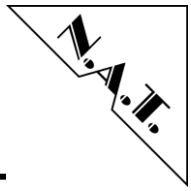
Bit	Name	Description	Default	Access
7..0	MC_INFO_6	MC_INFO_6	na	Read Only

5.2.8 0x1F – MC_INFO_7

Bit	Name	Description	Default	Access
7..0	MC_INFO_7	MC_INFO_7	na	Read Only

5.2.9 0x200 – MDIO_TX

Bit	Name	Description	Default	Access
7..0	MDIO_TX	mdio_cmd_reg(7 downto 0)	0x00	Read/Write



5.2.10 0x201 – MDIO_TX

Bit	Name	Description	Default	Access
7..0	MDIO_TX	mdio_cmd_reg(15 downto 8)	0x00	Read/Write

5.2.11 0x202 – MDIO_TX

Bit	Name	Description	Default	Access
7..0	MDIO_TX	mdio_cmd_reg(23 downto 16)	0x00	Read/Write

5.2.12 0x203 – MDIO_TX

Bit	Name	Description	Default	Access
7..0	MDIO_TX	mdio_cmd_reg(31 downto 24); bit 31 transmitted first – bit 0 last	0x00	Read/Write

5.2.13 0x210 – MDIO_RX

Bit	Name	Description	Default	Access
7..0	MDIO_RX	mdio_rx_reg(7 downto 0)	0x00	Read Only

5.2.14 0x211 – MDIO_RX

Bit	Name	Description	Default	Access
7..0	MDIO_RX	mdio_rx_reg(15 downto 8)	0x00	Read Only

5.2.15 0x212 – MDIO_RX

Bit	Name	Description	Default	Access
7..0	MDIO_RX	mdio_rx_reg(23 downto 16)	0x00	Read Only

5.2.16 0x213 – MDIO_RX

Bit	Name	Description	Default	Access
7..0	MDIO_RX	mdio_rx_reg(31 downto 24)	0x00	Read Only

6 Board Specification

Table 16: NAMC-ODSP-W Features – Overview

DSP	2x Octasic OCT2224M
FPGA	XILINX Kintex-7 XC7K160T
CPU	2x NXP QorIQ LS1043A
AMC-Module	Standard Advanced Mezzanine Card single width, mid-size
Front-I/O	4x SMP Rx, 4x SMP Tx connectors GPS antenna RF SMP connector Control connector to external power amplifier
Power Consumption	12V / 3A
Operating Temperature	0°C – +60°C with forced air cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh at +55°C (non-condensing)
Standards compliance	AMC.0 Rev. 2.0, AMC.2, IMPI V1.5 & V2.0, HPM.1 CE, RoHS, EN61000, EN5022, EN55024

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAMC-ODSP-W** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-ODSP-W** read this installation section
- Before installing or uninstalling the **NAMC-ODSP-W**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-ODSP-W** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-ODSP-W** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

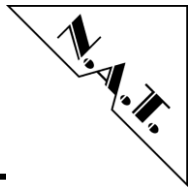
The installation requires only
- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-ODSP-W**
- power supply
- cooling devices

7.2.2 Power supply

The power supply for the **NAMC-ODSP-W** must meet the following specifications:
- required for the module:
  - +12V / 3A max.
  - + 3,3V / 0.15A max.

7.2.3 Automatic Power Up

In the following situations the **NAMC-ODSP-W** will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.



7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Octasic OCT2224W DSP,
Product Brief oct2200wpb2000 1.04 2016-02-22
[2] Xilinx Kintex-7 XC7k160T FPGA,
Product Brief
[3] NXP LS1043A CPU,
Fact Sheet LS1043AFS REV 6
[4] Broadcom BCM5396 16-GE Port Switch with integrated SerDes,
Product Brief 5396-PB01-R 04/18/06
[5] Analog Devices AD9361 RF Agile Transceiver,
Datasheet Rev.F
[6] u-blox LEA-M8F M8 time & frequency reference GNSS module,
Datasheet UBX-14001772 - R06

Appendix B: Document's History

Revision	Date	Description	Author
1.0	20.03.2018	initial release	se