NAMC-ECAT
AMC EtherCAT Slave Module
Technical Reference Manual V1.1
HW Revision 1.1

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	Byte
AMC	Advanced Mezzanine Card
ASIC	Application Specific Integrated Circuit
CPU	Central Processing Unit
EPU	EtherCAT Processing Unit
ESC	EhterCAT Slave Controller
EtherCAT	Ethernet for Control Automation Technology
FMMU	Fieldbus Memory Management Unit
FPGA	Field Programmable Gate Array
µTCA	Micro Telecommunications Computing Architecture
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PDI	Process Data Interface
RAM	Random Access Memory
ROM	Read Only Memory

1 Introduction

The **NAMC-ECAT** is an EtherCAT (Ethernet for Control Automation Technology) interface card in AMC (Advanced Mezzanine Card) form factor. The slave card has the task to connect a flexible, scalable and powerful Micro Telecommunications Computing Architecture (µTCA)-System to the high speed EtherCAT fieldbus. Using µTCA as dedicated slave nodes in an EtherCAT network adds a new dimension of intelligent and scalable nodes to this industrial automation network. This requires the utilization of the EtherCAT interface card (NAMC-ECAT).

Key component of the EtherCAT slave card NAMC-ECAT is the ESC (EtherCAT Slave Controller) as Interface between the EtherCAT bus and the user application within the µTCA-system. As ESC the EtherCAT-ASIC ET1100 from Beckhoff Automation is used. The ESC has an 8kByte Dual Port RAM to exchange data between the EtherCAT network and the application.

The NAMC-ECAT is available as a single mid or a single full-size module. Form the point of view of the EtherCAT fieldbus there are two different versions regarding the EtherCAT interfaces. The slave card is available in a two or three port version.

The **NAMC-ECAT** has the following major features implemented on-board:

- Ports: 3/2 x RJ45 EtherCAT interfaces
- RAM [KByte]: 8
- Fieldbus Memory Management Unit (FMMU): 8
- SyncManagers: 8
- Distributed Clocks: 64 bit
- Process Data Interface (PDI): 16/8 bit synchronous µController
- 1 Lane PCI Express Interface Rev. 1.1
- Configuration/Control via PCIe or via EtherCAT

Figure 1 shows a detailed block diagram of the NAMC-ECAT (3 Ports).

Figure 1: NAMC-ECAT Block Diagram (3 Ports)

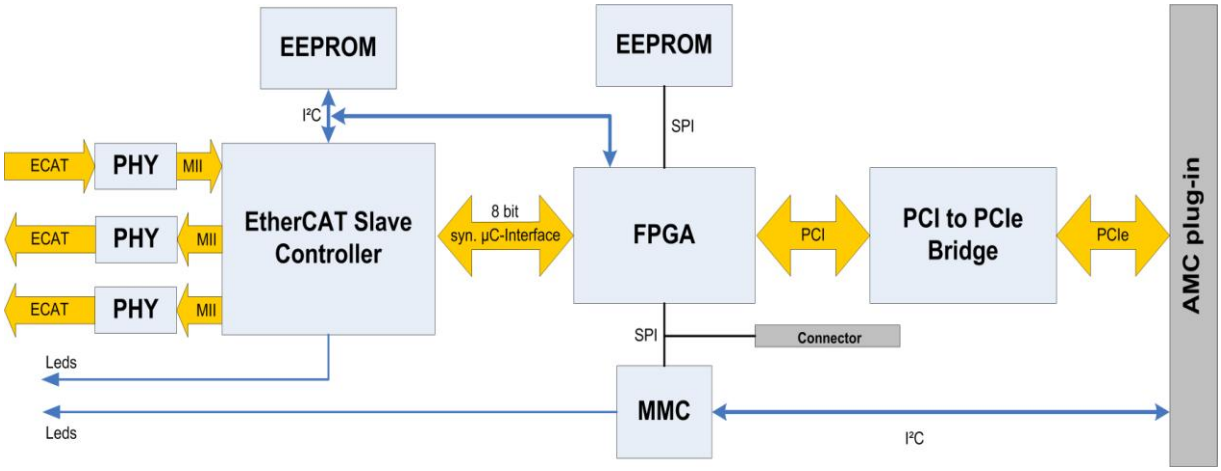
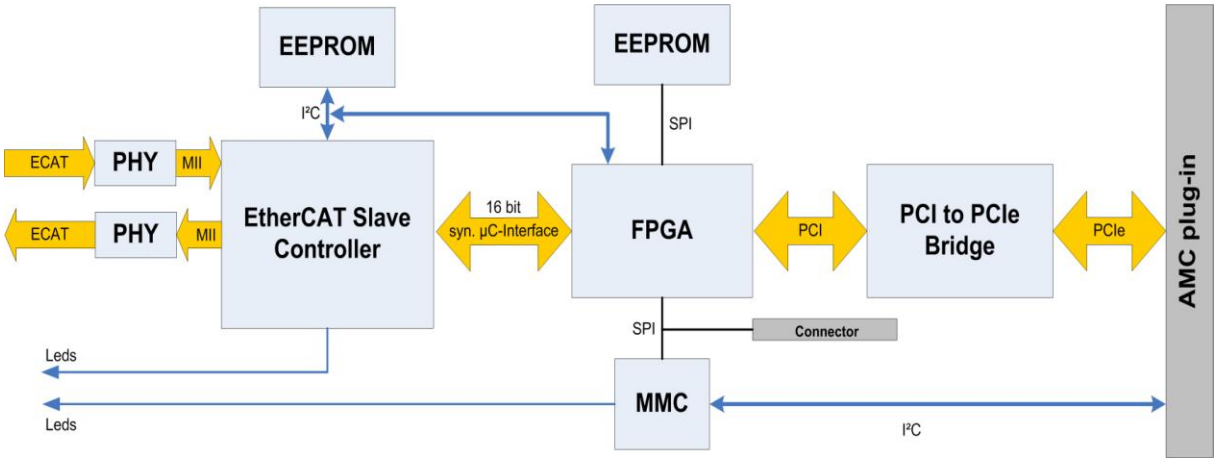


Figure 2 shows a detailed block diagram of the NAMC-ECAT (2 Ports).

Figure 2: NAMC-ECAT Block Diagram (2 Ports)



Board Features

- **EtherCAT Ports**

  There are 2 or 3 EtherCAT interfaces available on the NAMC-ECAT. They are realized by the Ethernet connectors and the PHYs which are connected to the EtherCAT Slave Controller (ESC). For the connection to the AMC based EtherCAT slave card a standard Ethernet patch cable is required.

- **EtherCAT Slave Controller (ESC)**

  The central component on the NAMC-ECAT is the EtherCAT slave controller (ET1100). The ESC is responsible for the EtherCAT communication between the EtherCAT fieldbus and the slave application. The ESC contains the necessary components (e.g. EtherCAT Processing Unit (EPU), FMMU, SyncManager, RAM, etc.) for the data transfer between the fieldbus and the FPGA. Thereby a 16 or 8 bit synchronous µController interface is used (depending on the number of available ports on the NAMC-ECAT).

- **Backplane Interface**

  PCIe: The **NAMC-ECAT** includes a x1-PCI Express interface. This is implemented in a PEX8112 PCI-X to PCIe bridge (PLX). The PCI Express interface connects to Port 4 of the Fat Pipe Region of the AMC backplane connector. The implementation of PCIe conforms to the AMC.1 specification.

  IPMB: The **NAMC-ECAT** implements an IPMB interface which conforms to the AMC.0 specification.

1.1 Board Specification

Table 2: NAMC-ECAT Features

AMC-Module	standard Advanced Mezzanine Card, single width, double height	
Front-I/O	3/2 x RJ45 connectors	
RAM	8 KByte RAM	
Power consumption	3,3V MP 0.1A max	
	12V 0.7A max.	
Environmental conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 1.0	
	PCI Express Base Specification Rev. 1.1	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	IPMI Specification v2.0 Rev. 1.0	
	PICMG µTCA.0 Rev. 1.0	
	ETG.1300 Indicator and Labeling Specification	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NAMC-ECAT** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAMC-ECAT** read this installation section
- Before installing or uninstalling the **NAMC-ECAT**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-ECAT** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-ECAT** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-ECAT**
- power supply
- cooling devices

2.2.2 Power supply

The power supply for the **NAMC-ECAT** must meet the following specifications:

- required for the module:
  +12V / 0.7A max.

2.2.3 Automatic Power Up

In the following situations the **NAMC-ECAT** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +12V voltage level drops below 8V
- when +3.3V voltage level drops below 3.08V

or when the carrier board / backplane signals a PCIe Reset.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

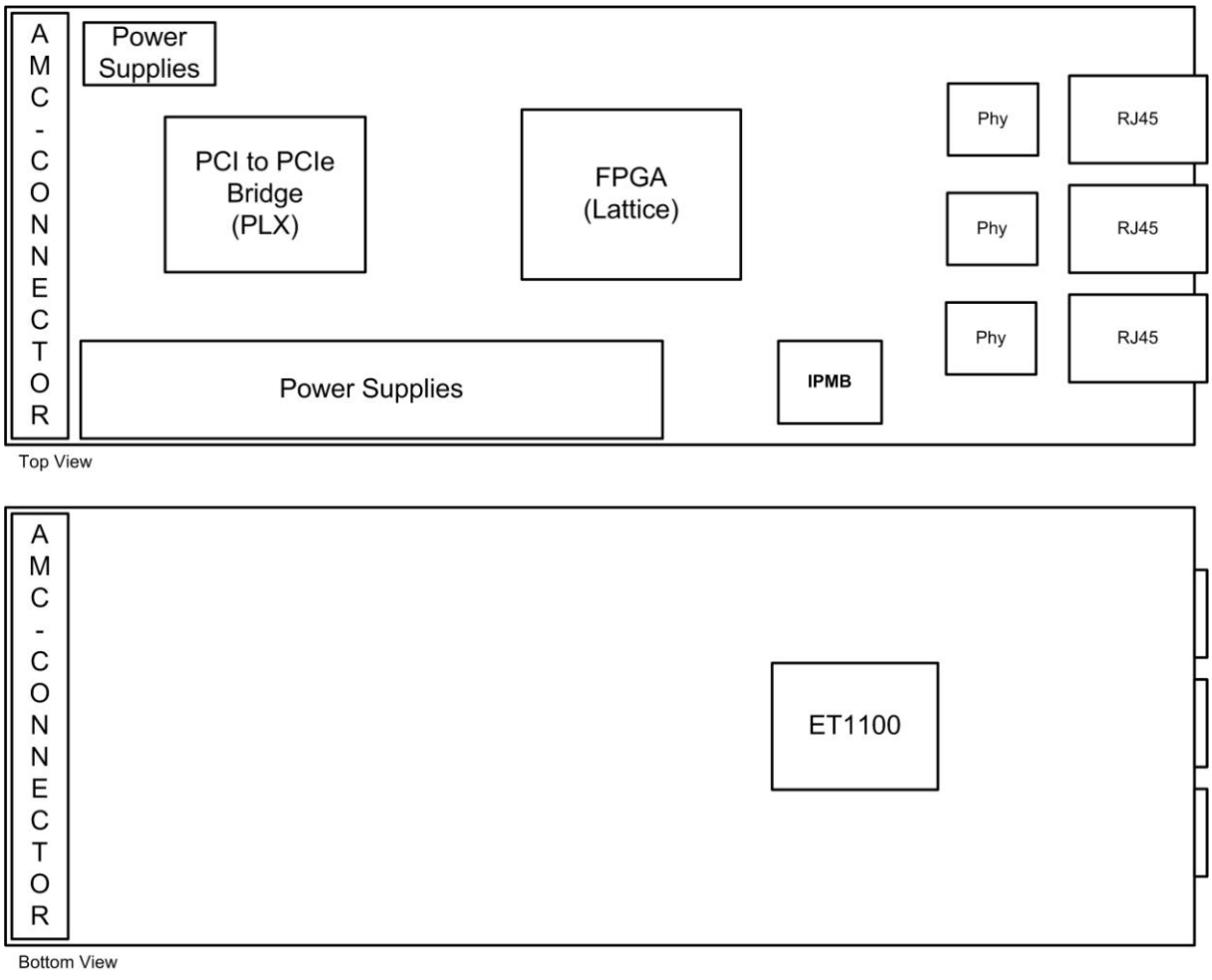
2.3.4 Product Safety

The board complies with EN60950 and UL1950.

2.4 Location Overview

Figure 3 and Figure 4 show the position of important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: Location diagram of the NAMC-ECAT



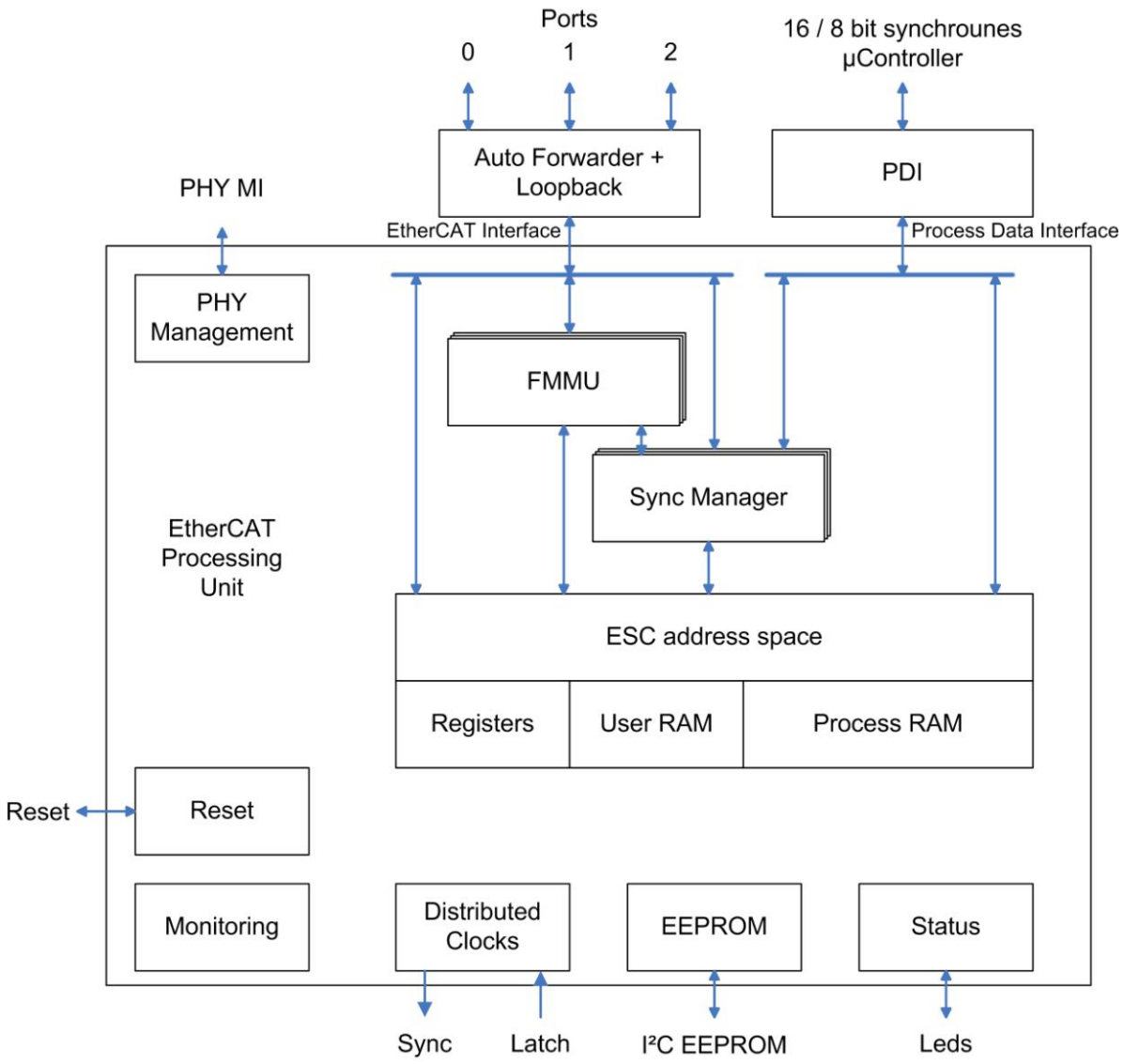
3 Functional Blocks

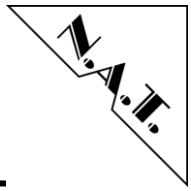
The **NAMC-ECAT** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 EtherCAT Slave Controller (ESC)

The ESC (ET1100) is an ASIC from Beckhoff Automation that process the EtherCAT protocol in the hardware. It offers various possibilities for the configuration and utilization of the available hardware recourses. In figure 3 you can see the block diagram of the ESC and its configuration.

Figure 4: EtherCAT Slave Controller Block Diagram





For more details regarding the EtherCAT Slave Controller, its function, features, properties and the allocation of the ESC address space please consider the ET1100 data sheet.

3.2 FPGA

The FPGA implements the following functional blocks:

- PCI interface for management
- 16/8 bit µController interface

3.3 PCI Express Interface

The **NAMC-ECAT** includes a 1 lane PCI Express interface. This is implemented in a PEX8112 PCI to PCIe bridge (PLX). The PCIe bridge may receive its reference clock either from the Clock 3 port of the AMC backplane connector, or from a local 100 MHz oscillator circuitry (default). The clock source is programmable.

3.4 AMC Clock Interface

AMC backplane clock port Clock 1 is connected to the FPGA, in order to be used as a Telecom standard clock. Clock 1 is only received.

AMC backplane clock port Clock 2 is connected to the FPGA, in order to be used as a Telecom standard reference. Clock 2 may be received from or transmitted to the backplane, in order to become the reference clock for the entire system.

AMC backplane clock port Clock 3 is connected to the PCI → PCIe bridge, in order to be used as a reference clock for PCI Express. Clock 3 is only received. Clock 3 is routed to a multiplexer, which allows programming the clock source of the PCIe line to be either Clock 3, or an internal differential 100 MHz reference clock. In case clock 3 is to be used for a different functionality, it also feeds the FPGA and may be used there for any suitable purpose.

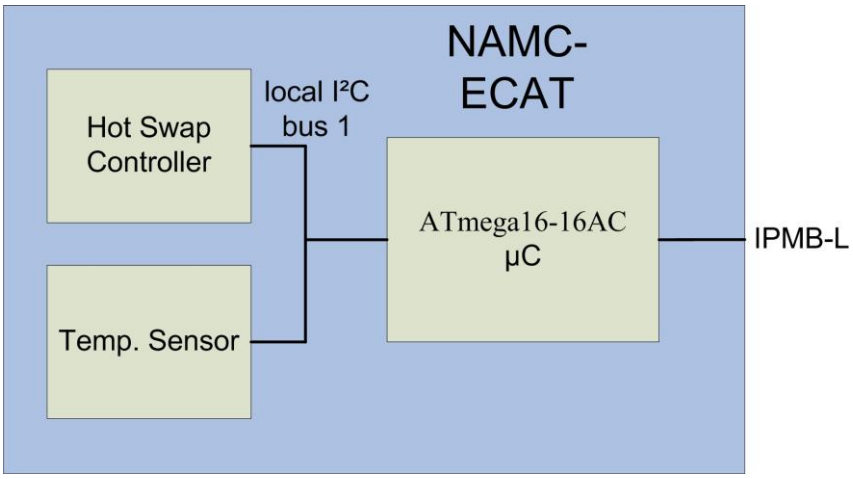
3.5 IPMB Interface

The **NAMC-ECAT** implements an IPMB interface consisting of an ATmega16-16AC microcontroller and a couple of I2C devices, such as a temperature sensor. The IPMB controller manages also the hot swap functionality and the geographical address as requested by the AMC specification.

3.6 I²C Devices

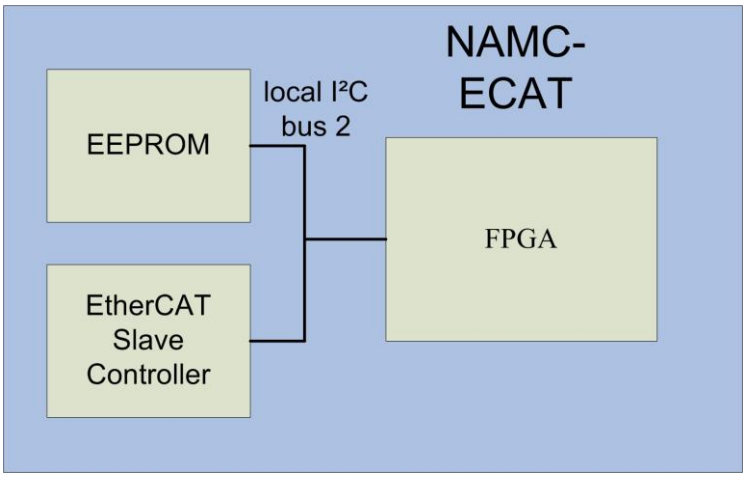
Two I^2C busses connect to the IPMI controller (an ATmega16-16AC microcontroller). The first one is the IPMB bus of the AMC connector. The second I²C bus connects the IPMI controller, the Hot Swap Controller and a temperature sensor. These devices are all powered by IPMB power.

Figure 5: I²C Structure of the NAMC-ECAT (a)



A third I²C bus connects the FPGA and the EEPROM which is necessary for the ESC. The EEPROM can also be accessed via ESC.

Figure 6: I²C Structure of the NAMC-ECAT (b)



3.7 AMC Port Definition

Table 3: AMC Port Definition

	Port No.	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1
	CLK2		Reference Clock 2
	CLK3		Reference Clock 3
	0	Common Options Region	Unassigned
	1		Unassigned
	2		Unassigned
	3		Unassigned
	4	Fat Pipes	PCI Express Lane 0, default
	5		Unassigned
	6		Unassigned
	7		Unassigned
Extended Connector	8	Region	Unassigned
	9		Unassigned
	10		Unassigned
	11		Unassigned
	12	Extended Options Region	Unassigned
	13		Unassigned
	14		Unassigned
	15		Unassigned
	CLK4/5		Reference Clock 4/5
	17		Unassigned
	18		Unassigned
	19		Unassigned
	20		Unassigned

3.8 Front Panel and LEDs

The **NAMC-ECAT** module is equipped with 4 or 6 LEDs (depending on the number of available ports on the NAMC-ECAT). They are integrated in the RJ45 interface jacks.

Additionally the module contains the standard AMC LEDs and a status indicator LED for the EtherCAT bus.

Figure 7: Front Panel (3 Port)

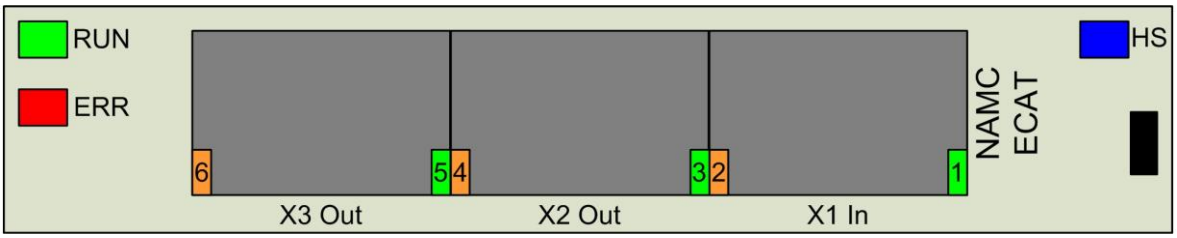
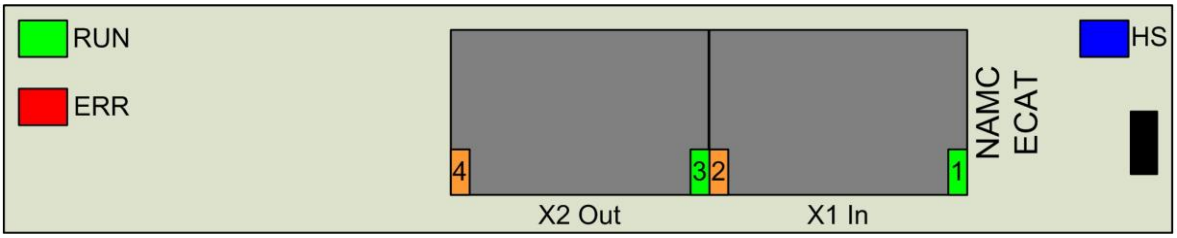


Figure 8: Front Panel (2 Port)



The function of the LEDs is described in the following table:

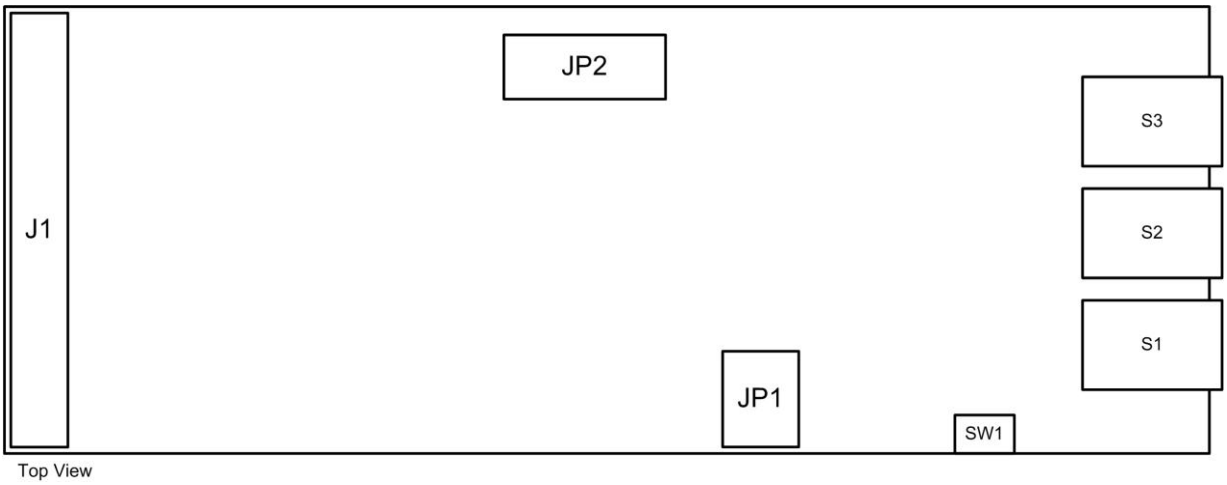
Table 1: LED Functionality

LED	Function
RUN	Status of the EtherCAT State Machine
ERR	AMC Error LED
HS	AMC Hot swap LED
1	Link / Activity LED on port 1
2	port receive error LED on port 1
3	Link / Activity LED on port 2
4	port receive error LED on port 2
5	Link / Activity LED on port 2
6	port receive error LED on port 2

4 Connectors

4.1 Connector Overview

Figure 9: Connectors of the NAMC-ECAT



Please refer to the following tables to look up the connector pin assignment of the **NAMC-ECAT**.

4.2 AMC Connector J1

Table 2: AMC Connector J1

Pin No.	AMC-Signal	AMC-Signal	Pin No.
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	/SPISEL	163
9	PWR	SPICLK	162
10	GND	GND	161
11	XLINK1_P	SPIMOSI	160
12	XLINK1_N	SPIMISO	159
13	GND	GND	158
14	RLINK1_P	PORT19TX_P	157
15	RLINK1_N	PORT19TX_N	156
16	GND	GND	155
17	GA1	PORT19RX_P	154
18	PWR	PORT19RX_N	153
19	GND	GND	152
20	XLINK2_P	PORT18TX_P	151
21	XLINK2_N	PORT18TX_N	150
22	GND	GND	149
23	RLINK2_P	PORT18RX_P	148
24	RLINK2_N	PORT18RX_N	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134

Pin No.	AMC-Signal	AMC-Signal	Pin No.
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PET0_P_P4	RESVD	127
45	PET0_N_P4	TDM_REF	126
46	GND	GND	125
47	PER0_P_P4	TDM_FS	124
48	PER0_N_P4	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	PER1_P	TDM5	118
54	PER1_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	CLK_1_P	NC	97
75	CLK_1_N	NC	96
76	GND	GND	95
77	CLK_2_P	NC	94
78	CLK_2_N	NC	93

Pin No.	AMC-Signal	AMC-Signal	Pin No.
79	GND	GND	92
80	CLK_3_P	PET0_P_P8	91
81	CLK_3_N	PET0_N_P8	90
82	GND	GND	89
83	/PS0	PER0_P_P8	88
84	PWR	PER0_N_P8	87
85	GND	GND	86

4.3 Connector JP1: IPMI-µC Programming Port

Connector JP1 connects the programming-port of the Atmel µC device.

Table 1: Atmel Programming Port

Pin No.	Signal
1	MISO
2	VCC_IPMB
3	SCK
4	MOSI
5	/RST_IMPI
6	GND

4.4 Connector JP2: Lattice FPGA programming port

Connector JP2 connects the JTAG- or programming-port of the Lattice FPGA device.

Table 1: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	+3.3V	TDO	2
3	TDI	/PROGRAM	4
5	nc	TMS	6
7	GND	TCK	8
9	DONE_LAT	/INIT_LAT	10

4.5 Hot Swap Switch SW1

Switch SW1 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

4.6 The Front Panel Connectors (S1 – S3)

4.6.1 The Ethernet Connector S1

Table 2: shows the pin assignment of RJ45-connector S1. This connector carries the 100BaseT signals of the EtherCAT interface.

Table 2: Pin Assignment of the Front-panel Connectors S1 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	TX0+	CT	2
3	TX0-	RX0+	4
5	CT	RX0-	6
7	nc	GND	8
9	LED1_A	LED1_K	10
11	LED2_A	LED2_K	12

4.6.2 The Ethernet Connector S2

Table 2: shows the pin assignment of RJ45-connector S2. This connector carries the 100BaseT signals of the EtherCAT interface.

Table 3: Pin Assignment of the Front-panel Connectors S2 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	TX1+	CT	2
3	TX1-	RX1+	4
5	CT	RX1-	6
7	nc	GND	8
9	LED1_A	LED1_K	10
11	LED2_A	LED2_K	12

4.6.3 The Ethernet Connector S3

Table 2: shows the pin assignment of RJ45-connector S3. This connector carries the 100BaseT signals of the EtherCAT interface.

Table 4: Pin Assignment of the Front-panel Connectors S3 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	TX2+	CT	2
3	TX2-	RX2+	4
5	CT	RX2-	6
7	nc	GND	8
9	LED1_A	LED1_K	10
11	LED2_A	LED2_K	12

5 NAMC-ECAT Programming Notes

The table below shows the memory map for the logical sub-blocks of the design. Refer to the following sub-chapters for detailed information.

Table 1: FPGA Memory Map

Address Offset	Logical Block
0x00000	General Purpose Status (read-only)
0x00100	General Purpose Registers
0x01000	SPI interface to FPGA PROM
0x02000	SPI interface to MMC (Atmel)
0x10000	µC interface to EtherCAT Slave Controller

The FPGA-Design consists of two main blocks:

- Misc. board control- and status registers, and a register-interface to access the FPGA's PROM and the MMC
- µController interface to access the EtherCAT slave controller registers (for configuration and process data exchange)

5.1.1 FPGA GP Registers/Status

This chapter describes the basic board control registers implemented within the FPGA. Further register description will follow up in future versions of this manual.

5.1.1.1 PCB Version Register

The Version Register holds the PCB Revision, encoded in two nibbles.

Table 1: PCB Version Register

PCB Version - Address 0x00			
Default value 0x0011			
Bit	15..8	7..4	3..0
Access	R	R	R
Func	**reserved**	**Version Major**	**Version Minor**

5.1.1.2 FPGA Version Register

The Version Register holds the FPGA Revision, encoded in two nibbles.

Table 1: FPGA Version Register

FPGA Version - Address 0x02			
Default value 0x0010			
Bit	15..8	7..4	3..0
Access	R	R	R
Func	**reserved**	**Version Major**	**Version Minor**

5.1.1.3 FPGA ID_1 Register

This read only register can be used by the device driver to probe register access.

Table 2: FPGA ID_1 Register

FPGA ID_1 - Address 0x04	
Default value 0xAA55	
Bit	15..0
Access	R
Func	**ID_1**

5.1.1.4 FPGA ID_2 Register

This read only register can be used by the device driver to probe register access.

Table 3: FPGA ID_2 Register

FPGA ID_2 - Address 0x06	
Default value 0xDEAD	
Bit	15..0
Access	R
Func	**ID_2**

5.1.1.5 FPGA BOARD_ID Register

This read only register can be used by the device driver to probe register access. It holds the N.A.T. internal board-id of the **NAMC-ECAT.**

Table 4: FPGA BOARD_ID Register

FPGA BOARD_ID - Address 0x08	
Default value 0x0B0f	
Bit	15..0
Access	R
Func	**BOARD_ID**

5.1.1.6 FPGA Reset Register

The Reset Register is used to trigger a reset to the whole FPGA logic, FPGA blocks, or external devices. Writing a '1' to a bit triggers the reset. After reset, the bit is self-cleared to '0'.

Table 5: FPGA Reset Register

Reset – Address Offset 0x100								
Default value 0x0000								
Bit	15	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	**ESC**

5.1.1.7 SPI interface register to FPGA PROM

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further information.

5.1.1.8 SPI interface register to Atmel

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further information.

5.1.1.9 ESC Register

The ESC registers are divided into registers for configuration and control and registers for process data exchange. The start address for the access on the ESC register is 0x10000. The table below shows the memory map. For more information regarding read and write accesses on these registers please consider the ESC data sheet [1].

Table 1: ESC Register

Address Offset	Logical Block
0x10000	Register for ESC configuration and control
0x11000	Register for ESC process data exchange

6 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Beckhoff, ET1100 Hardware Data Sheet, Rev. 1.5
[2] Broadcom, BCM5241 Data Sheet, Document 5241-DS12-R
[3] Atmel, AT24C128/256 Data Sheet, Rev. 0670J-SEEPR-4/1/03
[4] Atmel, Atmega16/16L Product Data, Rev. 2466C-03/02
[5] Lattice, ECP2/M Handbook, Version 04.2
[6] PLX Technology, PEX8112-AA, PCI Express to PCI Bridge, Data Book, Version 1.2

Appendix B: Document's History

Revision	Date	Description	Author
1.0	15.06.2010	initial revision	rm
1.1	17.05.2013	Address, phone and fax updated, words updated	fh