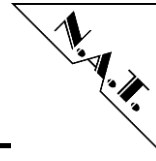


**NAMC-8569-CPU  
CPU AMC Module  
Technical Reference Manual V1.5  
HW Revision 1.0/1.1**

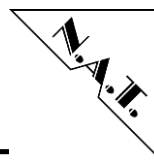


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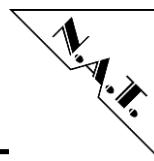
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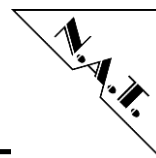
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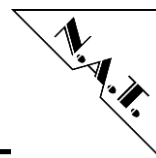


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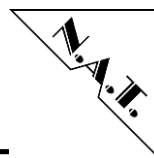
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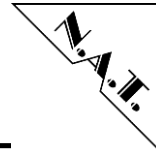
## Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x.

The following table gives a list of the abbreviations used in this document.

**Table 1: List of used abbreviations**

Abbreviation	Description
AMC	Advanced Mezzanine Card
BDM	Background Debug Mode
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
FCLK	Fabric Clock
FPGA	Field Programmable Gate Array
GMII	Gigabit Media Independent Interface
I <sup>2</sup> C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt Request
iTDM	Internal TDM
LSB	Least Significant Bit
μC	Microcontroller
μTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MCC	Memory Chip Controller
MLVDS	Multipoint Low Voltage Differential Signaling
MRAM	Magnetoresistive RAM
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PHY	Physical Layer Device
R/W	Read/Write
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
(P)ROM	(Programmable) Read Only Memory
RTC	Real Time Clock
PLL	Phase Locked Loop
SD-Card	Secure Digital Memory Card
SerDes	Serializer/Deserializer
SRIO	Serial Rapid I/O
TCKL	Telecom Clock
TDM	Time Division Multiplex
TSI	Time Slot Interchanger
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus



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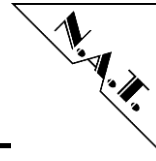
## 1 Introduction

The **NAMC-8569-CPU** is a versatile CPU card in AMC (Advanced Mezzanine Card) form factor. A powerful onboard CPU capable of handling a wide range of processing tasks is surrounded by a comprehensive pool of memory devices and I/O paths. These software based processing resources are extended by FPGA based hardware resources to offer a wide spread of possible applications.

Key component of the **NAMC-8569-CPU** is the MPC8569 CPU. It offers an e500 PowerPC core combined with dedicated interface hardware and four RISC cores.

The **NAMC-8569-CPU** is available as a single compact-, a single mid- or a single full-size module. The full-size version can be equipped with an additional extension board that can be used to add customized I/O functionality to the card.





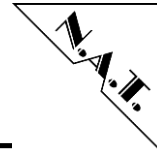
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## 2 Overview

### 2.1 Major Features

- PowerQUICC III MPC8569 based Embedded PowerPC Architecture
- 128 – 1024 MB DDR2 SDRAM at 800MHz as main Memory
- 128 MB NOR Flash
- 2 GB of NAND Flash
- Micro SD-Card slot
- 512kB MRAM (non-volatile SRAM)
- Flexible Fat Pipe Connectivity
- 2 x 10/100/1000-BaseT Front Panel Ethernet
- 2 x Gigabit Backplane Ethernet to AMC Ports 0 / 1
- iTDM Interface
- TDM functionality
- AMC Clock Interface
- I<sup>2</sup>C-Devices and IPMB Interface
- Front Panel I/O - USB / RS232
- IPMB Interface
- Optional: H.110 alike Backplane TSI bus
- Optional: MLVDS I/O via AMC Ports 17-20

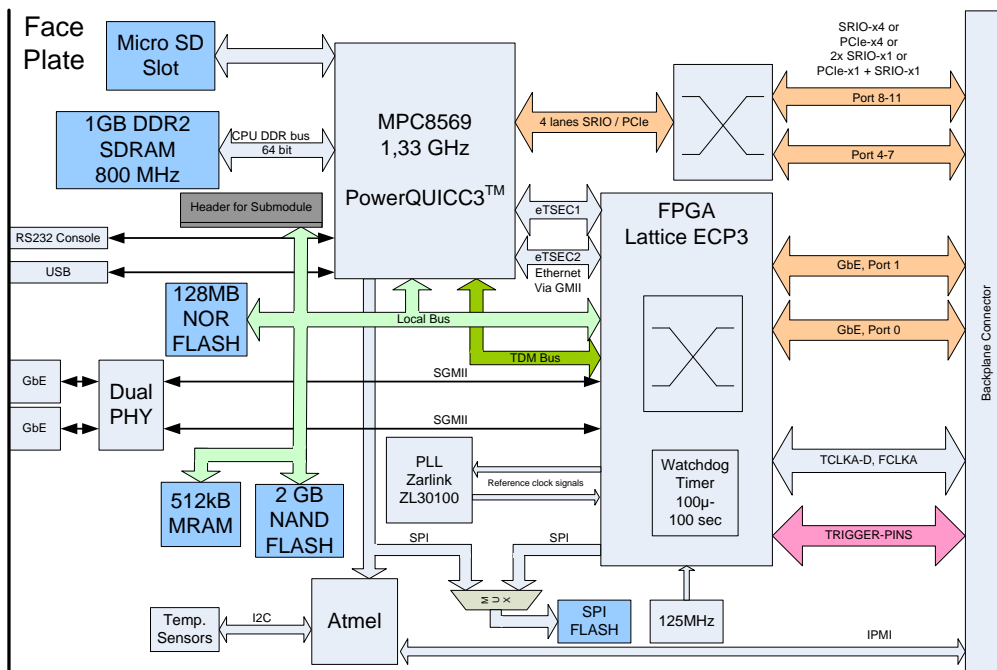
For detailed description see the following chapter.

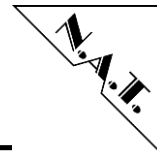


## 2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-8569-CPU**. If the extension module is added (only available for full-size face plate), customized I/O functionality is available.

**Figure 1: NAMC-8569-CPU – Block Diagram Baseboard - Overview**

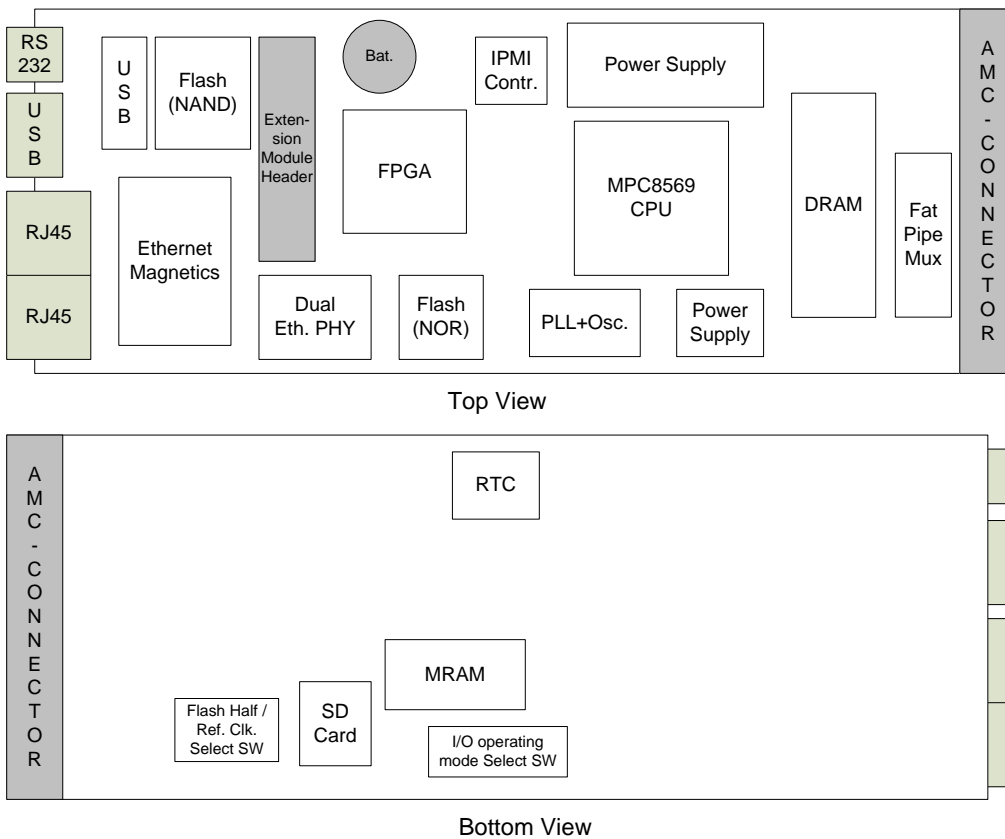


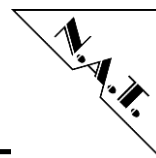


### 2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

**Figure 2: NAMC-8569-CPU – Location Diagram Baseboard - Overview**





---

## 3 Board Features

The **NAMC-8569-CPU** can be divided into a number of functional blocks, which are described in the following paragraphs.

### 3.1 CPU

The MPC8569 PowerQUICC III™ is a versatile communications processor that integrates on one chip a high-performance PowerPC™ microprocessor, a very flexible co-processor unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PowerPC e500™ core with 32 Kbytes of instruction cache and 32 Kbytes of data cache. To this primary cache adds 512 Kbytes of Level 2 cache. The auxiliary co-processor unit consists of four RISC cores and many hardware peripherals making this device a complete system on a chip.

Depending on the assembled CPU the PowerQUICC III runs with a core clock frequency of 800 - 1333 MHz. The QUICCEngine frequency may be set up to 667 MHz (assembly option).

### 3.2 Memory

#### 3.2.1 SDRAM

The onboard DDR2 SDRAM memory is 64 bit wide. Its default size is 512 MB or 128, 256, 1024 MB as assembly option. The interface to the DDR2 SDRAM is implemented in the MPC8569. By programming several registers the DDR2 RAM controller can be adapted to different RAM architectures.

#### 3.2.2 NOR-/NAND-Flash

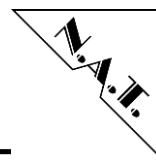
The flash memory on the **NAMC-8569-CPU** is connected to the de-multiplexed upper 16 data bits D0 – 15 and to the latched address lines. De-multiplexing of the local address/data bus of the CPU, as well as address latching, is performed by an FPGA. The flash memory can be programmed by the CPU or through the BDM port. The 16 bit wide Flash PROM provides a capacity of 16 – 128 MB (assembly option). Its default size is 128 MB.

#### 3.2.3 Micro SD-Card Slot

The Micro SD-Card Slot provides an additional non-volatile memory up to 2GB.

#### 3.2.4 MRAM

The non-volatile 512kB MRAM is used for storing data permanently. It can be accessed like an SRAM, without having any limitation in the number of allowed write cycles like known from EEPROM or Flash memories.



### 3.3 Flexible Fat Pipe Connectivity

The MPC8569 CPU offers four bidirectional serial lines (four-line SerDes) that can be operated either as PCIe, SRIO, or a combination of both. In cooperation with an external multiplexing unit the full Fat Pipe Region from Ports 4-11 is made accessible.

#### 3.3.1 PCIe

The **NAMC-8569-CPU** can be configured to implement either an x1 or an x4 PCIe interface. Per default and per AMC specification this interface operates on Ports 4-7 for the x4 and on Port 4 for the x1 configuration. This implementation of PCIe conforms to the AMC.1 specification.

Beyond the specification the board can also be configured to run PCIe on Port 8 (x1 Link) or Port 8-11 (x4 Link).

#### 3.3.2 SRIO

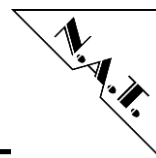
The **NAMC-8569-CPU** can be configured to implement either two x1 or one x4 SRIO interface(s). If configured for two x1 interfaces these operate on Port 4 and Port 8. If configured for one x4 interface this can be selected to operate on Port 4-7 or on Port 8-11. In addition the speed of the SRIO interface(s) can be configured for 1.25Gb/s, 2.5Gb/s or 3.125 Gb/s operation.

#### 3.3.3 PCIe/SRIO

The **NAMC-8569-CPU** can be configured to implement an x1 PCIe interface operating on Port 4 and an SRIO interface operating on Port 8. In this case the speed of the SRIO interface is fixed at 2.5Gb/s

**Table 2: Flexible Fat Pipe Connectivity – Configuration options**

Configuration options							
Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11
PCIe x4				-	-	-	-
-	-	-	-	PCIe x4			
PCIe x1	-	-	-	-	-	-	-
-	-	-	-	PCIe x1	-	-	-
SRIO x4				-	-	-	-
-	-	-	-	SRIO x4			
SRIO x1	-	-	-	SRIO x1	-	-	-
PCIe x1	-	-	-	SRIO x1			



---

## 3.4 Ethernet

The **NAMC-8569-CPU** is equipped with four Gigabit Ethernet paths which can be connected to UEC1/2 Ethernet MAC of the MPC8569 CPU through the iTDM FPGA, and share the port with iTDM. The 1000BaseX physical layer device is realized using the FPGA SerDes units. The default configuration for the Ethernet paths is that UEC1 connects to Front Ethernet 1 and UEC2 connects to Front Ethernet 2.

### 3.4.1 Front Ethernet

On its face plate the **NAMC-8569-CPU** is equipped with two RJ45 jacks, which offer a 10/100/1000-BaseT Ethernet interface each, handled by a Broadcom dual PHY device (BCM5482). The PHY's MAC side interfaces are then further connected to the FPGA. Within here it can be selected whether the CPU's two Ethernet controllers operate via the backplane Ethernet lines, via the front Ethernet ports or use a combination of both. Future FPGA versions could offer application specific switching functionality at this point.

### 3.4.2 Backplane Ethernet

The **NAMC-8569-CPU** implements a so called SerDes Ethernet interface towards the backplane. This path connects to Port 0/1 of the Common Options Region of the AMC backplane connector.

The FPGA internal SerDes Ethernet is connected to the MPC8569's Ethernet MAC through two GMII interfaces, which are fed through the FPGA. It connects to the backplane Ethernet, the physical layer of which is 1000BaseX. Within FPGA logic the CPU Ethernet data is multiplexed with the iTDM data and transferred through the same physical port.

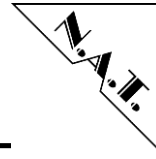
## 3.5 iTDM

The **NAMC-8569-CPU** implements a serial iTDM backplane interface, the physical layer of which is 1000BaseX. The iTDM interface connects to Port 0/1 of the Common Options Region of the AMC backplane connector and shares the ports with the CPU Ethernet path by doing arbitration for iTDM packets and for CPU Ethernet packets to be sent. The iTDM interface is implemented in FPGA logic and conforms to the SFP.0 and SFP.1 specifications.

Main task of the FPGA residing on the **NAMC-8569-CPU** is offering a powerful TDM to iTDM conversion engine to the board. For the on-board chip TDM devices, the FPGA implements TSI functionality. This can be used for directly connecting channels from the line interface of other AMC boards to channels of the MPC8569 MCC controllers. Attached to this TSI are then 1024 bidirectional iTDM channels that can be used for connecting CPU channels to destinations outside the board.

## 3.6 TDM

The **NAMC-8569-CPU** implements an 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz. Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. It bridges to a module – internal TDM bus, which connects



to the MCC ports of the MPC8569 CPU. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Common Options Region of the AMC connector.

### 3.7 AMC Clock Interface

The **NAMC-8569-CPU** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D and FCLKA.

All TCLK ports are connected directly to the FPGA and can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from the line interfaces or to synchronize the **NAMC-8569-CPU** to an external clock.

AMC backplane clock port FCLKA is connected to a multiplexer, which allows programming the clock source of the MPC8569 SerDes reference clock input to be either sourced from FCLKA or an internal differential reference clock.

### 3.8 I<sup>2</sup>C-Devices and IPMB

The **NAMC-8569-CPU** owns several I<sup>2</sup>C-Devices on different busses. Please note that the 7-bit I<sup>2</sup>C-Address is left aligned in the notation below, meaning that in the most-right bit (LSB) the I<sup>2</sup>C R/W bit resides.

#### 3.8.1 CPU Local I<sup>2</sup>C-Bus

Two I<sup>2</sup>C-Devices connect to the MPC8569's local bus:

- AT24C256 – EEPROM used for storage of board-specific information  
– I<sup>2</sup>C-Address: 0xA0
- DS1339 – Real-Time-Clock device – I<sup>2</sup>C-Address: 0xD0

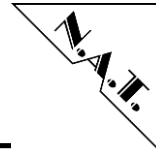
#### 3.8.2 IPMB

To the IPMI-Controller (ATmega1284) connect several I<sup>2</sup>C-Devices:

- LM95241 – Temperature sensor device with two external sensors (for CPU temperature) and one internal sensor – I<sup>2</sup>C-Address: 0x56
- LTC4215 – Hot Swap Controller – I<sup>2</sup>C-Address: 0x96
- IDT8N3Q001 – programmable oscillator – I<sup>2</sup>C-Address :0xDC

Additionally, the IPMB-Bus of the AMC connector is attached to the IPMI-Controller.

The IPMI-Controller manages the geographical address as requested by the AMC specification.



## **3.9 Front Panel I/O**

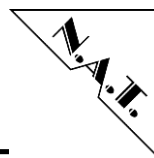
### **3.9.1 USB**

The AMC module features an USB Type A Jack on its face plate which connects to the CPU internal USB controller. It can be used to implement various USB functionality covering both host or device behaviour.

### **3.9.2 RS232**

The RS232 interface is physically presented in a Mini-USB Type B jacket. It is normally used for debugging purpose along with a standard terminal program (default baud rate: 19200).



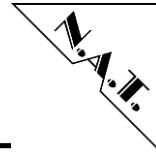


## 4 Hardware

### 4.1 AMC Port Definition

**Table 3: AMC Port Mapping Strategy**

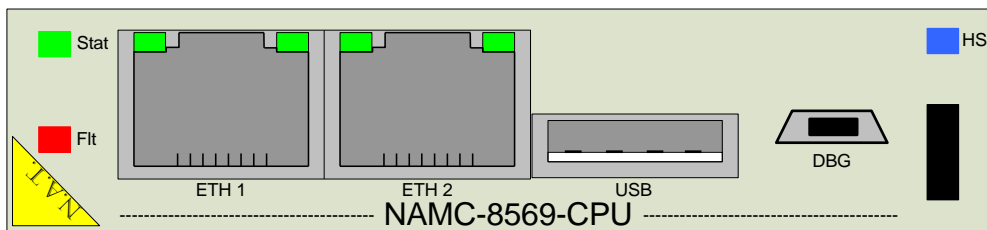
	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and CPU Ethernet), default
	1		1000BaseX Ethernet Channel 2 (iTDM and CPU Ethernet), redundant
	2		Unassigned
	3		Unassigned
	4	Fat Pipes	SerDes Mux Lane 0
5	SerDes Mux Lane 1		
6	SerDes Mux Lane 2		
7	SerDes Mux Lane 3		
Extended Connector	8	Region	SerDes Mux Lane 4
	9		SerDes Mux Lane 5
	10		SerDes Mux Lane 6
	11		SerDes Mux Lane 7
	12	Extended Options Region	TDM Bus D0-3 (H.110 extended)
	13		TDM Bus D4-7 (H.110 extended)
	14		optional clock lines (H.110 extended)/ unassigned
	15		Unassigned
	16		TCLKC / TCLKD
	17		MLVDS I/O (Trigger Signals for xTCA)
	18		MLVDS I/O (Trigger Signals for xTCA)
	19		MLVDS I/O (Trigger Signals for xTCA)
	20	MLVDS I/O (Trigger Signals for xTCA)	



## 4.2 Front Panel and LED

The **NAMC-8569-CPU** module is equipped with 4 bicoloured LEDs integrated in the RJ45 interface jacks. They are driven by the Ethernet PHY and can be programmed to various link indication modes.

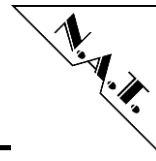
**Figure 3: NAMC-8569-CPU – Front Panel View**



Additionally the module contains the standard AMC LED consisting of a fault indication LED controlled by the IPMI controller and a general purpose status LED controlled by the FPGA/CPU.

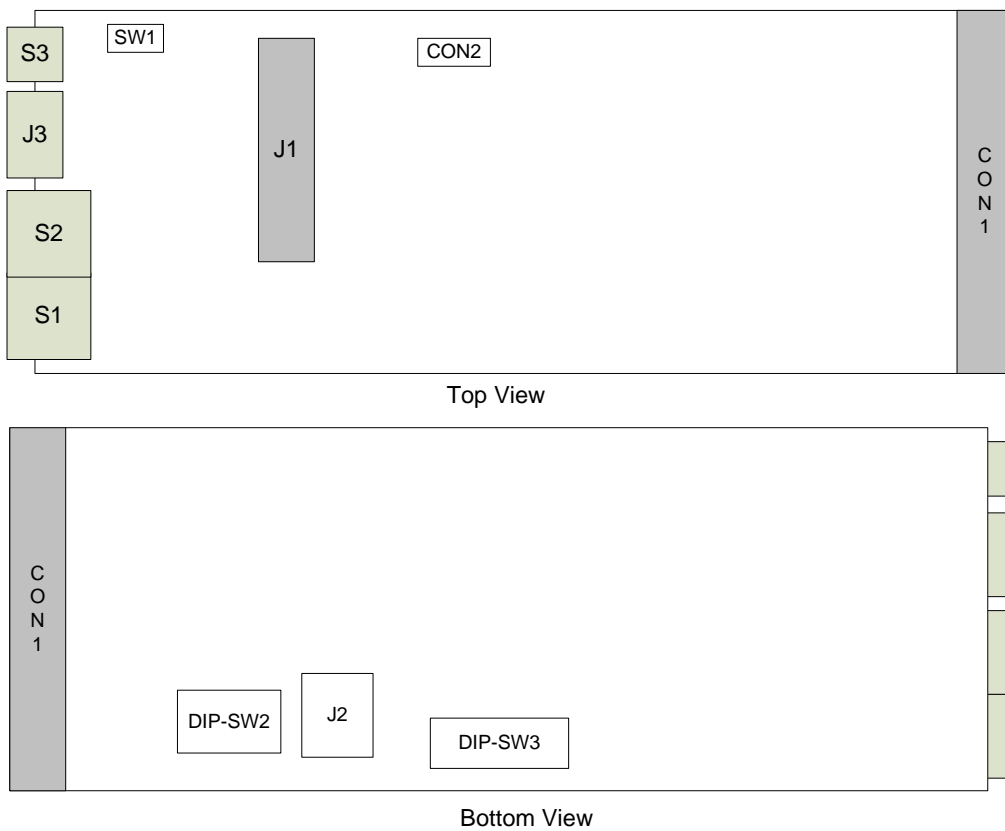
The Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the General Purpose LED physically consists of two LEDs (green and orange) sharing the same hole in the Front Plate. For more information on the behaviour of these LEDs, please refer to chapter 5.2.1.10.

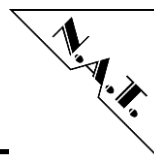


### 4.3 Connectors and Switches

**Figure 4: NAMC-8569-CPU – Connector and Switch Location – Overview**



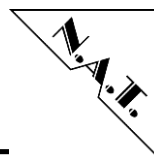
Please refer to the following tables to look up the connector and switch pin assignment of the **NAMC-8569-CPU**.



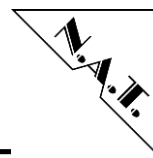
4.3.1 CON1: AMC Connector

Table 4: CON1: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	PORT20_TX_P	163
9	PWR	PORT20_TX_N	162
10	GND	GND	161
11	PORT0_TX_P	PORT20_RX_P	160
12	PORT0_TX_N	PORT20_RX_N	159
13	GND	GND	158
14	PORT0_RX_P	PORT19_TX_P	157
15	PORT0_RX_N	PORT19_TX_N	156
16	GND	GND	155
17	GA1	PORT19_RX_P	154
18	PWR	PORT19_RX_N	153
19	GND	GND	152
20	PORT1_TX_P	PORT18_TX_P	151
21	PORT1_TX_N	PORT18_TX_N	150
22	GND	GND	149
23	PORT1_RX_P	PORT18_RX_P	148
24	PORT1_RX_N	PORT18_RX_N	147
25	GND	GND	146
26	GA2	PORT17_TX_P	145
27	PWR	PORT17_TX_N	144
28	GND	GND	143
29	NC	PORT17_RX_P	142
30	NC	PORT17_RX_N	141
31	GND	GND	140
32	NC	TCLKD_P	139
33	NC	TCLKD_N	138
34	GND	GND	137
35	NC	TCLKC_P	136
36	NC	TCLKC_N	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PORT4_TX_P	RESVD	127



Pin #	AMC-Signal	AMC-Signal	Pin #
45	PORT4_TX_N	TDM_REF	126
46	GND	GND	125
47	PORT4_RX_P	TDM_FS	124
48	PORT4_RX_N	TDM_CLK	123
49	GND	GND	122
50	PORT5_TX_P	TDM7	121
51	PORT5_TX_N	TDM6	120
52	GND	GND	119
53	PORT5_RX_P	TDM5	118
54	PORT5_RX_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	PORT6_TX_P	TDM1	112
60	PORT6_TX_N	TDM0	111
61	GND	GND	110
62	PORT6_RX_P	PORT11_TX_P	109
63	PORT6_RX_N	PORT11_TX_N	108
64	GND	GND	107
65	PORT7_TX_P	PORT11_RX_P	106
66	PORT7_TX_N	PORT11_RX_N	105
67	GND	GND	104
68	PORT7_RX_P	PORT10_TX_P	103
69	PORT7_RX_N	PORT10_TX_N	102
70	GND	GND	101
71	IPMB_SDA	PORT10_RX_P	100
72	PWR	PORT10_RX_N	99
73	GND	GND	98
74	TCLKA_P	PORT9_TX_P	97
75	TCLKA_N	PORT9_TX_N	96
76	GND	GND	95
77	TCLKB_P	PORT9_RX_P	94
78	TCLKB_N	PORT9_RX_N	93
79	GND	GND	92
80	FCLKA_P	PORT8_TX_P	91
81	FCLKA_N	PORT8_TX_N	90
82	GND	GND	89
83	/PS0	PORT8_RX_P	88
84	PWR	PORT8_RX_N	87
85	GND	GND	86



**4.3.2 CON2: RS232 Connector**

The Debug Terminal Connector CON2 offers the option to connect to the UART1 of the MPC8569 CPU to realize a serial terminal interface. This connector can be used as alternative to the front panel connector S3.

**Table 5: CON2: RS232 Connector – Pin-Assignment**

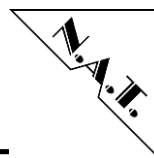
Pin#	Signal	Signal	Pin No.
1	RxDA	GND	2
3	TxDA		

**4.3.3 J1: Extension Module Connector**

Connector J1 connects to an extension module mounted on the NAMC-8569-CPU and is used for initial programming of the board.

**Table 6: J1: Extension Module Connector – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	SGND	+12V	2
3	NC	+12V	4
5	NC	GND	6
7	GND	PS1_PIGGYn	8
9	SCL_INT	SDA_INT	10
11	P_RES2	UPC_TX_ADDR0	12
13	UPC_CLKO	UPC_TX_ADDR1	14
15	FPGA_TDI	UPC_TX_ADDR2	16
17	FPGA_DONE	UPC_TX_ADDR3	18
19	FPGA_TDO	CPU_TDO	20
21	/PROGRAMN	CPU_TDI	22
23	FPGA_TMS	CPU_TCK	24
25	FPGA_TCK	CPU_TMS	26
27	INITN	CPU_/SRESET	28
29	ATMEL_MISO	CPU_/HRESET	30
31	ATMEL_MOSI	/CKSTP_OUT	32
33	ATMEL_SCK	/CKSTP_IN	34
35	/RST_IPMI	UPC_TX_ADDR4	36
37	P_CLK	P_RES1	38
39	P_RES0	UPC_RX_PRTY	40
41	GND	/CPU_TRST	42
43	UPC_RX_ADDR0	UPC_TX_PRTY	44
45	UPC_RX_ADDR1	/LCS6	46
47	UPC_RX_ADDR2	/RST_IPMI_P	48
49	UPC_RX_ADDR3	/LWE1	50
51	UPC_RX_ADDR4	UPC_RX_ENB	52
53	UPC_RX_CLAV0	UPC_TX_ENB	54
55	UPC_TX_CLAV0	UPC_RX_SOC	56
57	UPC_TXD15	UPC_TX_SOC	58
59	GND	GND	60
61	VCC_IPMB	UPC_RXD0	62



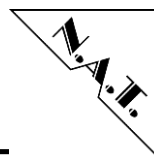
Pin #	Signal	Signal	Pin #
63	GND	UPC_RXD1	64
65	P_/RESET	UPC_RXD2	66
67	P_/INT	UPC_RXD3	68
69	P_/CS	UPC_RXD4	70
71	UPC_TXD0	UPC_RXD5	72
73	UPC_TXD1	UPC_RXD6	74
75	UPC_TXD2	UPC_RXD7	76
77	UPC_TXD3	UPC_RXD8	78
79	UPC_TXD4	UPC_RXD9	80
81	UPC_TXD5	UPC_RXD10	82
83	UPC_TXD6	UPC_RXD11	84
85	UPC_TXD7	UPC_RXD12	86
87	UPC_TXD8	UPC_RXD13	88
89	UPC_TXD9	UPC_RXD14	90
91	UPC_TXD10	UPC_RXD15	92
93	LAD0	UPC_TXD11	94
95	LAD1	/LOE	96
97	LAD2	/LWE0	98
99	LAD3	LA18	100
101	LAD4	LA19	102
103	LAD5	LA20	104
105	LAD6	LA21	106
107	LAD7	LA22	108
109	UPC_TXD12	LA23	110
111	UPC_TXD13	LA24	112
113	UPC_TXD14	LA25	114
115	GND	LA26	116
117	+3.3V	LA27	118
119	+3.3V	GND	120

**4.3.4 J2: Micro SD-Card Slot**

J2 connects directly to the MPC8569 SD-Card interface and offers the option to use Micro SD-Cards as removable Flash Memory on the **NAMC-8569-CPU** board.

**Table 7: J2: Micro SD Card slot – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	SD_DAT2	SD_DAT3	2
3	SD_CMD	+3.3V	4
5	SD_CLK	GND	6
7	SD_DAT0	SD_DAT1	8



**4.3.5 J3: USB Connector**

Connector J3 offer access to the USB interface of the MPC8569 CPU.

**Table 8: J3: USB Front-panel Connector – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	VBUS	USB_D_N	2
3	USB_D_P	GND	4

**4.3.6 S1/S2: RJ45 Ethernet**

Connectors S1 and S2 offer access to a 10/100/1000-BaseT Ethernet interface each.

**Table 9: S1/S2: RJ45 Front-panel Connectors – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	TRD0+	TRD0-	2
3	TRD1+	TRD2+	4
5	TRD2-	TRD1-	6
7	TRD3+	TRD3-	8

**4.3.7 S3: RS232 for Terminal Interface**

Connector S3 offers access to a RS232 interface connected to UART1 of the MPC8569 CPU.

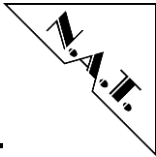
**Table 10: S3: RS232 Front-panel Connector – Pin-Assignment**

Pin #	Signal	Signal	Pin #
1	RTS_SCC1	RxD_SCC1	2
3	TxD_SCC1	CTS_SCC1	4
5	GND		

**4.3.8 SW1: Hot-Swap Switch**

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.





**4.3.9 DIP SW2: Flash Half Select / Reference Clock Select**

The table below gives an overview of the operating parameters configurable via DIP SW2. Details are given in the following subchapters.



**Table 11: DIP SW2 – Pin-Assignment – Overview**

Switch #	Function
1	Flash half select
2	Ref. clock select

**4.3.9.1 DIP SW2: Switch 1 – Boot Flash Select Switch**

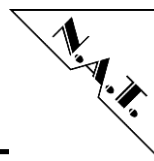
By operating switch 1 of DIP SW2 to ON, the upper half of the Boot Flash is selected for booting. If switch 1 of DIP SW2 is turned to OFF, the lower half of the Boot Flash is selected for booting.

**Table 12: DIP SW2: Switch 1 – Boot Flash Select – Pin-Assignment**

DIP SW2 – Switch 1	Function
	Upper Flash Half, Usually used for OK1
	Lower Flash Half, Usually used for Linux

**Default:**



Switch 1 of DIP SW2 is toggled to OFF; lower half of the Boot Flash is selected for booting.



**4.3.9.2 DIP SW2: Switch 2 – Reference Clock Select Switch**

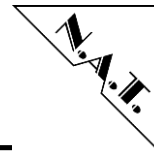
This switch is used to select the source for the MPC8569 SerDes reference clock input. Switching it to ON selects FCLKA as source for this input, setting to OFF selects the board-internal generated reference clock.

**Table 13: DIP SW2: Switch 2 – Reference Clock Select – Pin-Assignment**

DIP SW2 – Switch 2	Function
	FCLKA
	Board-internal

**Default:**

Switch 2 of DIP SW2 is toggled to OFF; board-internal reference clock is used for SerDes.



**4.3.10DIP SW3: I/O operating mode**

The table below gives an overview of the operating parameters configurable via DIP SW3. Details are given in the following subchapters.

**Table 14: DIP SW3 – Pin-Assignment – Overview**

Switch #	Function
1	SerDes Mode
2	
3	
4	
5	PortSel 4-7 / 8-11
6	PCIe RC enable
7	SRIO host enable
8	unassigned

**Please note:**

After changing parameters of DIP SW3, a complete power cycle (including IPMI µC) is required to make the new settings active within E-keying. This is indicated by the orange AMC LED (label Stat) blinking fast, regardless of the register value stated in the respective FPGA register.

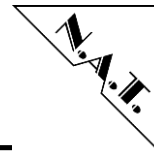
Therefore, after changing DIP SW3 please insert the board once, let power up, then extract it from the backplane to interrupt the management power of the Atmel µC and insert it again. On the first inserting after a DIP switch change it will do E-Keying using the old Fat Pipe configuration, on the second insertion it will use the new configuration for E-keying. The orange AMC LED operates again according to the register value.

**4.3.10.1 DIP SW3: Switches 1-4 – SerDes Mode Select Switch**

By operating switches 1-4 of DIP SW3 one of the SerDes configurations listed in the following table can be selected.

**Table 15: DIP SW3: Switches 1-4 – SerDes Mode Select – Pin-Assignment**

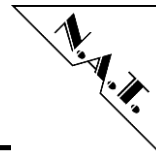
DIP SW3 – Switches 1-4	Function
	PCIe x1
	Redundant SRIO x1; 2.5Gb/s



	<p>Redundant SRIO x1; 1.25Gb/s</p>
	<p>Redundant SRIO x1; 3.125Gb/s</p>
	<p>SRIO x4; 1.25Gb/s</p>
	<p>SRIO x4; 2.5Gb/s</p>
	<p>SRIO x4; 3.125Gb/s</p>
	<p>Port4: PCIe x1 / Port8: SRIO x1</p>
	<p>SerDes disabled</p>
	<p>PCIe x4</p>

**Default:**

Switches 1-4 of DIP SW3 are toggled to OFF, PCIe x4 is selected.



**4.3.10.2 DIP SW3: Switch 5 – Fat Pipe Port Select**

By operating switch 5 of DIP SW3 the active ports within the Fat Pipe Region for the non-redundant operation can be selected.

**Table 16: DIP SW3: Switch 5 – Fat Pipe Port Select – Pin-Assignment**

DIP SW3 – Switch 5	Function
	Operation on Ports 8-11
	Operation on Ports 4-7

**Default:**

Switch 5 of DIP SW3 is toggled to OFF; operation on Ports 4-7 is selected.

**4.3.10.3 DIP SW3: Switch 6 – PCIe Root Complex Select**

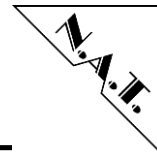
By operating switch 6 of DIP SW3 the CPU can be configured to operate as PCIe root complex or as PCIe end point.

**Table 17: DIP SW3: Switch 6 – PCIe Root Complex Select – Pin-Assignment**

DIP SW3 – Switch 6	Function
	PCIe Root Complex
	PCIe End-Point

**Default:**

Switch 6 of DIP SW3 is turned to OFF, operation as PCIe End-Point is selected.



**4.3.10.4 DIP SW3: Switch 7 – SRIO Host Mode Selection**

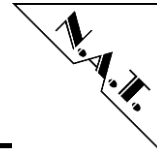
By operating switch 7 of DIP SW3 the CPU can be configured to operate in SRIO Host Mode or as SRIO Agent.

**Table 18: DIP SW3: Switch 7 – SRIO Host Mode Select – Pin-Assignment**

DIP SW3 – Switch 7	Function
	SRIO Host Mode
	SRIO Agent

**Default:**

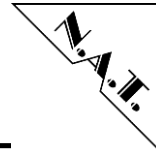
Switch 7 of DIP SW3 is toggled to OFF, operation as SRIO Agent is selected.



### 4.4 CPU Port Pin Definition

**Table 19: CPU Port Pin Definition – Port A**

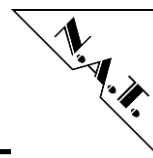
Signal Function	Port A Pin
UCC1_TXD0	PA[0]
UCC1_TXD1	PA[1]
UCC1_TXD2	PA[2]
UCC1_TXD3	PA[3]
UCC1_TX_EN	PA[4]
UCC1_TX_ER	PA[5]
UCC1_RXD0	PA[6]
UCC1_RXD1	PA[7]
UCC1_RXD2	PA[8]
UCC1_RXD3	PA[9]
nc	PA[10]
nc	PA[11]
UCC1_RX_DV	PA[12]
UCC1_RX_ER	PA[13]
UCC2_TXD0	PA[14]
UCC2_TXD1	PA[15]
UCC2_TXD2	PA[16]
UCC2_TXD3	PA[17]
nc	PA[18]
UCC2_TX_ER	PA[19]
UCC2_RXD0	PA[20]
UCC2_RXD1	PA[21]
UCC2_RXD2	PA[22]
UCC2_RXD3	PA[23]
CPU_CON	PA[24]
UCC2_TX_EN	PA[25]
UCC2_RX_DV	PA[26]
UCC2_RX_ER	PA[27]
UCC2_RXD4	PA[28]
nc	PA[29]
nc	PA[30]
UCC1_RXD7	PA[31]



**Table 20: CPU Port Pin Definition – Port B**

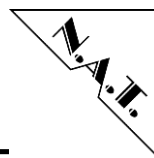
Signal Function	Port B Pin
UCC1_TX_D5	PB[0]
nc	PB[1]
UCC1_RXD6	PB[2]
CPU_DEBUG5	PB[3]
nc	PB[4]
UCC1_TXD7	PB[5]
UCC1_RXD5	PB[6]
UCC1_TXD6	PB[7]
UCC1_TXD4	PA[8]
nc	PB[9]
nc	PB[10]
UCC1_RXD4	PB[11]
UCC4_TXD0	PB[12]
UCC4_TXD1	PB[13]
UUC4_TXD2 / UCC2_RXD7	PB[14]
UCC4_TXD3 / UCC2_TXD5	PB[15]
UCC4_TX_EN	PB[16]
UCC4_TX_ER / UCC2_RXD6	PB[17]
UCC4_RXD0	PB[18]
UCC4_RXD1	PB[19]
UCC4_RXD2 / UCC2_TXD7	PA[20]
UCC4_RXD3 / UCC2_RXD5	PB[21]
UCC2_TXD6	PB[22]
UCC2_TXD4	PB[23]
UCC4_RX_DV	PB[24]
UCC4_RX_ER	PB[25]
USB_SPEED	PB[26]
CPU_DEBUG4	PB[27]
CPU_SPI MOSI	PB[28]
CPU_SPI MISO	PB[29]
CPU_SPI CLK	PB[30]
CPU_/SPI SEL	PB[31]





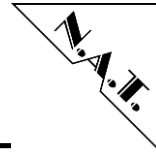
**Table 21: CPU Port Pin Definition – Port C**

Signal Function	Port C Pin
nc	PC[0]
QE_CLK2	PC[1]
UCC2_GTX_CLK	PC[2]
UCC2_GRX_CLK	PC[3]
QE_CLK5	PC[4]
nc	PC[5]
QE_CLK7	PC[6]
nc	PC[7]
UCC1_GRX_CLK	PC[8]
QE_CLK10	PC[9]
QE_CLK11	PC[10]
nc	PC[11]
nc	PC[12]
nc	PC[13]
nc	PC[14]
QE_CLK16	PC[15]
nc	PC[16]
UCC4_GRX_CLK	PC[17]
QE_CLK19	PC[18]
nc	PC[19]
UCC1_GTX_CLK	PC[20]
RESET_ATMEL	PC[21]
nc	PC[22]
nc	PC[23]
UCC4_GTX_CLK	PC[24]
nc	PC[25]
UPC_CLKO	PC[26]
nc	PC[27]
nc	PC[28]
nc	PC[29]
UCC1_MDIO	PC[30]
UCC1_MDC	PC[31]



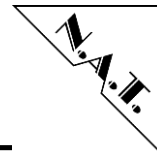
**Table 22: CPU Port Pin Definition – Port D**

Signal Function	Port D Pin
UPC_TX_SOC	PD[0]
UPC_TX_ENB	PD[1]
TX_CLAV0	PD[2]
UPC_RXD15	PD[3]
UPC_TXD14	PD[4]
UPC_TXD13	PD[5]
UPC_TXD12	PD[6]
UPC_TXD11	PD[7]
UPC_TXD10	PD[8]
UPC_TXD9	PD[9]
UPC_TXD8	PD[10]
UPC_TXD7	PD[11]
UPC_TXD15	PD[12]
UPC_RXD14	PD[13]
UPC_TXD6	PD[14]
UPC_TXD5	PD[15]
UPC_RXD2	PD[16]
UPC_RXD1	PD[17]
UPC_RXD0	PD[18]
UPC_RXD3	PD[19]
UPC_TXD2	PD[20]
UPC_TXD3	PD[21]
UPC_RXD6	PD[22]
UPC_TXD1	PD[23]
UPC_TXD0	PD[24]
UPC_TXD4	PD[25]
UPC_RXD4	PD[26]
UPC_RXD5	PD[27]
UPC_RXD13	PD[28]
UPC_RXD12	PD[29]
UPC_RXD11	PD[30]
UPC_RXD10	PD[31]



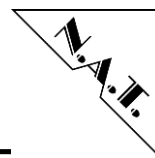
**Table 23: CPU Port Pin Definition – Port E**

Signal Function	Port E Pin
UPC_RXD9	PE[0]
UPC_RXD8	PE[1]
UPC_RXD7	PE[2]
UPC_RX_SOC	PE[3]
UPC_RX_ENB	PE[4]
UPC_RX_CLAV0	PE[5]
UPC_TX_PRTY	PE[6]
UPC_RX_PRTY	PE[7]
PLL_MS1	PE[8]
CPU_DEBUG7	PE[9]
UPC_RX_ADDR2	PE[10]
UPC_RX_ADDR4	PE[11]
nc	PE[12]
UPC_RX_ADDR0	PE[13]
UPC_RX_ADDR3	PE[14]
UPC_RX_ADDR1	PE[15]
UPC_TX_ADDR2	PE[16]
UPC_TX_ADDR3	PE[17]
nc	PE[18]
PLL_MS0	PE[19]
UPC_TX_ADDR0	PE[20]
UPC_TX_ADDR1	PE[21]
nc	PE[22]
UPC_TX_ADDR4	PE[23]
PLL_TIE_CLEARn	PE[24]
PLL_OUTSEL	PE[25]
PLL_BW_SEL	PE[26]
CPU_DEBUG0	PE[27]
CPU_DEBUG1	PE[28]
CPU_DEBUG2	PE[29]
PLL_HMS	PE[30]
SI_TDM_SYNC	PE[31]



**Table 24: CPU Port Pin Definition – Port F**

Signal Function	Port F Pin
SI1_TDMb_RxD	PF[0]
SI1_TDMb_TxD	PF[1]
SI_TDM_SYNC	PF[2]
USB_/OE	PF[3]
USB_TP	PF[4]
USB_TN	PF[5]
USB_RP	PF[6]
USB_RXD	PF[7]
USB_RN	PF[8]
UART1_SOUT	PF[9]
UART1_CTS	PF[10]
UART1_RTS	PF[11]
UART1_SIN	PF[12]
CPU_DEBUG6	PF[13]
CPU_DEBUG3	PF[14]
SI_TDM_SYNC	PF[15]
SI2_TDMa_TxD	PF[16]
SI2_TDMa_RxD	PF[17]
SI_TDM_SYNC	PF[18]
USB_SUSPND	PF[19]
USB_MODE	PF[20]
/INT2_ATMEL	PF[21]
PS1_PIGGYn	PF[22]
nc	PF[23]
nc	PF[24]
nc	PF[25]
nc	PF[26]
nc	PF[27]
nc	PF[28]
nc	PF[29]
nc	PF[30]
nc	PF[31]



## 5 NAMC-8569-CPU Programming Notes

### 5.1 Linux NOR Flash Memory Map

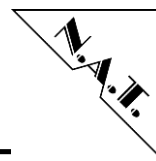
**Table 25: Linux NOR Flash Memory Map – Overview**

Start Address	End Address	Definition	Size
0xF8000000	0xF877FFFF	Data-A	7 MB
0xF8780000	0xF879FFFF	U-Boot-A Env.	128 KB
0xF87A0000	0xF87FFFFFFF	U-Boot-A (Primary boot loader)	384 KB
0xF8800000	0xF8F7FFFF	Data-B	7 MB
0xF8F80000	0xF8F9FFFF	U-Boot-B Env.	128 KB
0xF8FA0000	0xF8FFFFFFF	U-Boot-B (Backup boot loader)	384 KB
0xF9000000	0xF92FFFFFFF	Kernel Image	3 MB
0xF9300000	0xF93FFFFFFF	Device Tree Blob (DTB)	1 MB
0xF9400000	0xFF800000	Root File System	100 MB

### 5.2 FPGA Memory Map

**Table 26: FPGA Memory Map – Overview**

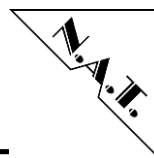
	Logical Block	Description
<b>0x00000..0x000ff</b>	General Purpose Status	General Purpose Read-Only
<b>0x00100..0x001ff</b>	General Purpose Registers	General Purpose Read/Write
<b>0x01000..0x01fff</b>	FPGA SPI Flash Interface	
<b>0x02000..0x02fff</b>	Atmel SPI Interface	
<b>0x10000..0x1ffff</b>	GigabitEthernet Interface Block	
<b>0x20000..0x2ffff</b>	Local TDM Block	
<b>0x80000..0xfffff</b>	iTDM Block	



**5.2.1 FPGA Register Description General Purpose Status Registers - 0x00..0x1ff**

**Table 27: FPGA Register Description General Purpose Status / Registers**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	Reserved								PCB_VERS							
0x02	Reserved								FPGA_VERS							
0x04	TEST_VAL_1															
0x06	TEST_VAL_2															
0x08	Board_ID															
0x0A	Reserved											ASS_OPT	Reserved			
0x0C	IRQ_STAT															
0x0E	Reserved										PLL_STAT					
0x10	Reserved															
0x100	RST															
0x102	Reserved								AMC_LED_CTRL							
0x104	Reserved															
0x106	Reserved															
0x108	Reserved															
0x10A	Reserved															
0x10C	IRQ_ENBL															
0x10E	TCKL_A_CTRL															
0x110	TCKL_B_CTRL															
0x112	TCKL_C_CTRL															
0x114	TCKL_D_CTRL															
0x116	PLL_REF0_SEL															
0x118	PLL_REF1_SEL															
0x11A	Reserved															
0x11C	Reserved															
0x11E	Reserved															
0x120	PLL_CTRL															



**5.2.1.1 FPGA Register Description – PCB\_VERS – 0x00**

Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read Only
7..4	PCB_MAJ_VERS	PCB Major Version (x.y) 4 bit unsigned number	HW init	Read Only
3..0	PCB_MIN_VER	PCB Minor Version (x.y) 4 bit unsigned number	HW init	Read Only

**Note:** The PCB Version is determined by the level of unused pins hardcoded on the PCB.

**5.2.1.2 FPGA Register Description – FPGA\_VERS – 0x02**

Bit	Name	Description	Default	Access
15..8	FPGA_SUB_VERS	FPGA Sub Version (x.y.z); 8 bit unsigned number	n/a	Read Only
7..4	FPGA_MAJ_VERS	FPGA Major Version (x.y.z) 4 bit unsigned number	n/a	Read Only
3..0	FPGA_MIN_VERS	FPGA Minor Version (x.y.z) 4 bit unsigned number	n/a	Read Only

**5.2.1.3 FPGA Register Description – TEST\_VAL\_1 – 0x04**

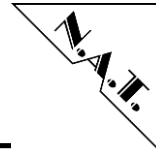
Bit	Name	Description	Default	Access
15..0	TEST_1	Random number for testing purposes	0xAA55	Read Only

**5.2.1.4 FPGA Register Description – TEST\_VAL\_2 – 0x06**

Bit	Name	Description	Default	Access
15..0	TEST_2	Random number for testing purposes	0xDEAD	Read Only

**5.2.1.5 FPGA Register Description – BOARD\_ID – 0x08**

Bit	Name	Description	Default	Access
15..0	BOARD_ID	Holds the Board ID	0x0b13	Read Only



**5.2.1.6 FPGA Register Description – ASS\_OPT – 0x0A**

Bit	Name	Description	Default	Access
15..4		Reserved	0x00	Read Only
3..2	DRAM_SIZE	Assembly option – DRAM size 00 – 128 MB 01 – 256 MB 10 – 512 MB 11 – 1024 MB	10	Read Only
1..0		Reserved	00	Read Only

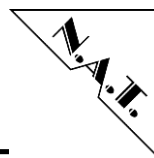
**5.2.1.7 FPGA Register Description – IRQ\_STAT – 0x0C**

Bit	Name	Description	Default	Access
15..0	IRQ_STAT	IRQ_Status	0x0000	Read Only

**5.2.1.8 FPGA Register Description – PLL\_STAT – 0x0E**

Bit	Name	Description	Default	Access
15..5		Reserved	na	Read Only
4	LOCK	PLL locked	na	Read Only
3	HLD_OV	Hold over mode	na	Read Only
1..2	REF_FAIL	PLL reference failed	na	Read Only
0	SEL_REF	Selected reference signal	na	Read Only





**5.2.1.9 FPGA Register Description – RST – 0x100**

Writing “1” to a bit of this register causes a reset pulse on the respective device. All bits are self-clearing.

Bit	Name	Description	Default	Access
15	BOARD_RST	Complete System reset	0x0	Read/Write
7..14		Reserved	0x0	Read/Write
6	IPMI_RST	IPMI reset	0x0	Read/Write
5		Reserved	0x0	Read/Write
4	SPI_RST	SPI controller to FPGA configuration EEPROM reset	0x0	Read/Write
3	LOC_TDM_RST	Local TDM logic reset	0x0	Read/Write
2	GBE_RST	Gigabit Ethernet logic reset	0x0	Read/Write
1	ITDM_RST	IDTM reset	0x0	Read/Write
0	LOC_RST	Local bus devices reset	0x0	Read/Write

**5.2.1.10 FPGA Register Description – AMC\_LED\_CTRL – 0x102**

Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read/Write
7..4	ORNG	AMC_LED control orange	0x0	Read/Write
3..0	GRN	AMC_LED control green	0x7	Read/Write

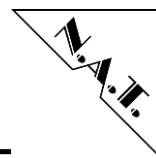
**Note:** As both LEDs share one hole in the Front Panel, they optically appear as one LED.

Register Value	Behaviour green LED	Behaviour orange LED
0x0	LED off	
0x1	LED solid on	
0x2	LED slow blink	
0x3	LED fast blink	
0x4	PLL locked	
0x5	Ethernet Activity	
0x6	Ethernet Link established	
0x7	Alternating: PLL locked / Ethernet Link established*	PCIe-Link established*
0x8	Local Bus Activity	

\* If both LED control nibbles hold the value “0x7”, they show alternating “PLL locked”, “Ethernet Link established” and “PCIe-Link established” in the corresponding colour.

**5.2.1.11 FPGA Register Description – IRQ\_ENBL – 0x10C**

Bit	Name	Description	Default	Access
15..0	IRQ_ENBL	IRQ_Enable	0x0000	Read/Write



**5.2.1.12 FPGA Register Description – TCKL\_A\_CTRL – 0x10E**

Bit	Name	Description	Default	Access
15..0	TCKL_A	Selects which signal is driven on TCKLA	0x0000	Read/Write

Register Value	Signal
0x0	Output disabled (Tristate)
0x1..0x10	Static Low Level
0x11	TCLK_A
0x12	TCLK_B
0x13	TCLK_C
0x14	TCLK_D
0x15	Frame sync signal of the local TSI
0x16	Telecom PLL output 8.192 MHz
0x17	Telecom PLL output 65.536 MHz
0x18	Telecom PLL output 1.544 MHz

**5.2.1.13 FPGA Register Description – TCKL\_B\_CTRL – 0x110**

Bit	Name	Description	Default	Access
15..0	TCKL_B	Selects which signal is driven on TCKLB	0x0000	Read/Write

For detailed information on the register values and the related signals, please refer to chapter 5.2.1.12.

**5.2.1.14 FPGA Register Description – TCKL\_C\_CTRL – 0x112**

Bit	Name	Description	Default	Access
15..0	TCKL_C	Selects which signal is driven on TCKLC	0x0000	Read/Write

For detailed information on the register values and the related signals, please refer to chapter 5.2.1.12.

**5.2.1.15 FPGA Register Description – TCKL\_D\_CTRL – 0x114**

Bit	Name	Description	Default	Access
15..0	TCKL_D	Selects which signal is driven on TCKLD	0x0000	Read/Write

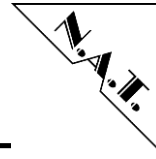
For detailed information on the register values and the related signals, please refer to chapter 5.2.1.12.

**5.2.1.16 FPGA Register Description – PLL\_REF0\_SEL – 0x116**

Bit	Name	Description	Default	Access
15..0	PLL_REF0_SEL	Selects which signal is driven to PLL_REF0	0x0011	Read/Write

For detailed information on the register values and the related signals, please refer to chapter 5.2.1.12.

**Note:** If the PLL\_REF0\_SEL-Register holds the value "0", the signal is "0" (not Tristate).



**5.2.1.17 FPGA Register Description – PLL\_REF1\_SEL – 0x118**

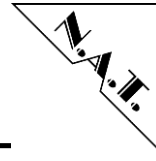
Bit	Name	Description	Default	Access
15..0	PLL_REF1_SEL	Selects which signal is driven to PLL_REF1	0x0000	Read/Write

For detailed information on the register values and the related signals, please refer to chapter 5.2.1.12.

**Note:** If the PLL\_REF1\_SEL-Register holds the value "0", the signal is "0" (not Tristate).

**5.2.1.18 FPGA Register Description – PLL\_CTRL – 0x120**

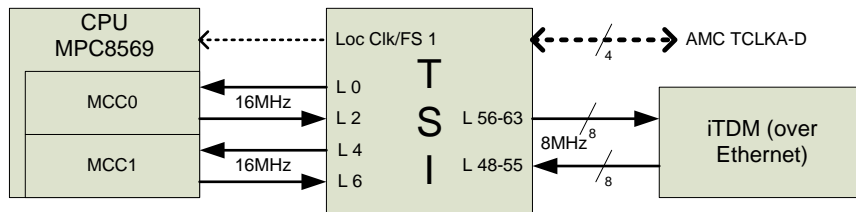
Bit	Name	Description	Default	Access
15..8		Reserved	0x00	Read/Write
7	PLL_OOR_SEL	Out of range Select For detailed information please refer to the Zarlink ZL30100 Data Sheet	0	Read/Write
6..0		Reserved	0x00	Read/Write



## 6 TDM Structure

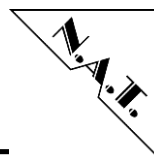
The block diagram below shows the basic TDM structure realized on the **NAMC-8569-CPU**. Central connecting element here is a time slot interchanger (TSI) implemented within the FPGA. It offers the option to setup connections between the CPU and the iTDM engine for data exchange with board external devices.

**Figure 5: TDM Structure**



**Table 28: TDM Structure**

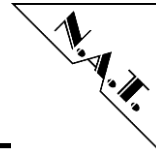
TSI data line	Connected TDM Device	TDM Channel	Direction from FPGA-TSI	Frequency	Sync and Clock for TDM Channel
L 0	MPC8569	SI1_B_Rx	Output	16 MHz	Local CLK/FS 1
L 2	MPC8569	SI1_B_Tx	Input	16 MHz	Local CLK/FS 1
L 4	MPC8569	SI2_A_Rx	Output	16 MHz	Local CLK/FS 1
L 6	MPC8569	SI2_A_Tx	Input	16 MHz	Local CLK/FS 1
L 48-55	iTDM	TimeSlot 0-1023 Rx	Input	8 MHz	internal
L 56-63	iTDM	TimeSlot 0-1023 Tx	Output	8MHz	internal



## 7 Board Specification

**Table 29: NAMC-8569-CPU Features – Overview**

<b>Processor</b>	PowerQUICC III MPC8569 (800, 1000 or 1333 MHz) based Embedded PowerPC Architecture
<b>AMC-Module</b>	Standard Advanced Mezzanine Card, single width
<b>Front-I/O</b>	2x RJ45 Ethernet, USB Type A, RS 232 (Mini-USB)
<b>Main Memory</b>	128 – 1024 MB DDR2 SDRAM
<b>Flash PROM</b>	128 MB 16-bit parallel NOR-Flash 2 GB NAND-Flash
<b>Removable Flash</b>	Micro SD-Card Slot
<b>Firmware</b>	OK1, QNX BSP and Linux BSP (on request)
<b>Power Consumption (MPC8569 / 1333 MHz)</b>	12V / 2.0A
<b>Operating Temperature</b>	0°C – +55°C with forced cooling
<b>Storage Temperature</b>	-40°C - +85°C
<b>Humidity</b>	10% – 90% rh non-condensing
<b>Standards compliance</b>	PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG AMC.2 Rev. 1.0 (Type E2) PCI Express Base Specification Rev. 1.1 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG $\mu$ TCA.0 Rev. 1.0



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## 8 Installation

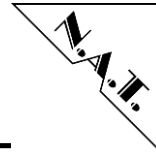
### 8.1 Safety Note

To ensure proper functioning of the **NAMC-8569-CPU** during its usual lifetime take the following precautions before handling the board:

#### CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-8569-CPU** read this installation section
- Before installing or uninstalling the **NAMC-8569-CPU**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-8569-CPU** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-8569-CPU** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing



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## 8.2 Installation Prerequisites and Requirements

### IMPORTANT

Before powering up check this section for installation prerequisites and requirements!

#### 8.2.1 Requirements

The installation requires only:

- an ATCA carrier board, or a  $\mu$ TCA backplane for connecting the **NAMC-8569-CPU**
- power supply
- cooling devices

#### 8.2.2 Power supply

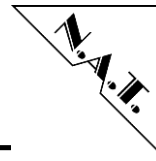
The power supply for the **NAMC-8569-CPU** must meet the following specifications:

- required for the module: +12V / 2.0A max.

#### 8.2.3 Automatic Power Up

In the following situations the **NAMC-8569-CPU** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
  - when +12V voltage level drops below 10V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe-Reset.



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## **8.3 Statement on Environmental Protection**

### **8.3.1 Compliance to RoHS Directive**

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

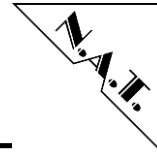
### **8.3.2 Compliance to WEEE Directive**

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronic equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.





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If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

**8.3.3 Compliance to CE Directive**

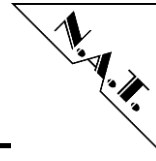
Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

**8.3.4 Product Safety**

The board complies with EN60950 and UL1950.

**8.3.5 Compliance to REACH**

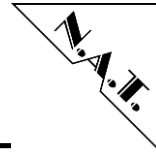
The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.



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## 9 Known Bugs / Restrictions

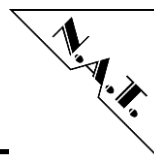
none



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## Appendix A: Reference Documentation

- [1] MPC8569 Reference Manual, Rev. 0
- [2] Atmel, AT24C128/256 Data Sheet, Rev. 0670J-SEEPR-4/1/03
- [3] Atmel, Atmega16/16L Product Data, Rev. 2466C-03/02
- [4] Lattice, ECP3 Handbook, Version 1.7
- [5] Zarlink, T1/E1 System Synchronizer Data Sheet, April 2010



## Appendix B: Document's History

Revision	Date	Description	Author
1.0	31.08.2010	initial revision	te
1.1	20.04.2011 03.08.2011	Added chapter 5 Updated to new layout, adapted contents Updated company contact data	se
1.2	10.10.2012	Fixed wrong default description in 4.3.10.2 Added note for Ekeying update in 4.3.10	te
1.3	05.06.2013	Address updated, words updated Layout update, typo correction	Fh se
	26.06.2013	Added chapter 5.1 Linux NOR Flash Memory Map	am/ww
	09.10.2013	Adress updated	se
1.4	22.01.2014	Register update 0x10	se
	26.03.2014	Added chapter 6 „TDM Structure“ Update „Location Diagram“, „Connector Diagram“ Minor changes	se
1.5	31.03.2014	Minor changes in block diagram	se
	07.05.2014 13.05.2014	Reworked Table 1: Abbreviations Update Pin Assignment J1 Update chapter 5.2 Register Description Update chapter 4.3.8/4.3.9 – DIP SW 2/3 Update chapter 8.3 RoHS-Directive / REACH Update chapter 4.2 LED Description Added chapter 4.4 CPU Port Pin Definition	se

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