NVME-PMC

VMEbus Carrier for 2 PMC Modules for Telecom Applications

Technical Reference Manual V1.10
Hardware Revision V1.5

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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1 Introduction

The NVME-PMC is a non intelligent VMEbus carrier board for PMC modules. The board is capable of carrying two PMC modules.

1.1 Technical Data

VMEbus Interface:

- A32/D32 support
- A24/D16 support
- Uses only 64Kbyte address space in A32 or A24 area
- Two independent mapping areas for PCI memory space

VME to PCI bridge:

- FPGA design based on Altera EP1K30 chip
- PCI master support
- Power supply for both PMC slots independently switchable (PCB V1.2 up)

PMC Slots

- Two 32Bit / 33 MHz PMC slots
- 3.3V PCI Bus signaling, 5V tolerant
- Power supply switchable by software
- SCBus wired to VMEbus backplane (P2)

VME SCBus Backplane Support

- SCBus signals from both PMC slots (connector P14) routed to VME P2 backplane connector according to ANSI/VITA standard 6-1994 SCSA

1.2 Board Specification

Table 1: NVME-PMC Features

Board Format	standard 6U VME board	
VME to PCI bridge	FPGA	
PMC	2 PMC slots (32 Bit / 33 MHz) 3.3 V Signals, 5V tolerant	
Power consumption Carrier	5.0V 1A typ. + PMC module supply ***note:*** the 3.3V supply of the PMC's is derived from the 5V of the carrier!	
Power Supply PMC Slots	3.3 V: max 2.5 A 5V: max 2A	
Environmental conditions	Temperature (operating): Temperature (storage): Humidity:	0°C to +60°C with forced cooling -40°C to +85°C 10 % to 90 % rh non-condensing
Standards compliance	PCI Rev. 2.2 ANSI/VITA 1-1994 VME64 (subset supported) ANSI/VITA standard 6-1994 SCSA	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NcPCI PMC** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NcPCI PMC** read this installation section
- Before installing or uninstalling the **NcPCI PMC** in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NcPCI PMC** is connected to the backplane via all cPCI connectors and that the power is available on all cPCI connectors (GND, +5V, +3,3V, +12V, +12V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is firmly screwed to the rack
  - and shielded by closed housing

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a VMEbus backplane for connecting the **NVME-PMC**
- power supply

2.2.2 Power supply

The power supply for the **NVME-PMC** must meet the following specifications:

- required for the board:
  - +5V / 0.5A typical

- required for optionally mounted PMC modules:
  - +5V / 3.0A max.
  - +12V / 0.25 A max.
  - –12V / 0.25 A max.

Refer to User's Manuals of the PMC modules for information on their power consumption. The numbers given above are the maximum values, if both PMC slots are populated, and each module draws the maximum current allowed from one supply. The overall maximum power allowed to be drawn by both modules together is 15W according to the PMC spec.

2.2.3 Automatic Power Up

In the following situations the **NVME-PMC** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset

  - when any of the voltages supervised fall out of ±5% tolerance
    supervised voltages are: +5V
  - when the system slot board signals a PCI Reset

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

2.3.4 Product Safety

The board complies to EN60950 and UL1950.

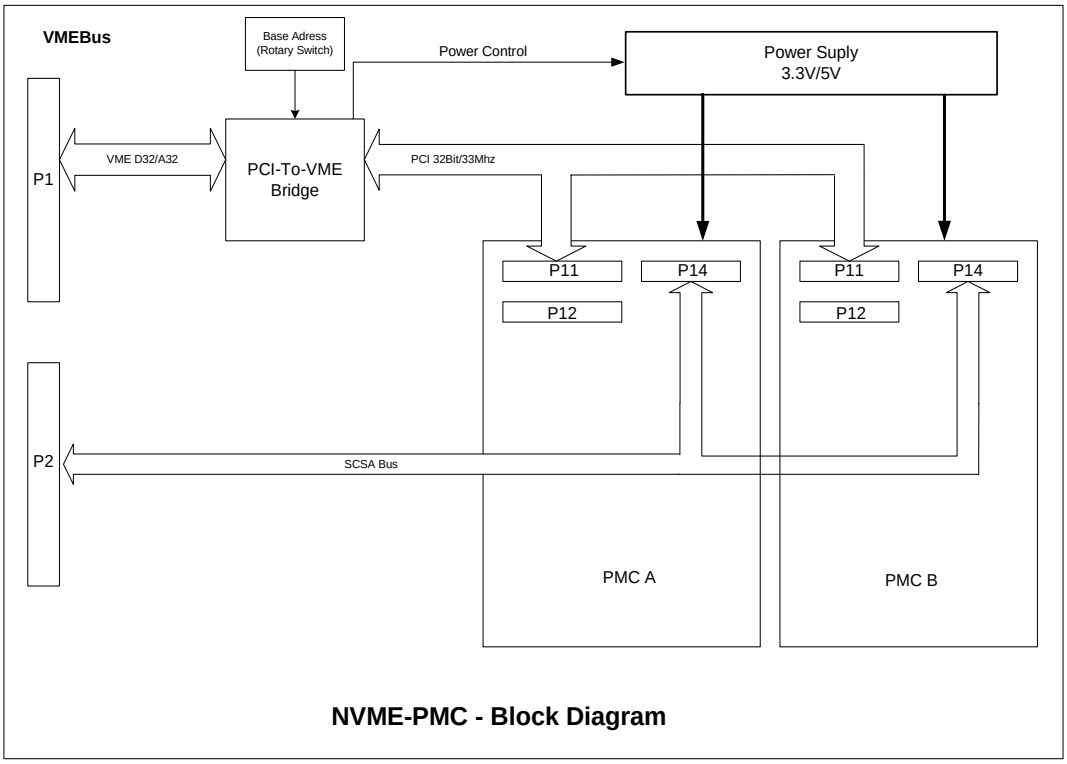
3 Hardware Description

This chapter contains a brief description of the functional blocks of the NVME-PMC board.

3.1 Hardware Overview

The NVME-PMC is a VMEbus carrier board for PMC modules. It supports two PMC slots. The internal PCI bus which interconnects the VME-to-PCI bridge and the PMC slots is a D32 / 33MHz PCI bus. The power supply for each PMC slot can be switched independently by configuration registers within the VME-to-PC bridge (PCB V1.2 and up).
Interrupts from each of the PMC modules are forwarded to the VMEbus and result in a standard VMEbus interrupt cycle supplying and interrupt vector to the host CPU. The interrupt vector and interrupt level to be used can be programmed in the VME-to-PCI bridge chip.
The VME bus base address of the board is set by two rotary switches (SW2 and SW11).
The board can be used in A24 or A32 address space, selectable by JP2.
Four software programmable LEDs are available to display status informations.

Figure 1: NVME-PMC Block Diagram



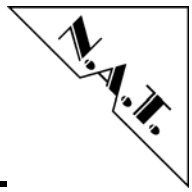
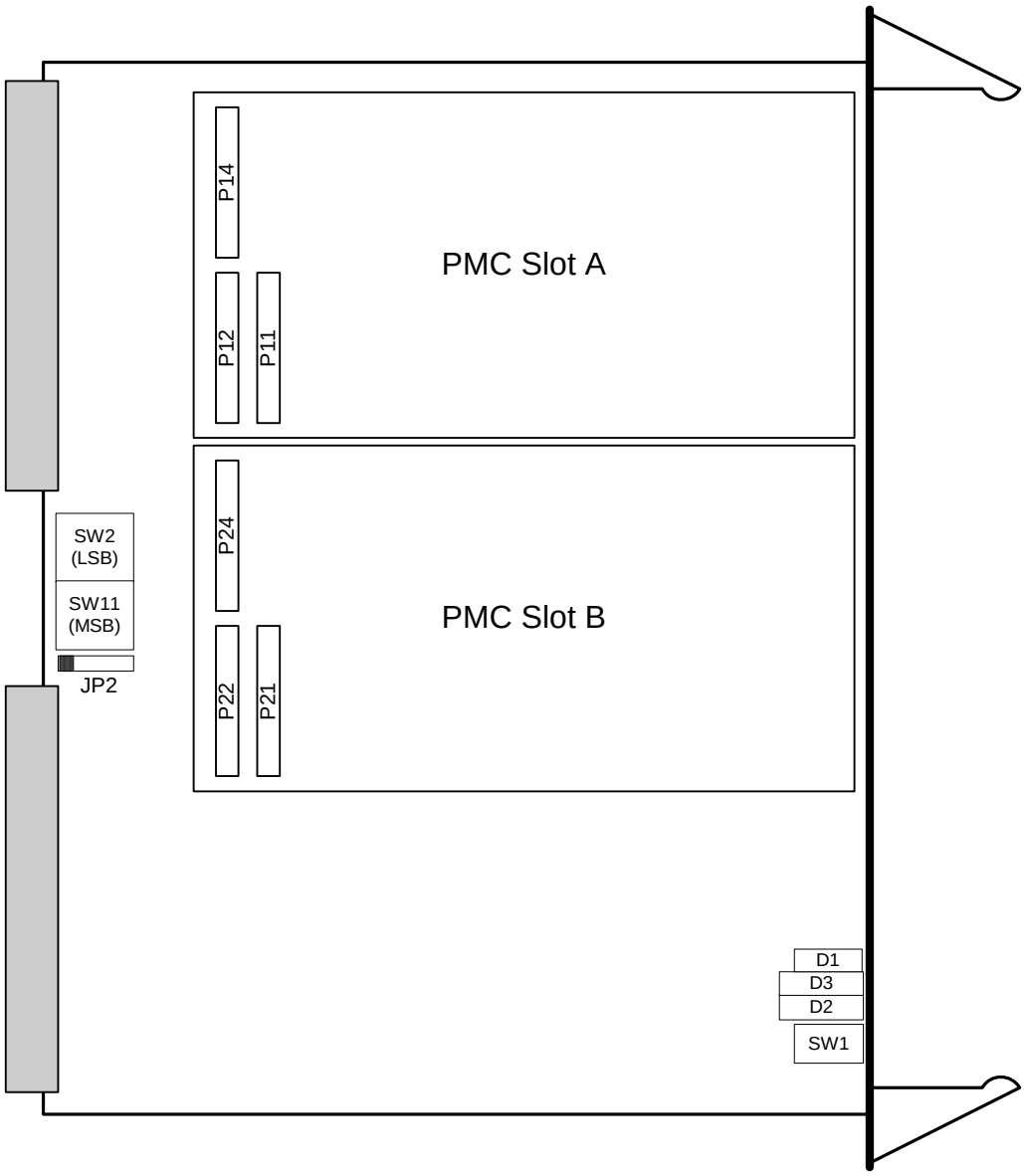


Figure 2: Location Diagram



4 Address Map and Registers

4.1 Memory Map

The NVME-PMC board occupies a 64 KByte window within the VME A32 or VME A24 address space. The base address of the board within the A32/A24 address space is selected via SW2/SW11. The address space is selected by JP2.

Table 2: JP2 -Address Space Selector

Position	Function
1-2	Extended Address Space selected (A32)
2-3	Standard Address Space selected (A24)

Only the lowest 2 KByte of the address window is used. The organization of this memory area is shown in the following table.

Table 3: Memory Map

Address	Memory Block	PCI mapping address	Width
0x0000-0x3FF	Control and Status Registers of the VME to PCI Bridge	n.a.	D16
0x0400-0x04FF	Configuration Space PMC Slot A	n.a.	D8/D16/D32
0x0500-0x05FF	Configuration Space PMC Slot B	n.a.	D8/D16/D32
0x0600-0x06FF	I/O Space PMC Slot A	0x0600 (I/O)	D8/D16/D32
0x0700-0x07FF	I/O Space PMC Slot B	0x0700 (I/O)	D8/D16/D32

4.1.1 Access to the PCI Configuration Space

The PCI configuration spaces of the two PMC slots are mapped to fixed locations within the VME address window of the NVME-PMC (locations 0x400 and 0x500, see table above).
Any access to these locations leads to a configuration cycle on the PCI bus being generated by the controller.

4.1.2 Access to the PCI I/O Space

An I/O space area for each module is mapped by default. For each module a standard I/O space size of 256 bytes is preallocated. The corresponding BAR (base address register) of the PMC module must be programmed accordingly. As the VME-to-PCI routes through the lowest 16 address lines unmodified, the modules BAR must be programmed to be 0x600 (module A) or 0x700 (module B).

4.1.3 Access to the PCI Memory Space

Additional to the standard window which is defined by the VME-toPCI controller itself, which is always accessible, two optional windows within the VMEbus A32 address space can be mapped by software. These two windows can be assigned to the PCI memory space as required by the two PMC slots. The size of the memory window is defined by the mask register. The minimum size is 64Kbyte.
The memory areas can be individually enabled, their addresses and sizes are defined by the corresponding address and mask registers within the VME to PCI bridge chip.

4.2 Internal Registers of VME to PCI Bridge

The VMEbus to PCI bridge implements the following set of registers:
All registers are 16 bit wide.

4.2.1 Device ID Register

The device ID register represents a unique ID assigned to the VME to PCI bridge chip by N.A.T..

Table 4: Device ID Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Device ID															
Reset	0x2014															
R/W	R															
Addr	0x0000															

4.2.2 Revision ID Register

The revision ID register carries a numeric value identifying the current hardware release of the VME to PCI chip.

Table 5: Revision ID

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RevisionID															
Reset	RevisionID															
R/W	R															
Addr	0x0002															

4.2.3 Control Register

The control register contains control bits for the various onboard hardware functions.

Table 6: Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field					Mb	Ma	Pb	Pa	unused				LED3..0			
Reset	0	0	0	0	0	0	0	0	0x00							
R/W	R/W															
Addr	0x0004															

Bit	Name	Description
11	Mb	Memory Space PMC Slot B 1 Memory Space is enabled 0 Memory Space is disabled Precautions must be taken to set the corresponding Base and Mask registers with appropriate values before enabling the memory space. Otherwise the system may hang.
10	Ma	Memory Space PMC Slot A 1 Memory Space is enabled 0 Memory Space is disabled Precautions must be taken to set the corresponding Base and Mask registers with appropriate values before enabling the memory space. Otherwise the system may hang.
9	Pb	Power Control PMC Slot B 1 - power is ON 0 – power is OFF
8	Pa	Power Control PMC Slot A 1 - power is ON 0 – power is OFF
3-0	LED	LED Control 1 - LED is ON 0 – LED is OFF

4.2.4 VMEbus Interrupt Vector Register

To allow interrupts from one of the PMC modules to be issued to the host CPU, the host CPU must write the VMEbus interrupt vector and level into this register.

Table 7: VMEbus Interrupt Vector Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field						Level			Vector							
Reset						0x00			0x00							
R/W	R/W															
Addr	0x0006															

4.2.5 Status Register

The status register shows the status information of the onboard hardware devices and PMC modules.

Table 8: Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field															Ib	Ia
Reset															0	0
R/W															R	R
Addr	0x0008															

Bit	Name	Description
1	Ib	Interrupt pending form PMC Slot B
0	Ia	Interrupt pending form PMC Slot A

4.2.6 Memory Access Control Registers

The following set of registers allows the VMEbus master CPU to gain access to memory spaces on the PMC modules. Before enabling the access to the PCI memory space the BASE, MASK and TRANSLATION registers must be set. To finally enable the access the corresponding bit in the Control register (register address 4) must be set(Ma, Mb).
The base registers of the PMC modules must be programmed accordingly.
All register values represent the upper half of a 32 bit address only.

The effective address transferred on the PCI bus during a memory cycle is calculated by the following formula:

Address_on_PCI[31..16] = (vme_address[31..16] & ~mask) + (trans_addr & mask)
Address_on_PCI[15..1] = vme_address[15..1]
Address_on_PCI[0] = 0;

Table 9: Memory Base Register Slot A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Base[31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x000A															

Table 10: Memory Mask Register Slot A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Mask [31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x000C															

Table 11: Address Translation Register Slot A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Translation [31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x000E															

Table 12: Memory Base Register Slot B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Base[31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x0010															

Table 13: Memory Mask Register Slot B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Mask[31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x0012															

Table 14: Address Translation Register Slot B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Address Translation [31..16]															
Reset	0x0000															
R/W	R/W															
Addr	0x0014															

5 LEDs

The board contains 10 LEDs on the frontpanel (see location diagram). The dual LED D1 shows the status of the power supply of the two PMC modules.
The four software programmable LED can be programmed by the control register (Offset 0x0004). The bit assignment is according to the following table:

Name	Color	Function	Label
D2a	Green	Reset	R
D2b	Green	VME-Int	I
D2c	Orange	Reg Access	R
D2d	Red	PCI Access	P
D3a	Green	CntrReg-D0	1
D3b	Green	Cntr Reg-D1	2
D3c	Green	Cntr Reg-D2	3
D3d	Green	Cntr Reg-D3	4

6 Connectors

6.1 The PMC Connectors

The following pages specify the pin assignment of the PMC connectors of the. While P11 and P12 are specified in the PMC, resp. PCI specification, P14 is manufacturer specific and reserved for proprietary I/O signals.
The **NVME-PMC** P14 supports the SC-Bus signaling

Figure 3: **Location of PMC connectors on a PMC Module**

Please refer to the following tables to look up the pin assignment of the P11, P12 and P14.

6.1.1 Pin Assignment of the PMC Connector -- P11

Table 15: Pin Assignment of the PMC Connector -- P11

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	TCK	-12V	2	n.c.
GND	3	GND	/INT A	4	/IRQ-QSPAN
n.c.	5	/INT B	/INT C	6	n.c.
n.c.	7	bus mode 1	+5V	8	+5V
n.c.	9	/INT D	PCI_RSV1	10	n.c.
GND	11	GND	PCI_RSV2	12	n.c.
CLK	13	CLK	GND	14	n.c.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
n.c.	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
n.c.	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	n.c.
n.c.	41	/SDONE	/SB0	42	n.c.
PAR	43	PAR	GND	44	GND
n.c.	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
n.c.	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	n.c.

6.1.2 Pin Assignment of the PMC Connector -- P12

Table 16: Pin Assignment of the PMC Connector -- P12

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	+12V	/TRST	2	n.c.
n.c.	3	TMS	TDO	4	n.c.
n.c.	5	TDI	GND	6	GND
GND	7	GND	PCI_RSV3	8	n.c.
n.c.	9	PCI_RSV	PCI_RSV4	10	n.c.
n.c.	11	BUS-MODE 2	+3.3V	12	+3.3V
/RST	13	/RTS	BUS-MODE 3	14	n.c.
+3.3V	15	+3.3V	BUS-MODE 4	16	n.c.
n.c.	17	PCI_RSV	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESVD	34	n.c.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	n.c.
+3.3V	53	+3.3V	PCI_RESV	54	n.c.
n.c.	55	PCI_RESV	GND	56	GND
n.c.	57	PCI_RESV	PCI_RESV	58	n.c.
GND	59	GND	PCI_RESV	60	n.c.
n.c.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	n.c.

6.1.3 Pin Assignment of the PMC Connector -- P14 (PMC I/O)

Table 17: Pin Assignment of the PMC Connector -- P14

Ext. signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
MC	1	I/O	I/O	2	SD_15
SD_14	3	I/O	I/O	4	SD_13
SD_12	5	I/O	I/O	6	GND
SD_11	7	I/O	I/O	8	SD_10
SD_09	9	I/O	I/O	10	SD_8
SD_07	11	I/O	I/O	12	GND
SD_06	13	I/O	I/O	14	SD_5
SD_04	15	I/O	I/O	16	SD_3
SD_02	17	I/O	I/O	18	SD_1
GND	19	I/O	I/O	20	SD_0
CLKFAIL	21	I/O	I/O	22	FSYNCN
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	SCLKx2N
SL_4L	27	I/O	I/O	28	n.c.
SL_2L	29	I/O	I/O	30	SL_3L
SL_0L	31	I/O	I/O	32	SL_1L
NC	33	I/O	I/O	34	NC
NC	35	I/O	I/O	36	NC
NC	37	I/O	I/O	38	NC
NC	39	I/O	I/O	40	NC
NC	41	I/O	I/O	42	NC
NC	43	I/O	I/O	44	NC
NC	45	I/O	I/O	46	NC
NC	47	I/O	I/O	48	NC
GND	49	I/O	I/O	50	GND
NC	51	I/O	I/O	52	NC
NC	53	I/O	I/O	54	NC
NC	55	I/O	I/O	56	NC
GND	57	I/O	I/O	58	GND
NC	59	I/O	I/O	60	NC
NC	61	I/O	I/O	62	NC
NC	63	I/O	I/O	64	NC

6.1.4 Description P14 Signals

Table 18: Description P14 Signals

Signal	Description VITA Spec.	Description SC4000 Manual	DescriptionGeneral
MC	identical	identical	SC-Bus message channel
SD_15	identical	identical	SC-Bus serial data stream 15
SD_14	identical	identical	SC-Bus serial data stream 14
SD_13	identical	identical	SC-Bus serial data stream 13
SD_12	identical	identical	SC-Bus serial data stream 12
SD_11	identical	identical	SC-Bus serial data stream 11
SD_10	identical	identical	SC-Bus serial data stream 10
SD_9	identical	identical	SC-Bus serial data stream 9
SD_8	identical	identical	SC-Bus serial data stream 8
SD_7	identical	identical	SC-Bus serial data stream 7
SD_6	identical	identical	SC-Bus serial data stream 6
SD_5	identical	identical	SC-Bus serial data stream 5
SD_4	identical	identical	SC-Bus serial data stream 4
SD_3	identical	identical	SC-Bus serial data stream 3
SD_2	identical	identical	SC-Bus serial data stream 2
SD_1	identical	identical	SC-Bus serial data stream 1
SD_0	identical	identical	SC-Bus serial data stream 0
GND	identical	identical	Ground
CLKFAIL	identical	identical	SC-Bus System Clock Fail signal
SREF_8K	SREF8k	identical	SC-Bus 8 kHz Reference
n.c.	identical	identical	Not Connected
SL_0L	SL_0		SC-Bus ID SC4000
SL_1L	SL_1		SC-Bus ID SC4000
SL_2L	SL_2		SC-Bus ID SC4000
SL_3L	SL_3		SC-Bus ID SC4000
SL_4L	SL_4		SC-Bus ID SC4000

For more details please refer to the *SC4000 User´s Manual* and the VITA *Extensions to ANSI/VITA 6 - 1994 SCSA.*

6.1.5 Description VMEbus P2 Signals

Table 19: Pin Assignment of the VMEbus Connector -- P2

Pin No.	Row A	Row B	Row C
1	SC_D15		MC
2	SC_D13		SC_D14
3	GND		SC_D12
4	SC_D10		SC_D11
5	SC_D08		SC_D09
6	GND		SC_D07
7	SC_D05		SC_D06
8	SC_D03		SC_D04
9	SC_D01		SC_D02
10	SC_D00		GND
11	FSYNC		CLKFAIL
12	SCLK		SREF_8K
13	SCLKx2	VMEbus	GND
14	nc	P2B	SL_4
15	SL_3		SL_2
16	SL_1		SL_0
17	nc		nc
18	nc		nc
19	nc		nc
20	nc		nc
21	nc		nc
22	nc		nc
23	nc		nc
24	nc		nc
25	nc		nc
26	nc		nc
27	nc		nc
28	nc		nc
29	nc		nc
30	nc		nc
31	nc		nc
32	nc		nc

7 Product Errata – Known Bugs

PCB Version: V1.1

Release 020628:

Known Bugs:

1.) VME RETRY signal is driven low allways
2.) VME SYSRESET is not routed to internal logic
3.) BGIN/BGOUT Daisy chain signals are not connected
Workaround: BGIN/BGOUT signals must be jumpered on the backplane

Release 030507:

Bugs (1) and (2) from release 020628 have been fixed

8 Document's History

Version	Date	Description	Author
1.0	5.9.2001	Initial Version	hl
1.1	2.7.2002	Added location diagram	hl
1.2	21.1.2003	Reworked	hl
1.3	20.3.2003	description of VMEbus P2 pinning added	ga
1.4	22.4.2003	Added clearification on address mapping, corrected address of Interrupt Control /status register, added LEDs description	hl
1.5	07.05.2003	Changes according to Board Release 030507: - LED assignement has changed - added Known Bugs chapter	hl
1.6	27.05.2003	Added PCI signal voltage levels	hl
1.7	01.09.2003	Added Power Supply features for PMC Slots	hl
1.8	10.02.2006	chapter 'Installation' added	ga
1.9	06.06.2007	chapter 2.3.3. and 2.3.4. added	ga
1.10	06.04.2010	Fixed LED description to match latest design	te