NcPCI PMC
cPCI Carrier for 2 PMC Modules for Telecom Applications
Technical Reference Manual V2.2
Hardware Revision V2.0

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

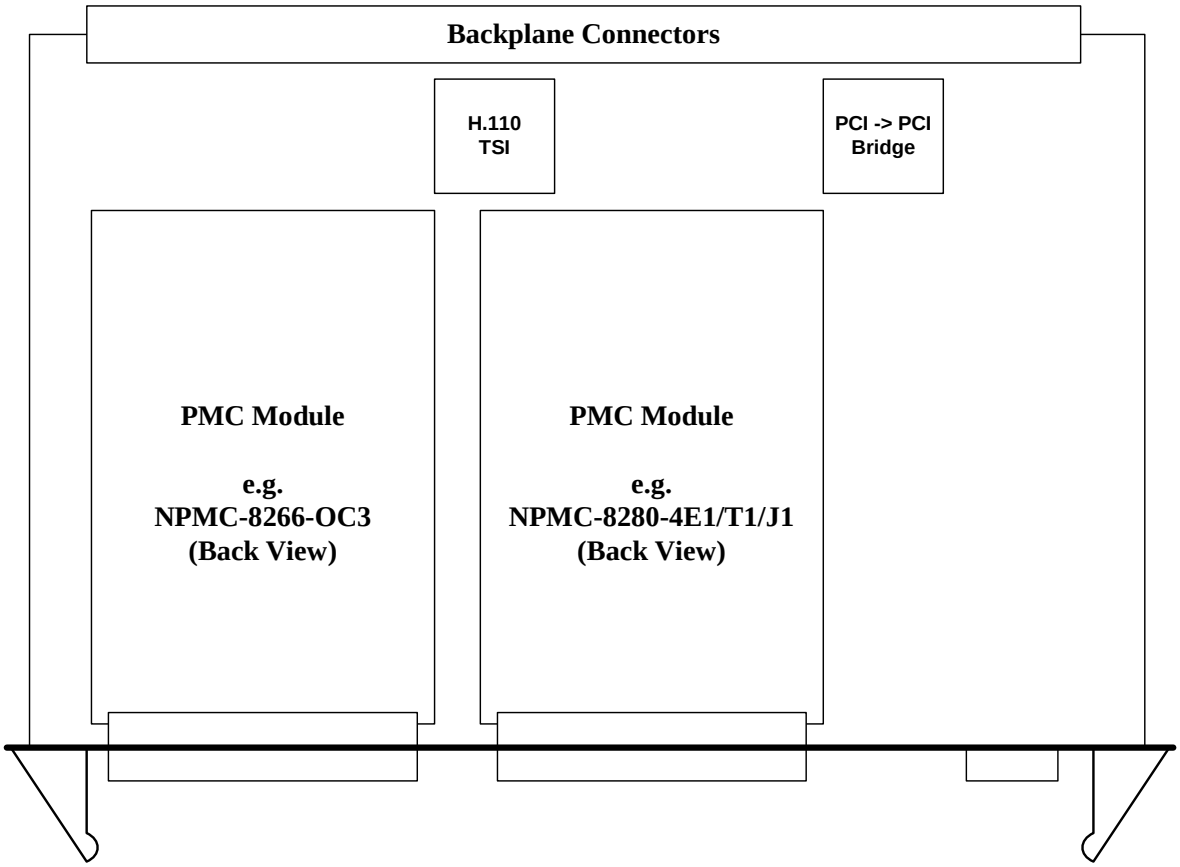
Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
H.110	Time-Slot Interchange Bus
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCSA	Signal Computing System Architecture
T1	1,544 Mbit G.703 Interface (USA)
T8110	Agere H.110 Controller
TDM	Time Division Multiplex
TSA	Time Slot Assigner
TSI	Time Slot Interchange

1 Introduction

The **NcPCI PMC** is a high performance PCI Mezzanine Card carrier board especially suited for Telecom and networking applications.

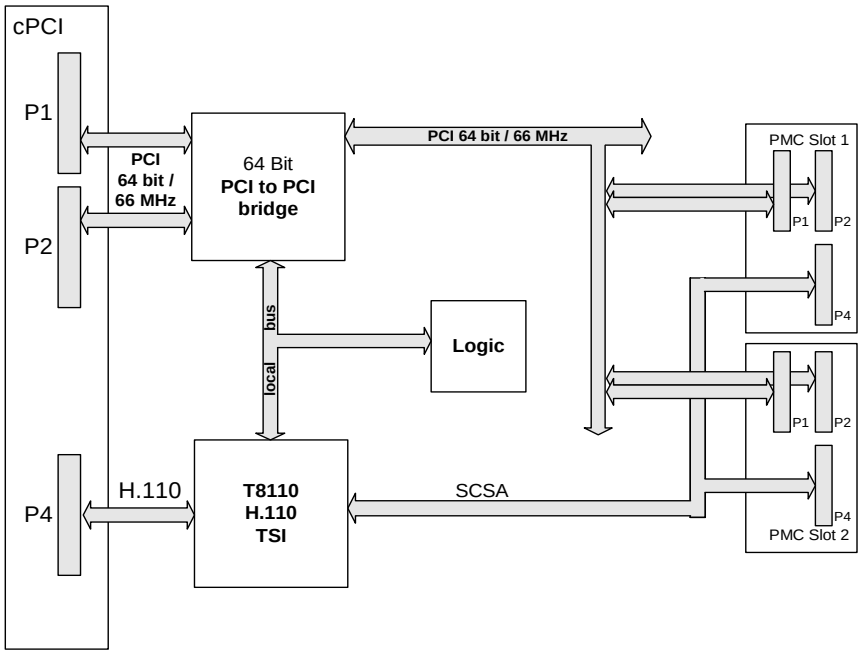
Figure 1: NcPCI PMC cPCI Intelligent Carrier Board for PMC Modules



The **NcPCI PMC** has the following major features:

- Intel 21555 PCI – PCI bridge (cPCI bus → internal PCI bus 1), 64 bit / 66 MHz
- cPCI hot-swap - capable
- cPCI 64 bit / 66 MHz, PCI Rev. 2.2
- 2 PMC slots, 64 bit / 66 MHz, PCI Rev. 2.2, P1386.1 / Draft 2.4a
- Agere T8110 TSI controller with H.110 / SCSA bus interface

Figure 2: NcPCI PMC Block Diagram



1.1 Board Features

- **Interfaces**

  cPCI: The **NcPCI PMC** includes a 32/64 bit 33/66 MHz Compact PCI bus interface. This is implemented by an Intel i21555 PCI → PCI bridge. The cPCI interface supports hot swap.

  int. PCI: The **NcPCI PMC** implements a 64 bit / 66 MHz PCI bus, which connects the i21555 PCI → PCI bridge to the 2 PMC slots, implemented according to IEEE P1386.1 / Draft 2.4a.

  int. TDM: The **NcPCI PMC** implements 2 internal TDM interfaces, one each for every PMC I/O connector. These interfaces have 32-bit TDM data path and comply to H.110 as well as SCSA timing constraints.

- **I/O**

  H.110: The **NcPCI PMC** implements a 32 bit H.110 interface according to PICMG 2.5 R1.0. This is implemented by an Agere T8110 TSI device. This device also sets the interface characteristics for the 2 internal TDM interfaces.

1.2 Board Specification

Table 2: NcPCI PMC Features

Board Format	standard 6U Compact PCI board
PCI to cPCI bridge	i21555
cPCI functions	64 Bit / 66 MHz PCI, hot swap, with H.110 extension
PMC	2 PMC slots (64 Bit / 66 MHz)
Firmware	OK1, VxWorks BSP (on request)
Power consumption	3.3V 0.5A typ. 5.0V 0.1A typ. + PMC module supply ***note:*** the 3.3V supply of the PMC's is derived from the 5V of the carrier!
Environmental conditions	Temperature (operating): 0°C to +60°C with forced cooling Temperature (storage): -40°C to +85°C Humidity: 10 % to 90 % rh noncondensing
Standards compliance	PCI Rev. 2.2 PICMG 2.5 R1.0 IEEE P1386.1 / Draft 2.4a

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NcPCI PMC** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NcPCI PMC** read this installation section
- Before installing or uninstalling the **NcPCI PMC** in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NcPCI PMC** is connected to the backplane via all cPCI connectors and that the power is available on all cPCI connectors (GND, +5V, +3,3V, +12V, +12V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is firmly screwed to the rack
  - and shielded by closed housing

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NcPCI PMC**
- power supply

2.2.2 Power supply

The power supply for the **NcPCI PMC** must meet the following specifications:

- required for the board:
  - +3.3V / 0.5A typical
  - +5V / 0.1A typical

- required for optionally mounted PMC modules:
  - +5V / 6.0A max.
  - +12V / 1.0A max.
  - –12V / 1.0A max.

Refer to User's Manuals of the PMC modules for information on their power consumption. The numbers given above are the maximum values, if both PMC slots are populated, and each module draws the maximum current allowed from one supply. The overall maximum power allowed to be drawn by both modules together is 15W according to the PMC spec. The power supply of the **NcPCI PMC** supports PPMC modules with up to 30W in total for both slots. In order to prevent excessive loading of the +3.3V supply of the **NcPCI PMC**, the +3.3V supply for the PMC modules is derived from the +5V supply of the **NcPCI PMC** by onboard switching regulators.

2.2.3 Automatic Power Up

In the following situations the **NcPCI PMC** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset

  - when any of the voltages supervised fall out of ±5% tolerance
    supervised voltages are: +5V, +3.3V
  - when the system slot board signals a PCI Reset

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that whereever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly intergrated into larger and more complex envionments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

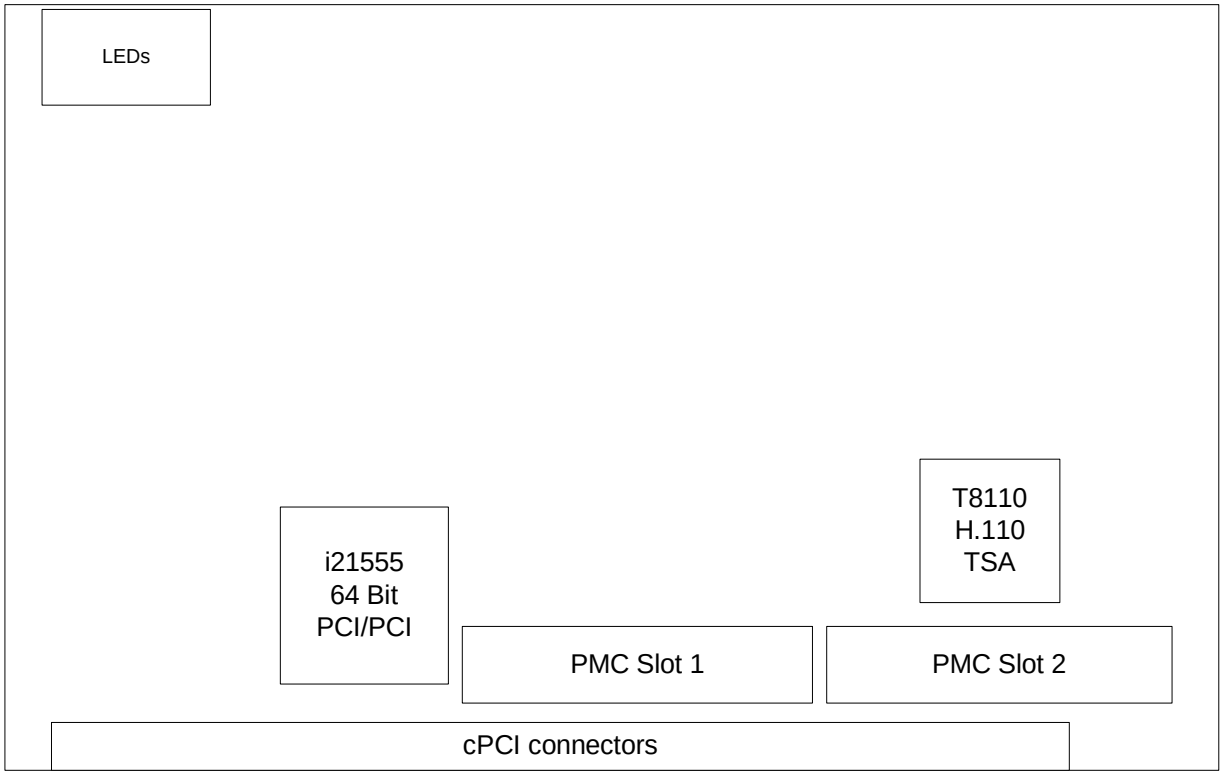
2.3.4 Product Safety

The board complies to EN60950 and UL1950.

3 Location Overview

The Figure 3: "Location diagram of the **NcPCI PMC**" shows the position of the important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

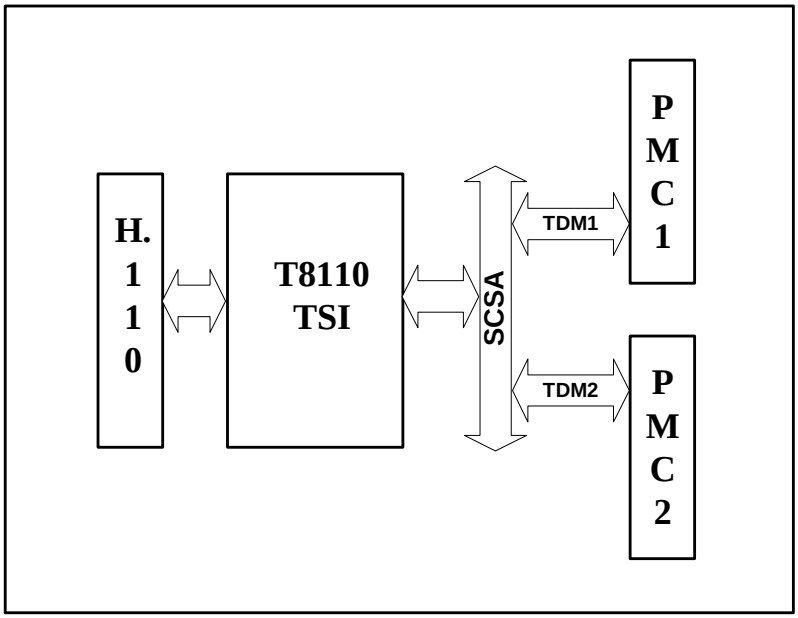
Figure 3: Location Diagram of the NcPCI PMC



4 TDM Bus and H.110 Bus Controller

Signal routing and data flow between the T8110 TSI device and the PMC slot I/O connectors is shown in Figure 4: below.

Figure 4: Local TDM Bus Organisation and Synchronisation



The TDM data are routed through the T8110 TSI device. Hence, any timeslot switching between H.110 bus and the local TDM buses is possible. The TSI device derives its time base from one of the SREF_8K or NETREF1 signals coming from the PMC modules, or from the H.110 bus. From this input it generates FSYNC and SCLK for the local SCbuses to synchronize to. For detailed information please refer to the Agere T8110 User's Manual.

5 Hardware

5.1 Memory Map (PCI)

All addresses on the internal PCI bus are set up by programming the corresponding address registers of the PCI devices and may be chosen by the user.

The following correspondence applies for PCI ADxx lines and IDSEL routing:

Table 3: IDSEL Routing for internal PCI Bus

Device	IDSEL	Address	Function
i21555	none	programmable	PCI arbiter
PMC slot 1	AD31	programmable	PMC expansion slot
PMC slot 2	AD30	programmable	PMC expansion slot

5.2 Memory Map (local)

Addresses on the internal local bus (minibridge of the i21555) are to be seen as offset to the minibridge base address programmed for the i21555 PCI bridge device.

The following correspondence applies:

Table 4: local Memory Map

Device	Address	Function
T8110	0x00.0000	H.110 TSI device
Status/Control registers	0x10.0000	Status/Control registers (see below)

5.3 Interrupt Structure

The different PCI / PMC interrupts are generated by a logical Wired-Or of the interrupt sources of the respective PCI buses. The interrupt sources are readable by status registers. Every interrupt source on the **NcPCI PMC** is maskable by software. The status of these mask registers is also readable. Refer to chapter 5.8 for a detailed description.

5.4 Hot Swap Capability

The **NcPCI PMC** is assembled with the hot swap feature enabled, and PCI signals are precharged to 1V during board insertion.

The hot swap capability of the **NcPCI PMC** according to PICMG 2.1 R2.0 complies to “Full Hot Swap”. For “High Availability” applications contact N.A.T. for support.

5.5 Clocking

The NcPCI-PMC is capable of supporting 33 MHz and 66 MHz PCI busses also in a mixed environment. Which bus frequency is actually selected for either side of the bridge depends on the status of the respective M66EN signal lines. If all PCI devices on the bus support 66 MHz, M66EN will be high. Any device not supporting 66 MHz drives M66EN low, thus forcing the bus to operate at 33 MHz bus speed.

5.6 Reset Strategy

5.6.1 Reset Sources

There are 3 Reset sources that influence the **NcPCI PMC**:

- Power-On Reset
- failure of one or more of the power supplies
- PCIRST signal of the cPCI bus

5.6.2 Reset of the PCI Bus

The i21555 PCI Bridge, which interfaces between the internal PCI bus of the **NcPCI PMC** and the Compact PCI bus, has 3 Reset pins, which carry special functionalities. P_RST and S_RST_IN are inputs, S_RST is an output. P_RST and S_RST_IN put the device into a well-defined Reset Mode and are functionally identical (wire-ored within the chip). S_RST_IN is not used on the **NcPCI PMC**; P_RST (connected to PCIRST of internal PCI bus) is generated by a CPLD, if one of the reset sources described in the above chapter becomes active, and if an external cPCI PCIRST is received.

5.7 Minibridges

5.7.1 Minibridge of the i21555 PCI Bridge

The Minibridge of the i21555 PCI bridge is used as such. Thus, it has to be programmed for support of the 8-bit peripheral devices connected to it. The connected circuitry serves also for serial load support of EEPROM configuration data and Reset configuration defined by logic pin levels during Reset.

5.7.2 Minibridge of the T8110 H.110 TSI Controller

The Minibridge of the T8110 TSI controller is not used as such. It is used as microprocessor interface instead and connects to the i21555 minibridge.

In order to write data to the microprocessor interface of the T8110 through the i21555 minibridge, it is necessary to obey to a special software handshake specified for writing to the parallel ROM interface of the i21555. Please refer to the i21555 User's Manual for further details, or ask N.A.T. for sample code.

5.8 Control / Status Registers

The address range of the Control / Status registers decoded by hardware is 16 bytes. Larger address ranges mirror every 16 bytes.

5.8.1 Interrupt Status Register 1

Interrupt Status Register 1 is accessed with address offset 0x0 to the base address programmed in the i21555 Mini Bridge Base Address Register plus the address value given in Table 4: .

Table 5: Interrupt Status Register 1

Bit Number	Read/Write	Reset Value	Status Information
Bit 7	R	0	PMC slot 2 INTD signal
Bit 6	R	0	PMC slot 2 INTC signal
Bit 5	R	0	PMC slot 2 INTB signal
Bit 4	R	0	PMC slot 2 INTA signal
Bit 3	R	0	PMC slot 1 INTD signal
Bit 2	R	0	PMC slot 1 INTC signal
Bit 1	R	0	PMC slot 1 INTB signal
Bit 0	R	0	PMC slot 1 INTA signal

5.8.2 Interrupt Status Register 2

Interrupt Status Register 2 is accessed with address offset 0x1 to the base address programmed in the i21555 Mini Bridge Base Address Register plus the address value given in Table 4: .

Table 6: Interrupt Status Register 2

Bit Number	Read/Write	Reset Value	Status Information
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	not used
Bit 3	R	0	not used
Bit 2	R	0	Compact PCI bus INTA signal
Bit 1	R	0	CLKERRTSI (T8110)
Bit 0	R	0	SYSERRTSI (T8110)

5.8.3 Interrupt Mask Control / Status Register 1

Every interrupt source on the **NcPCI PMC** is maskable by software. The status of these mask registers is readable anytime. The registers initialize to 0x0 after a reset of the PCI bus. Set a bit to enable an interrupt, clear a bit to mask (disable) an interrupt.

Interrupt Mask Control / Status Register 1 is accessed with address offset 0x2 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 7: Interrupt Mask Control / Status Register 1

Bit Number	Read/Write	Reset Value	Status Information / Control Setting
Bit 7	R/W	0	PMC slot 2 INTD signal mask bit
Bit 6	R/W	0	PMC slot 2 INTC signal mask bit
Bit 5	R/W	0	PMC slot 2 INTB signal mask bit
Bit 4	R/W	0	PMC slot 2 INTA signal mask bit
Bit 3	R/W	0	PMC slot 1 INTD signal mask bit
Bit 2	R/W	0	PMC slot 1 INTC signal mask bit
Bit 1	R/W	0	PMC slot 1 INTB signal mask bit
Bit 0	R/W	0	PMC slot 1 INTA signal mask bit

5.8.4 Interrupt Mask Control / Status Register 2

Interrupt Mask Control / Status Register 2 is accessed with address offset 0x3 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 8: Interrupt Control / Status Register 2

Bit Number	Read/Write	Reset Value	Status Information / Control Setting
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	not used
Bit 3	R	0	not used
Bit 2	R	0	not used
Bit 1	R/W	0	T8110 CLKERR signal mask bit
Bit 0	R/W	0	T8110 SYSERR signal mask bit

5.8.5 Status Register 1

Status Register 1 is accessed with address offset 0x4 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 9: Status Register 1

Bit Number	Read/Write	Reset Value	Status Information
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	cPCI geographical address bit GA4
Bit 3	R	0	cPCI geographical address bit GA3
Bit 2	R	0	cPCI geographical address bit GA2
Bit 1	R	0	cPCI geographical address bit GA1
Bit 0	R	0	cPCI geographical address bit GA0

5.8.6 Status Register 2

Status Register 2 is accessed with address offset 0x5 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 10: Status Register 2

Bit Number	Read/Write	Reset Value	Status Information
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	cPCI auxiliaury geographical address bit SGA4
Bit 3	R	0	cPCI auxiliaury geographical address bit SGA3
Bit 2	R	0	cPCI auxiliaury geographical address bit SGA2
Bit 1	R	0	cPCI auxiliaury geographical address bit SGA1
Bit 0	R	0	cPCI auxiliaury geographical address bit SGA0

5.8.7 Status Register 3

Status Register 3 is accessed with address offset 0x6 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 11: Status Register 3

Bit Number	Read/Write	Reset Value	Status Information
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	auxiliaury geographical address bit GA4 on cPCI Connector J4
Bit 3	R	0	auxiliaury geographical address bit GA3 on cPCI Connector J4
Bit 2	R	0	auxiliaury geographical address bit GA2 on cPCI Connector J4
Bit 1	R	0	auxiliaury geographical address bit GA1 on cPCI Connector J4
Bit 0	R	0	auxiliaury geographical address bit GA0 on cPCI Connector J4

5.8.8 Control / Status Register 4

Control / Status Register 4 is accessed with address offset 0x7 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: . The register initializes to 0x73 after a power-on reset, if no PMC module is installed. Otherwise, the status of bits 3-2 depend on the module installed.

Table 12: Control / Status Register 4

Bit Number	Read/Write	Reset Value	Status Information / Control Setting
Bit 7	R/W	0	OE_D16/31 TDM Bus routing switch
Bit 6	R/W	1	BUSMODE 4 signal
Bit 5	R/W	1	BUSMODE 3 signal
Bit 4	R/W	1	BUSMODE 2 signal
Bit 3	R	0	BUSMODE 1 signal of PMC slot 2
Bit 2	R	0	BUSMODE 1 signal of PMC slot 1
Bit 1	R/W	1	CTC8B_EN H.110 clock/frame Term. Enable
Bit 0	R/W	1	CTC8A_EN H.110 clock/frame Term. Enable

5.8.8.1 H.110 Clock/Frame Enable Configuration Pins

CTC8B_EN, CTC8A_EN

Two bits of Control / Status Register 4 are used to select the 33Ω serial line termination of the C8 clock and frame.
If the H.110 controller is clock/sync slave the serial lines have to be terminated according to the H.110 specification. If the H.110 controller is clock/sync master the serial lines must not be terminated.
The termination of the clock / frame signal groups A and B that connect T8110 and H.110 bus can be set separately for group A and group B.
Setting the respective bit to '1' selects the 33 Ω serial line termination (T8110 is clock/sync slave, default setting). Setting the respective bit to '0' shorts the 33 Ω serial line termination (T8110 is clock/sync master).

5.8.8.2 PMC Module BUSMODEx Configuration Pins

BUSMODE0-4

Five bits of Control / Status Register 4 are used to manage the PMC BUSMODEx signals. By this register the BUSMODE2-4 pins on the PMC modules can be set, and the status of all BUSMODE signals of both slots is readable. BUSMODE2 - 4 are bused.

5.8.8.3 TDM Bus Routing Switch Configuration Pin

OE_D16/31

This bit sets the way the local TDM buses of the PMC modules are routed to the T8110 TSI controller's local bus interface. The TDM switching element, which is controlled by OE_D16/31, was introduced due to compatibility reasons to older versions of the **NcPCI PMC**. By default, this bit is cleared, and the TDM routing is compatible to **NcPCI PMC** version 1.4 and older.

Routing between the local TDM buses of the PMC's and the T8110 TSI can be programmed as follows by programming OE_D16/31:

Table 13: local TDM Bus routing

OE_D16/31	PMC 1 local TDM D0-15 ←→ T8110 TDM	PMC 1 local TDM D16-31 ←→ T8110 TDM	PMC 2 local TDM D0-15 ←→ T8110 TDM	PMC 2 local TDM D16-31 ←→ T8110 TDM
0	D0-15	D16-31	D16-31	D16-31
1	D0-15 bused	D16-31 bused	D0-15 bused	D16-31 bused

OE_D16/31 = 0 is intended to be used with PMCs, which connect to the T8110 TSI with 16 TDM data lines each (like in a classical SCSA application). The N.A.T. NPMC-4E1 is such a module. In order to make use of all 32 TDM data lines of the T8110 for these modules also, the TDM data lines D0 – 15 of PMC2 are swapped onto the TDM data lines D16 – 31.

For OE_D16/31 = 1, all 32 TDM data lines of the PMCs are connected to the T8110 TSI, but they are bused. By setting this feature the user may not only distribute the number of TDM data lines from each PMC to the TSI freely, but may also specify a routing between the 2 PMC modules, without interference of the T8110.

Hence, for all applications NOT needing the compatibility mode to older **NcPCI PMC** versions, the setting OE_D16/31 = 1 is preferable.

5.8.9 Control / Status Register 5

Control / Status Register 5 is accessed with address offset 0x8 to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 14: Control / Status Register 4

Bit Number	Read/Write	Reset Value	Status Information / Control Setting
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R/W	GA3	Slot ID 4 signal of both PMC slots
Bit 4	R/W	GA2	Slot ID 3 signal of both PMC slots
Bit 3	R/W	GA1	Slot ID 2 signal of both PMC slots
Bit 2	R/W	GA0	Slot ID 1 signal of both PMC slots
Bit 1	R/W	0	Slot ID 0 signal of PMC slot 2
Bit 0	R/W	1	Slot ID 0 signal of PMC slot 1

This register allows the user to program a unique ID for each PMC module in the system. The ID definition complies to the Slot ID definition of the SCSA bus spec. By default, the upper 4 bits of the PMC ID is copied from the lower 4 bits of the cPCI Slot ID GA0 – GA3 (refer to chapter 5.8.5, Status Register 1).

5.8.10 Lattice Revision Status Register

The Lattice Hardware Revision Status Register is accessed with address offset 0xE to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 15: Board Hardware Revision Status Register

Bit Number	Read/Write	Status Information
Bit 7	R	Lattice CPLD revision
Bit 6	R	Lattice CPLD revision
Bit 5	R	Lattice CPLD revision
Bit 4	R	Lattice CPLD revision
Bit 3	R	Lattice CPLD revision
Bit 2	R	Lattice CPLD revision
Bit 1	R	Lattice CPLD revision
Bit 0	R	Lattice CPLD revision

5.8.11 Board Hardware Revision Status Register

The Board Hardware Revision Status Register is accessed with address offset 0xF to the base address programmed in the i21555 Mini Bridge Base Address Register, plus the address value given in Table 4: .

Table 16: Board Hardware Revision Status Register

Bit Number	Read/Write	Status Information
Bit 7	R	hardware PCB layout revision
Bit 6	R	hardware PCB layout revision
Bit 5	R	hardware PCB layout revision
Bit 4	R	hardware PCB layout revision
Bit 3	R	hardware PCB layout revision
Bit 2	R	hardware PCB layout revision
Bit 1	R	hardware PCB layout revision
Bit 0	R	hardware PCB layout revision

5.9 Port Pin Assignment of the Peripheral Devices

5.9.1 Port Pins of the T8110 H.110 TSI Controller

The T8110 H.110 Controller supplies an 8-bit parallel port, which is wired to the following control signals:

Table 17: Port Pins of the T8110 TSI Controller

Port Pin	Signal	Description
GP7	LED2.4	Front-Panel Led (green)
GP6	LED2.3	Front-Panel Led (yellow)
GP5	LED2.2	Front-Panel Led (orange)
GP4	LED2.1	Front-Panel Led (red)
GP3	LED1.4	Front-Panel Led (green)
GP2	LED1.3	Front-Panel Led (yellow)
GP1	LED1.2	Front-Panel Led (orange)
GP0	LED1.1	Front-Panel Led (red)

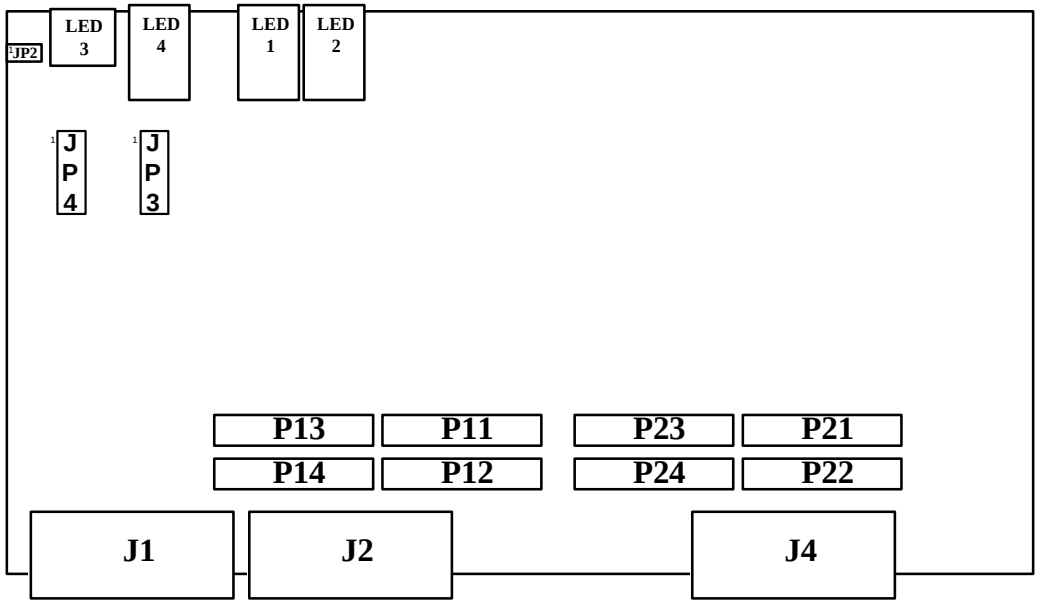
A bit value of “0” (logic low level) turns a LED on, a bit value of “1” (logic high level) turns it off.

See also Figure 5: for LED locations.

6 Connectors

6.1 Connector and Jumper Overview

Figure 5: Connectors and Jumpers of the NcPCI PMC



Please refer to the following tables to look up the pin assignment of the **NcPCI PMC**.

6.2 Connector JP2: Front Panel Ejector Switch

Table 18: Front Panel Ejector Switch

Pin No.	Signal
1	Switch Contact
2	nc
3	GND

The switch contact of the front panel ejector switch closes to GND, when pressed. Default position is open.

6.3 Connector JP3: JTAG chain of onboard Devices

Connector JP3 connects the onboard devices i21555 PCI bridge and T8110 TSI to a TDI – TDO daisy-chain JTAG chain. The device order in the chain is as described above.

Table 19: JTAG Chain of onboard Devices

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	nc	10

6.4 Connector JP4: CPLD Programming Port

Connector JP4 connects the JTAG- or programming-port of the Lattice CPLD devices. The CPLD devices are connected to a TDI – TDO daisy-chain.

Table 20: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	/ENABLE	10

6.5 PMC Slot 1 Connectors

6.5.1 PMC Slot 1 Connector P11

Table 21: PMC Slot 1 Connector P11

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A PMC1	4
5	/INT B PMC1	/INT C PMC1	6
7	/BUSMODE1 PMC1	+5V	8
9	/INT D PMC1	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK PMC1	GND	14
15	GND	/GNT PMC1	16
17	/REQ PMC1	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pin 3.3Vaux is not connected to the PMC slot. PCI signals /SDONE, and /SBO are not connected to other components, just pulled high. JTAG signal TCK is pulled low. V(I/O) pins are connected to +3.3V.

6.5.2 PMC Slot 1 Connector P12

Table 22: PMC Slot 1 Connector P12

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME PMC1	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL PMC1	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

JTAG signals TMS, TDI, and TDO are not connected to the PMC slot. JTAG signal /TRST is pulled low.

Signals labelled xxx PMCx are private for this PMC slot, signals without this attachment are bused to both PMC slots.

6.5.3 PMC Slot 1 Connector P13

Table 23: PMC Slot 1 Connector P13

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	PCI_RESV	GND	2
3	GND	/CBE7	4
5	/CBE6	/CBE5	6
7	/CBE4	GND	8
9	V (I/O)	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	V (I/O)	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	V (I/O)	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	V (I/O)	AD32	58
59	PCI_RESV	PCI_RESV	60
61	PCI_RESV	GND	62
63	GND	PCI_RESV	64

V(I/O) pins are connected to +3.3V.

6.5.4 PMC Slot 1 Connector P14 (PMC 1 I/O)

Table 24: PMC Slot 1 Connector P14

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
NC	1	I/O	I/O	2	CT_D15
CT_D14	3	I/O	I/O	4	CT_D13
CT_D12	5	I/O	I/O	6	GND
CT_D11	7	I/O	I/O	8	CT_D10
CT_D09	9	I/O	I/O	10	CT_D08
CT_D07	11	I/O	I/O	12	GND
CT_D06	13	I/O	I/O	14	CT_D05
CT_D04	15	I/O	I/O	16	CT_D03
CT_D02	17	I/O	I/O	18	CT_D01
GND	19	I/O	I/O	20	CT_D00
NC	21	I/O	I/O	22	/FSYNC_A
SREF_8K_A	23	I/O	I/O	24	SCLK_A
GND	25	I/O	I/O	26	/SCLKx2_A
SL_4	27	I/O	I/O	28	NC
SL_2	29	I/O	I/O	30	SL_3
SL_0_A	31	I/O	I/O	32	SL_1
NC	33	I/O	I/O	34	NC
NC	35	I/O	I/O	36	NC
NC	37	I/O	I/O	38	NC
NC	39	I/O	I/O	40	NC
CT_NETREF1_A	41	I/O	I/O	42	NC
NC	43	I/O	I/O	44	GND
NC	45	I/O	I/O	46	NC
NC	47	I/O	I/O	48	NC
NC	49	I/O	I/O	50	NC
GND	51	I/O	I/O	52	NC
NC	53	I/O	I/O	54	NC
NC	55	I/O	I/O	56	NC
GND	57	I/O	I/O	58	NC
NC	59	I/O	I/O	60	NC
NC	61	I/O	I/O	62	NC
NC	63	I/O	I/O	64	NC

6.5.5 PMC Slot 2 Connector P21

Table 25: PMC Slot 2 Connector P21

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A PMC2	4
5	/INT B PMC2	/INT C PMC2	6
7	/BUSMODE1 PMC2	+5V	8
9	/INT D PMC2	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK PMC2	GND	14
15	GND	/GNT PMC2	16
17	/REQ PMC2	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pin 3.3Vaux is not connected to the PMC slot. The same applies to PCI signals /SDONE, and /SBO. JTAG signal TCK is pulled low. V(I/O) pins are connected to +3.3V.

6.5.6 PMC Slot 2 Connector P22

Table 26: PMC Slot 2 Connector P22

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME PMC2	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL PMC2	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

JTAG signals TMS, TDI, and TDO are not connected to the PMC slot. JTAG signal /TRST is pulled low.

Signals labelled xxx PMCx are private for this PMC slot, signals without this attachment are bussed to both PMC slots.

6.5.7 PMC Slot 2 Connector P23

Table 27: PMC Slot 2 Connector P23

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	PCI_RESV	GND	2
3	GND	/CBE7	4
5	/CBE6	/CBE5	6
7	/CBE4	GND	8
9	V (I/O)	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	V (I/O)	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	V (I/O)	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	V (I/O)	AD32	58
59	PCI_RESV	PCI_RESV	60
61	PCI_RESV	GND	62
63	GND	PCI_RESV	64

V(I/O) pins are connected to +3.3V.

6.5.8 PMC Slot 2 Connector P24 (PMC 2 I/O)

Table 28: PMC Slot 2 Connector P24

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
NC	1	I/O	I/O	2	CT_D31
CT_D30	3	I/O	I/O	4	CT_D29
CT_D28	5	I/O	I/O	6	GND
CT_D27	7	I/O	I/O	8	CT_D26
CT_D25	9	I/O	I/O	10	CT_D24
CT_D23	11	I/O	I/O	12	GND
CT_D22	13	I/O	I/O	14	CT_D21
CT_D20	15	I/O	I/O	16	CT_D19
CT_D18	17	I/O	I/O	18	CT_D17
GND	19	I/O	I/O	20	CT_D16
NC	21	I/O	I/O	22	/FSYNC_B
SREF_8K_B	23	I/O	I/O	24	SCLK_B
GND	25	I/O	I/O	26	/SCLKx2_B
SL_4	27	I/O	I/O	28	NC
SL_2	29	I/O	I/O	30	SL_3
SL_0_B	31	I/O	I/O	32	SL_1
NC	33	I/O	I/O	34	NC
NC	35	I/O	I/O	36	NC
NC	37	I/O	I/O	38	NC
NC	39	I/O	I/O	40	NC
CT_NETREF1_B	41	I/O	I/O	42	NC
NC	43	I/O	I/O	44	GND
NC	45	I/O	I/O	46	NC
NC	47	I/O	I/O	48	NC
NC	49	I/O	I/O	50	NC
GND	51	I/O	I/O	52	NC
NC	53	I/O	I/O	54	NC
NC	55	I/O	I/O	56	NC
GND	57	I/O	I/O	58	NC
NC	59	I/O	I/O	60	NC
NC	61	I/O	I/O	62	NC
NC	63	I/O	I/O	64	NC

6.6 Compact PCI Backplane Connectors

The Compact PCI backplane connectors are 5 6-row connectors J1 A – F to J5 A – F. On the **NcPCI PMC** J3 and J5 are not populated. The 7th row Z does not connect to pins, but is just for shielding and completely connected to GND

6.6.1 Compact PCI Backplane Connector J1

Table 29: Compact PCI Backplane Connector J1 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	5V	-12V	nc
2	nc	5V	nc
3	/INTA	/INTB	/INTC
4	nc	/HEALTHY	V(I/O)_L
5	nc	nc	/RST
6	/REQ	GND	3.3V_L
7	AD30	AD29	AD28
8	AD26	GND	V(I/O)
9	/C/BE3	IDSEL	AD23
10	AD21	GND	3.3V
11	AD18	AD17	AD16
12	Key Area		
13			
14			
15	3.3V	/FRAME	/IRDY
16	/DEVSEL	GND	V(I/O)
17	3.3V	nc	nc
18	/SERR	GND	3.3V
19	3.3V	AD15	AD14
20	AD12	GND	V(I/O)_L
21	3.3V	AD9	AD8
22	AD7	GND	3.3V_L
23	3.3V	AD4	AD3
24	AD1	5V	V(I/O)
25	5V	/REQ64	/ENUM

Table 30: Compact PCI Backplane Connector J1 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	+12V	5V	GND
2	nc	nc	GND
3	5V_L	/INTD	GND
4	INTP	INTS	GND
5	GND_L	/GNT	GND
6	CLK	AD31	GND
7	GND_L	AD27	GND
8	AD25	AD24	GND
9	GND_L	AD22	GND
10	AD20	AD19	GND
11	GND_L	/C/BE2	GND
12	Key Area		
13			
14			
15	/BD_SEL	/TRDY	GND
16	/STOP	/LOCK	GND
17	GND_L	/PERR	GND
18	PAR	/C/BE1	GND
19	GND_L	AD13	GND
20	AD11	AD10	GND
21	M66EN	/C/BE0	GND
22	AD6	AD5	GND
23	5V_L	AD2	GND
24	AD0	/ACK64	GND
25	3.3V	5V	GND

6.6.2 Compact PCI Backplane Connector J2

Table 31: Compact PCI Backplane Connector J2 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	nc	GND	nc
2	nc	nc	nc
3	nc	GND	nc
4	V(I/O)	nc	/C/BE7
5	/C/BE5	/64EN	V(I/O)
6	AD63	AD62	AD61
7	AD59	GND	V(I/O)
8	AD56	AD55	AD54
9	AD52	GND	V(I/O)
10	AD49	AD48	AD47
11	AD45	GND	V(I/O)
12	AD42	AD41	AD40
13	AD38	GND	V(I/O)
14	AD35	AD34	AD33
15	nc	GND	nc
16	nc	nc	nc
17	nc	GND	nc
18	nc	GND	nc
19	GND	GND	nc
20	nc	GND	nc
21	nc	GND	nc
22	GA4	GA3	GA2

Table 32: Compact PCI Backplane Connector J2 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	nc	nc	GND
2	nc	nc	GND
3	nc	nc	GND
4	GND	/C/BE6	GND
5	/C/BE4	PAR64	GND
6	GND	AD60	GND
7	AD58	AD57	GND
8	GND	AD53	GND
9	AD51	AD50	GND
10	GND	AD46	GND
11	AD44	AD43	GND
12	GND	AD39	GND
13	AD37	AD36	GND
14	GND	AD32	GND
15	nc	nc	GND
16	GND	nc	GND
17	nc	nc	GND
18	GND	nc	GND
19	nc	nc	GND
20	GND	nc	GND
21	nc	nc	GND
22	GA1	GA0	GND

6.6.3 Compact PCI Backplane Connector J4

Compact PCI backplane connector J4 carries the H.110 bus signals.

Table 33: Compact PCI Backplane Connector J4 Rows A – C

Pin No.	Row A Signal	Row B Signal	Row C Signal
1	CT_D0	3.3V	CT_D1
2	CT_D4	CT_D5	CT_D6
3	CT_D8	CT_D9	CT_D10
4	CT_D11	5V	CT_D12
5	CT_D13	CT_D14	CT_D15
6	CT_D16	CT_D17	CT_D18
7	CT_D19	5V	CT_D20
8	CT_D21	CT_D22	CT_D23
9	CT_D24	CT_D25	CT_D26
10	CT_D27	3.3V	CT_D28
11	CT_D29	CT_D30	CT_D31
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	nc
22	nc	nc	nc
23	nc	nc	/CT_EN
24	GA4_J4	GA3_J4	GA2_J4
25	SGA4	SGA3	SGA2

Table 34: Compact PCI Backplane Connector J4 Rows D – F

Pin No.	Row D Signal	Row E Signal	Row F Signal
1	CT_D2	CT_D3	GND
2	CT_D7	GND	GND
3	GND	SCLKX2	GND
4	3.3V	SCLK	GND
5	3.3V	CT_NETREF2	GND
6	GND	CT_NETREF1	GND
7	GND	CT_C8B	GND
8	5V	CT_C8A	GND
9	GND	/FSYNC	GND
10	5V	CT_FRAMEA*	GND
11	V(I/O)	CT_FRAMEB*	GND
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	SGND**
22	nc	nc	SGND**
23	nc	nc	SGND**
24	GA1_J4	GA0_J4	SGND**
25	SGA1	SGA0	SGND**

* see chapter 7 on known bugs

** SGND is the protective GND of the board case and shielding, connected also to the front panel.

7 NcPCI PMC Programming Notes

7.1 Programming the PCI Bridges

7.1.1 Intel 21555 Bridge Programming

The Intel 21555 Bridge, which bridges between the Compact PCI bus and the internal PCI bus, is initialized by two ways: Power-Up configuration and EEPROM load of setup information on various Reset conditions.

7.1.1.1 Intel 21555 Power-Up Configuration

Power-Up configuration is done by pulling the data pins of the ROM interface to specific logic levels during Power-Up Reset. Details are found in the table below.

Table 35: Intel 21555 Power-Up Configuration

Data bit	Function	initialized to
PR_AD7	internal PCI bus central functions	enabled
PR_AD6	PCI arbiter internal PCI bus	enabled
PR_AD5	S_CLK_O	disabled
PR_AD4	Sync Mode	asynchronous
PR_AD3	Primary Lockout Reset Value	no lockout
PR_AD2	none	pulled high
PR_AD1	cPCI bus 64 bit enable	not used*

7.1.1.2 Intel 21555 Configuration by EEPROM Load

When reset, the i21555 loads several registers from EEPROM, if available. On the **NcPCI PMC**, a 93LC66A serial EEPROM is connected to the serial ROM interface of the i21555. The following data is loaded (please consult the i21555 User's Manual for a detailed description):

Table 36: i21555 EEPROM Configuration

Serial ROM Address	Hex Value															
0x0	80	00	00	00	00	80	06	00	00	02	06	00	00	00	80	06
0x10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0x20	00	00	00	00	00	00	F1	1F	00	00	00	FF	00	00	00	FF
0x30	00	08	00	00	00	00	7F	7F	00	00	00	00	00	00	00	00
0x40	00	40	00	FF	70	A5	10	00	02	06	00	00	01	00	00	00
0x50	00	00	00	00	00	00	00	00	FF	FF	FF	FF	FF	FF	FF	FF
0x60-0xFF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

Data bytes 0x0 – 0x42 are loaded into the i21555 as register setup. Data bytes from 0x44 up are N.A.T. coding of board parameters.

7.2 Programming the H.110 TSI Controller

The T8110 H.110 Timeslot Interchange Controller is located on the parallel ROM interface of the i21555 PCI bridge. Some setup information also resides in an EEPROM, which is loaded on Reset.

7.2.1 T8110 Configuration by EEPROM Load

The EEPROM connected to the T8110 is delivered empty (default), i.e. it reads 0xFF in all cells. This results in the T8110 ignoring it. Hence, all initialisation has to be done by external software. The user may program the EEPROM according to his needs.

7.2.2 T8110 local TDM bus Programming Examples

There are many different applications to which the bidirectional TDM bus between the T8110 TSI and the PMC modules may be adapted. In the following paragraphs, two possible and common applications are described, and the settings necessary for them.

The first example describes the connection to classical SCSA modules, i.e. with a SC4000 TSI device with 16 TDM data lines. Transmit and Receive data paths are set to be 8 bits wide each.

The second example describes the connection to modules with H.110 interface, i.e. with a CT812 TSI device with 32 TDM data lines. Due to compatibility reasons, SCbus protocol and control signal set is used, but the data bus is extended to 32 bits, in order to support H.110 standards. Transmit and Receive data paths are not restricted in use, and may be specified according to the user's needs.

7.2.2.1 T8110 connected to 2 PMCs with private SCbuses

The local TDM bus of the T8110 TSI has to be programmed to behave as an SCbus with clock master functionality, both PMC modules are supposed to be SCbus clock slaves, in order to achieve synchronisation. This is achieved by the following routing of T8110 local TDM signals to the SCbuses of the 2 PMC slots:

- T8110 TDM_D0-7 writes timeslot data to SCbus D0-7 of PMC module 1
- T8110 TDM_D16-23 writes timeslot data to SCbus D0-7 of PMC module 2

- PMC module 1 SCbus D8-15 writes timeslot data to T8110 TDM_D8-15
- PMC module 2 SCbus D8-15 writes timeslot data to T8110 TDM_D24-31

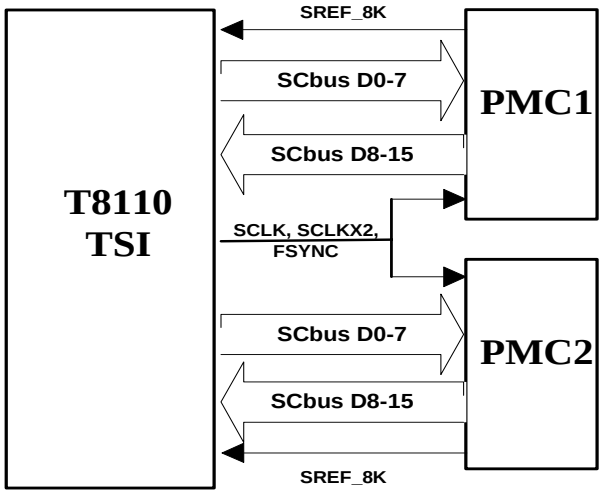
- T8110 local clock output LSC0 drives SCbus signal SCLK to PMC module 1
- T8110 local clock output LSC1 drives SCbus signal /SCLKx2 to PMC module 1
- T8110 local sync output FG0 drives SCbus signal /FSYNC to PMC module 1

- T8110 local clock output LSC2 drives SCbus signal SCLK to PMC module 2
- T8110 local clock output LSC3 drives SCbus signal /SCLKx2 to PMC module 2
- T8110 local sync output FG1 drives SCbus signal /FSYNC to PMC module 2

- PMC module 1 drives SCbus signal SREF_8K to T8110 LREF0 input
- PMC module 2 drives SCbus signal SREF_8K to T8110 LREF1 input
- PMC module 1 drives H.110 signal NETREF1_A to T8110 LREF2 input
- PMC module 2 drives H.110 signal NETREF1_B to T8110 LREF3 input

Figure 6: shows the local TDM bus and SCbus routing between T8110 and the PMC modules:

Figure 6: T8110 local TDM bus to private SCbus Routing



7.2.2.2 T8110 connected to 2 PMCs with a shared SCbus

The local TDM bus of the T8110 TSI has to be programmed to behave as an SCbus with clock master functionality, both PMC modules are supposed to be SCbus clock slaves, in order to achieve synchronisation. The routing of TDM data is not restricted. Please take into account that the bus is shared by the 2 PMC slots.

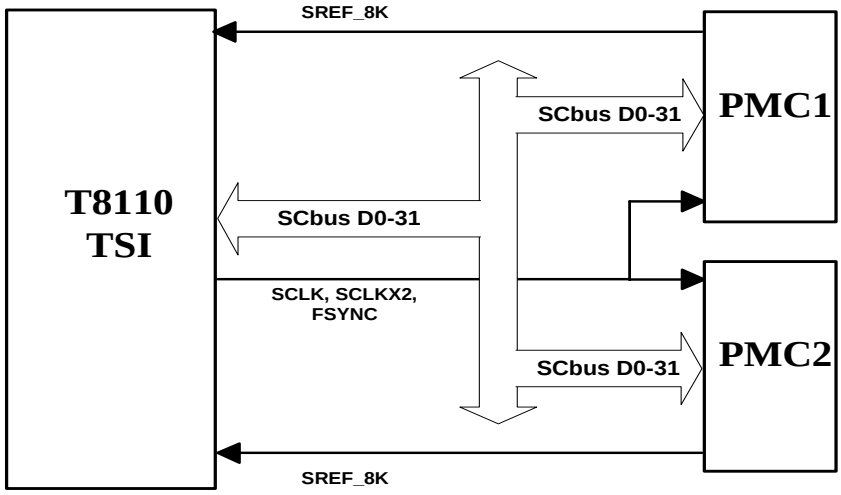
- T8110 local clock output LSC0 drives SCbus signal SCLK to PMC module 1
- T8110 local clock output LSC1 drives SCbus signal /SCLKx2 to PMC module 1
- T8110 local sync output FG0 drives SCbus signal /FSYNC to PMC module 1

- T8110 local clock output LSC2 drives SCbus signal SCLK to PMC module 2
- T8110 local clock output LSC3 drives SCbus signal /SCLKx2 to PMC module 2
- T8110 local sync output FG1 drives SCbus signal /FSYNC to PMC module 2

- PMC module 1 drives SCbus signal SREF_8K to T8110 LREF0 input
- PMC module 2 drives SCbus signal SREF_8K to T8110 LREF1 input
- PMC module 1 drives H.110 signal NETREF1_A to T8110 LREF2 input
- PMC module 2 drives H.110 signal NETREF1_B to T8110 LREF3 input

Figure 7: shows the local TDM bus and SCbus routing between T8110 and the PMC modules:

Figure 7: T8110 local TDM bus to shared SCbus Routing



8 Known Bugs and Restrictions

In hardware versions Rev. 1.0 – Rev. 1.2 of the NcPCI-PMC the H.110 bus signals FRAME_A and FRAME_B are swapped. As a software workaround enable both A and B signals on the clock master device, then the T8110 on the NcPCI-PMC will always lock correctly, no matter whether it synchronizes to A or B clocks. Fixed in Rev. 1.3 and higher.

The Board Hardware Revision Status Register as described in chapter 5.8.11 is available in Rev. 1.3 and higher.

The Lattice Revision Status Register as described in chapter5.8.10 is available in Rev. 2.0 and higher.

PMC module Slot ID programming as described in chapter 5.8.9 (Control / Status Register 5) is available in Rev. 2.0 and higher.

TDM bus routing as described in chapter 5.8.8.3 (TDM Bus Routing Switch Configuration Pin) is available in Rev. 2.0 and higher.

Appendix A: Reference Documentation

[1] Intel Corp., 21555 Non-Transparent PCI-to-PCI Bridge User Manual, July 2001
[2] Agere Systems, Ambassador T8110 PCI-based H.100/H.110 Switch and Packet Payload Engine, April 2001

Appendix B: Document's History

Revision	Date	Description	Author
	06.01.2003	initial version	ga
1.0	28.04.2003	corrections	ga
1.1	05.09.2003	chapter 7 Known Bugs added	ga
1.2	12.09.2003	table 31 corrected	ga
1.3	06.11.2003	chapter 6.2 TDM routing information added	ga
1.4	07.11.2003	table 24 TDM signals corrected	ga
1.5	15.12.2003	H.110 FRAME bug description added	ga
1.6	19.12.2003	adapted to HW Rev. 1.2	ga
1.7	02.09.2004	some amendments, Table 32 adapted	ga
1.8	03.05.2005	chapter 4.8.8 CTC8x_EN description corrected	ga
1.9	30.05.2005	Board Hardware Revision Status Register added	ga
2.0	28.09.2005	adapted to HW Rev. 2.0	ga
2.1	10.02.2006	'Statement on Environmental Protection' added	ga
2.2	06.06.2007	chapter 2.3.3 and 2.3.4 added	ga