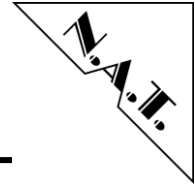


The NPMC-STM1 has been designed by:

**N.A.T. GmbH
Konrad-Zuse-Platz 9
D-53227 Bonn**

**Phone: +49 / 228 / 965 864 - 0
Fax: +49 / 228 / 965 864 - 10**

Internet: <http://www.nateurope.com>



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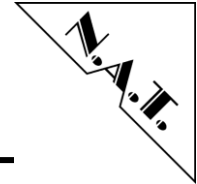
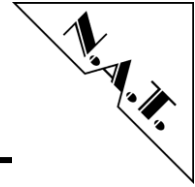


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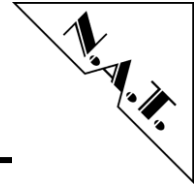
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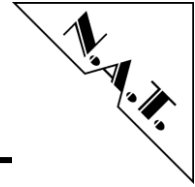
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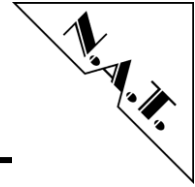
Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by a prefix *0x* (i.e. *0x1234*).

The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations:

Abbreviation	Description
b	bit
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 100000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SRAM	Static RAM
T1	1.544 Mbit G.703 Interface
SC-Bus	Time-Slot Interchange Bus of the SCSA
SCC	Serial Communication Channel of the MPC860
SCSA	Signal Computing System Architecture

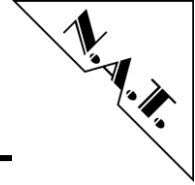


1 Introduction

The **NPMC-STM1** is a telecommunications interface board in PMC (PCI mezzanine card) form factor. It is targeted at telecom applications dealing with Synchronous Digital Hierarchy (SDH), such as SS7, ISDN or 3G/3.5G mobile applications in optical OC-3/STM-1 and SONET environments.

The **NPMC-STM1** is an ideal single board platform to interface between the frame oriented STM-1/SDH networks and classic TDM (**T**ime **D**ivision **M**ultiplex) standards as E1/T1/J1. Possible applications are i.e. add/drop multiplexer or terminal multiplexer. Equipped with a very efficient SDH-to-TDM cross mapping functionality the **NPMC-STM1** allows add/drop of all 63 E1 or 84 T1 payloads contained in a VC4 container of an STM-1 frame.

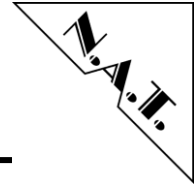
The **NPMC-STM1** provides this functionality on a single PMC form factor.



2 Overview

2.1 Major Features

- Dual Optical Interface for STM1/OC3 at 155Mbit/sec
- Add/Drop Multiplexer for 63E1/84T1 Channels
- H.110-Bus Interface on PMC P14 connector and P13 (PTMC Option)
- 63 E1 Framers or 84 T1 Framers
- Multiplexer cross connect between STM1 E1/T1 payload timeslots and H.110 timeslots
- PCI 2.1 standard compliant bus interface
- OPTIONS:
 - Single or Dual Optical Interface
 - Single – or Multi-Mode optical Transceiver
 - Monitoring Version (dual add/drop multiplexer) for concurrent Rx/Tx monitoring



2.2 Block Diagram

The following figure shows a block diagram of the **NPMC-STM1**.

Figure 1: NPMC-STM1 – Block Diagram V2.x – Overview

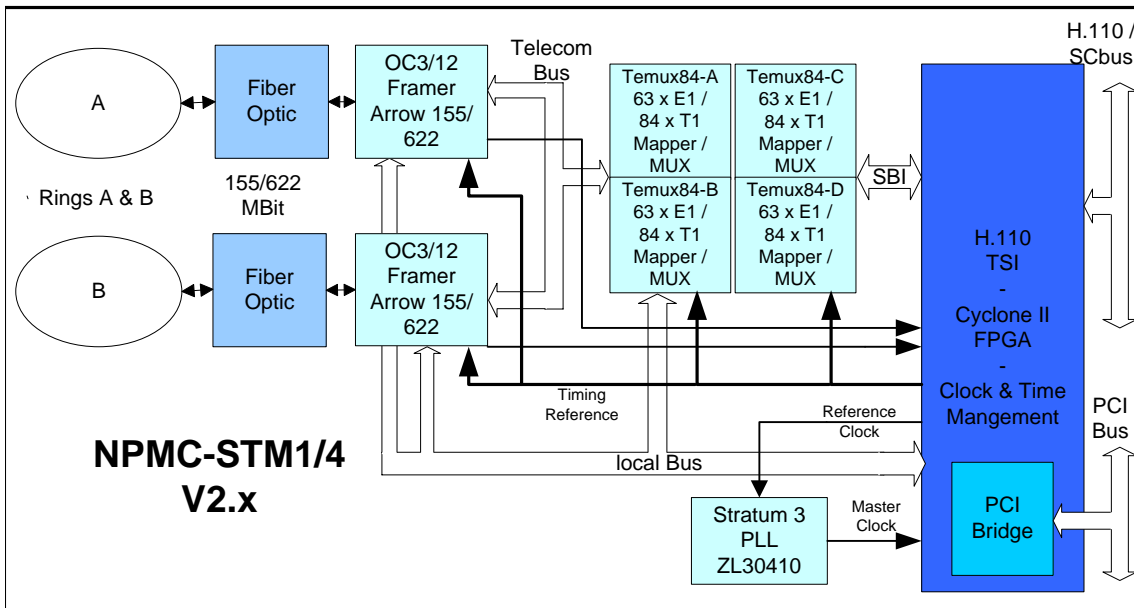
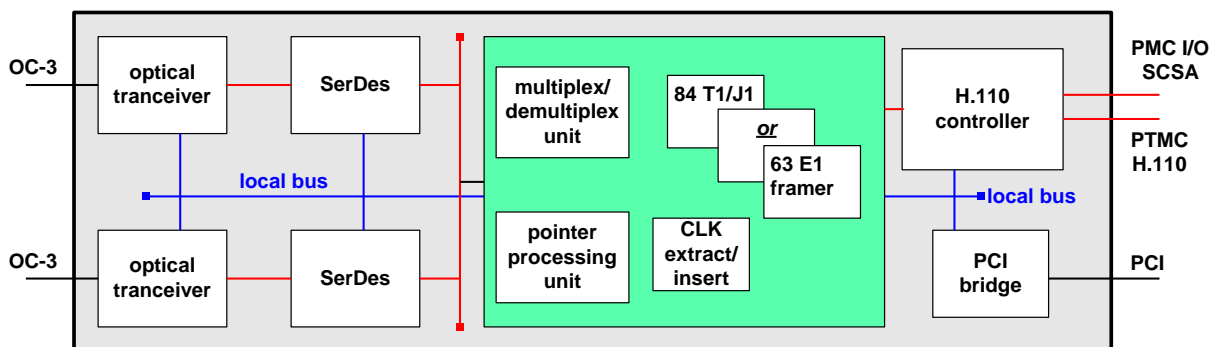
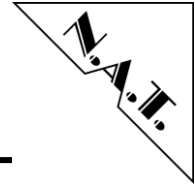


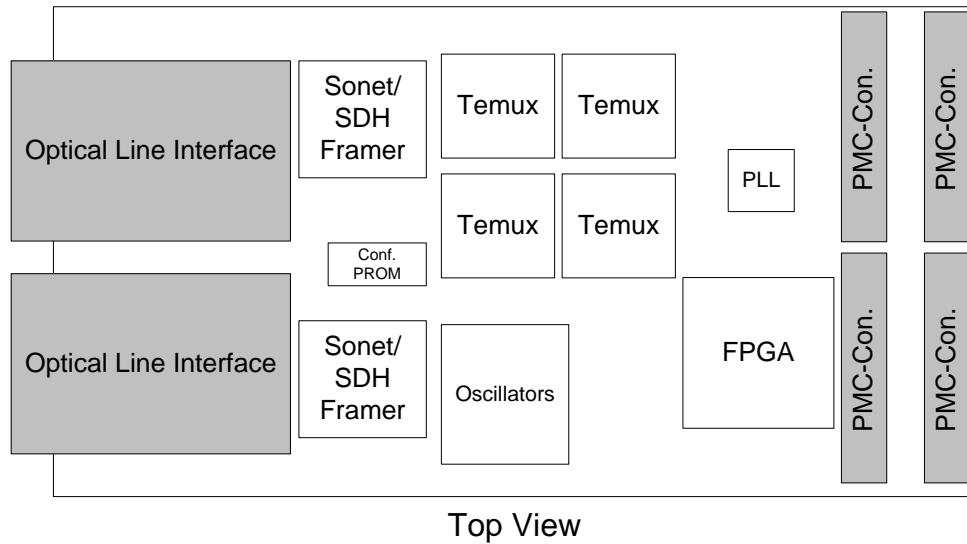
Figure 2: NPMC-STM1 – Block Diagram – Multiplexing Circuit

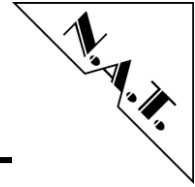




2.3 Location Overview

Figure 3: NPMC-STM1 – Location Diagram – Overview





3 Board Features

The **NPMC-STM1** is a standard form factor PMC module. It has a dual optical interface (OC-3/12) which is connected via framers (Arrow155) to the add/drop Multiplexer devices (Temux84). For standard applications only one Temux is required (OC-3) as the second optical ring acts as a backup ring. For monitoring applications or all applications where direct data access to both optical rings is required, a second add/drop multiplexer can be assembled.

When using in OC-12 applications all four Temux-84 chips need to be fitted. On the backplane side the E1 or T1 streams from both Temux chips are merged together into one TDM bus which interfaces to the H.110 timeslot FPGA chip.

3.1 Optical Interface

The two optical 155/622Mbps OC-3/12 STM-1 line interfaces are available on two standard OC-3/12 SDH/STM-1 connectors at the front panel. The STM1/OC3 interface consists of the Fiber Optic interface and the Sonet/SDH framer.

The PMC-Sierra device Arrow-155 works as Sonet/SDH framer. The Arrow-155 is a single port Sonet/SDH framer supporting the OC-3 (STM-1) data rates. It terminates section, line and path overhead of both the STS-n (AU-4) level and the TU-3 level. On the line side it incorporates a SERDES, allowing it to mate directly to an optics module.

The Arrow-155 maps/demaps up to three channels of DS3, E3, or EC-1 with bi-directional monitoring of traffic. The traffic may be multiplexed either into the system side or line side interfaces.

The system side interface is an 8-bit multi-drop parallel Telecom bus, allowing multiple devices to share a single bus.

3.2 VT/TU Access

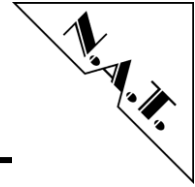
The two OC-3/STM1 framers are connected to an add/drop multiplexer/demultiplexer chipset. Since the chip performs the entire SDH pointer processing it is capable of accessing STS-1 SPEs (Synchronous Payload Envelopes), TUG3 tributary unit groups within in VC4 container as well as VC3 virtual containers and thus to extract/insert any of the 84 T1/J1 or 63 E1 streams including the respective clocking information contained in a single STM-1 SDH frame. Supported mappings are VT1.5/VT-2 to STS-1 SPE, TU-11/TU-12 to STM-1/VC3 or to TUG3 to STM-1/VC4.

The chip supports the M13 and G.747 multiplexing.

3.3 T1/J1/E1 Access

The multiplexer/demultiplexer chipset interfaces to 84 T1/J1 framers or 63 E1 timesliced framers, each having individual Rx/Tx, CLK and SYNC signals. For T1 the framing standards SF, SLC-96 and ESF, for E1 G.704 and G.706 (CRC-4 multiframe), for J1 the TTC JT-G.704 as well CRC-6 calculation are supported. Line and path performance are monitored.

The chip also provides full jitter attenuation and clock recovery.



3.4 H.110 Interface

The T1/J1/E1-Framers interface to the onboard H.110 controller. The H.110 controller allows flexible 64kbps timeslot routing between the various T1/J1/E1 streams as well as the selection of one of the T1/J1/E1-Clocks as the master clock for the TDM backplane bus. Thus it is possible to distribute all 84 T1/J1 or 63 E1 streams jitter-free and synchronised via the backplane.

The interface supports 8 MHz bus clock as well.

3.5 Backplane TDM Access

The onboard H.110 bus controller offers access to the backplane TDM bus supporting full the H.110 bus (PTMC) or the SC Bus subset on the PMC multi-purpose I/O connectors.

3.6 PCI-Interface

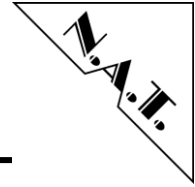
The **NPMC-STM1** is a P1386.1/Draft 2.0 compatible PMC module that can be plugged onto any VME, cPCI or other carrier board offering a PMC extension slot. It is PCI Rev. 2.2 compatible (32bit).

The PCI interface is a standard 32Bit/33MHz target interface contained in a FPGA. It supports 3.3V signaling and offers a 16 bit data / 16 bit address local bus interface as well as PCI interrupt support. It requires only 128 kByte address window in the PCI memory space.

The PCI-FPGA also contains a set of registers which control the operation of the **NPMC-STM1** Module.

3.7 Automatic Protection Switching (APS) Support

The Arrow-155 extracts and filters the K1/K2 bytes from three frames. The filtered K1/K2 bytes are accessible through the memory mapped registers of the framers. Error conditions detected within in K1/K2 bytes will lead to a device interrupt if not masked.

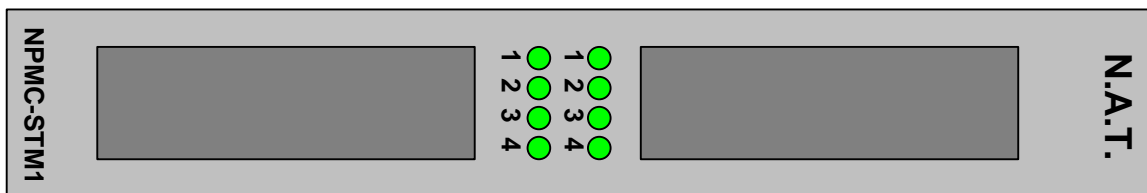


4 Hardware

4.1 Front Panel and LEDs

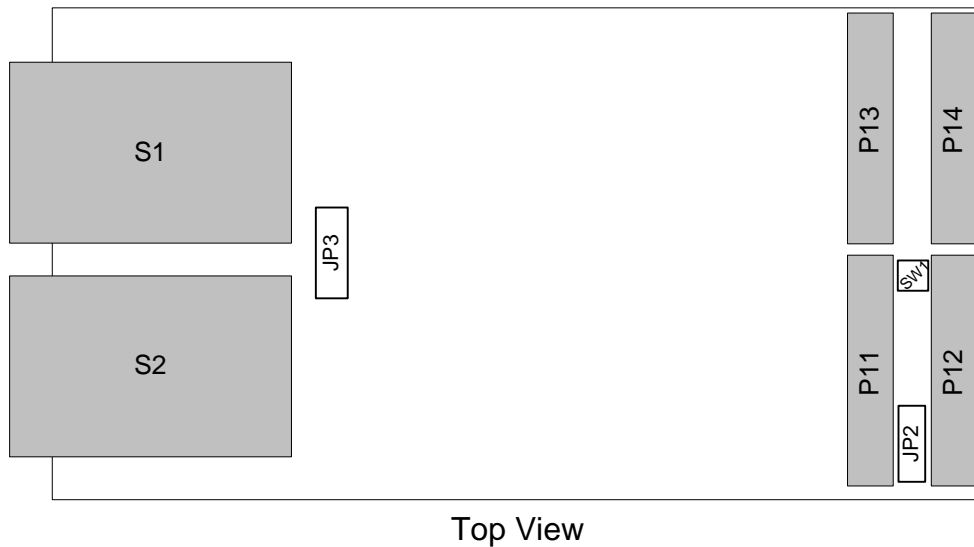
The **NPMC-STM1** module is equipped with 8 LEDs, which reflect the link status. They are mounted between the SDH connectors.

Figure 4: NPMC-STM1 – Front Panel

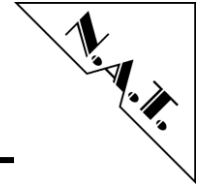


4.2 Connectors

Figure 5: NPMC-STM1 – Connector and Switch Location – Overview



Please refer to the following tables to look up the connector pin assignment of the **NPMC-STM1**.

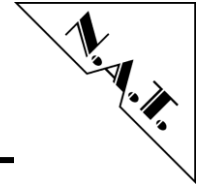


4.2.1 P11: PMC Connector

Table 2: P11: PMC Connector – Pin Assignment

Pin #	PCI-Signal	PCI-Signal	Pin #
1	TCK	-12V	2
3	GND	/INT A	4
5	/INT B	/INT C	6
7	/BUSMODE1	+5V	8
9	/INT D	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK	GND	14
15	GND	/GNT	16
17	/REQ	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SBO	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pins for -12V, Vaux, and V(I/O) are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but it 5V tolerant.

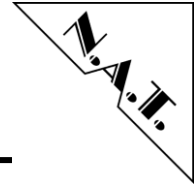


4.2.2 P12: PMC Connector

Table 3: P12: PMC Connector – Pin Assignment

Pin #	PCI-Signal	PCI-Signal	Pin #
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

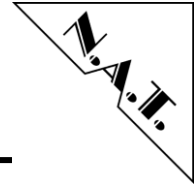
Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.



4.2.3 P13: PMC Connector – PTMC Option H.110

Table 4: P13: PMC Connector – Pin Assignment

ext. Signal	Pin #	Pin #	ext. Signal
CT_D26	1	2	GND
GND	3	4	-
CT_D24	5	6	-
CT_D22	7	8	GND
V(I/O)	9	10	CT_D31
GNDZ11	11	12	CT_D29
CT_D20	13	14	GND
GND	15	16	CT_D27
CT_FRAME_A	17	18	CT_D25
CT_FRAME_B	19	20	GND
V(I/O)	21	22	CT_D23
GNDZ23	23	24	CT_D21
CT_C8_A	25	26	GND
GND	27	28	CT_D19
CT_D18	29	30	CT_D17
CT_D16	31	32	GND
GND	33	34	CT_NETR2
CT_D14	35	36	CT_D30
CT_D12	37	38	GND
/PTEN	39	40	CT_D28
GNDZ41	41	42	CT_NETR1
CT_C8_B	43	44	GND
GND	45	46	CT_D15
CT_D10	47	48	CT_D13
CT_D8	49	50	CT_D11
GND	51	52	CT_D9
CT_D7	53	54	CT_D6
CT_D4	55	56	GND
-	57	58	CT_D5
CT_D2	59	60	CT_D3
CT_D1	61	62	GND
GND	63	64	CT_D1



4.2.4 P14: PMC Connector P14 – PMC I/O

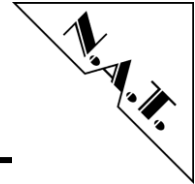
Table 5: P14: PMC Connector – Pin Assignment

ext. Signal	Pin #	Pin #	ext. Signal
MC	1	2	CT_D15
CT_D14	3	4	CT_D13
CT_D12	5	6	GND
CT_D11	7	8	CT_D10
CT_D09	9	10	CT_D8
CT_D07	11	12	GND
CT_D06	13	14	CT_D5
CT_D04	15	16	CT_D3
CT_D02	17	18	CT_D1
GND	19	20	CT_D0
CLKFAIL	21	22	/FSYNC
SREF_8K	23	24	SCLK
GND	25	26	/SCLKx2
-	27	28	-
-	29	30	-
-	31	32	-
-	33	34	-
-	35	36	-
-	37	38	CT_FRAME B
CT_FRAME_A	39	40	CT_NETREF2
CT_NETREF1	41	42	-
-	43	44	GND
CT_C8_B	45	46	CT_C8_A
CT_D16	47	48	CT_D17
CT_D18	49	50	CT_D19
GND	51	52	CT_D20
CT_D21	53	54	CT_D22
CT_D23	55	56	CT_D24
GND	57	58	CT_D25
CT_D26	59	60	CT_D27
CT_D28	61	62	CT_D29
CT_D30	63	64	CT_D31

The SCbus implemented on the **NPMC-STM1** is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15.

4.2.5 S1/S2: Front Panel Connectors

The two optical front panel connectors S1 and S2 have standard SC-plugs and can be equipped with either singlemode or multimode transceivers.



4.2.6 JP2: JTAG Connector

This JTAG port connects to the JTAG interfaces of the Arrow and Temux devices which are configured in a daisy chain.

Table 6: JP2: JTAG Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	TCK	GND	2
3	TDO	+3,3V	4
5	TMS	nc	6
7	nc	nc	8
9	TDI	GND	10

4.2.7 JP3: Altera FPGA Programming Port

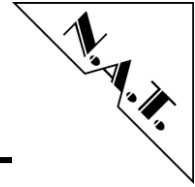
Connector JP3 connects to the programming-port of the Altera FPGA device.

Table 7: JP3: FPGA Programming Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	DCKL_U13	GND	2
3	CONF_DONE	+3,3V	4
5	nCONFIG	nCE	6
7	DATA0_U13	nCS0	8
9	ASDI	GND	10

4.2.8 DIP SW1: Dip Switch for testing purpose

Switch DIP SW1 is for development and testing purpose only and not intended to be used by the customer.



5 Memory Map

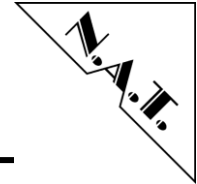
The following table gives a detailed overview of the internal address map of the **NPMC-STM1**. All addresses are given as offsets to the PCI memory space base address. In total the **NPMC-STM1** requires a PCI memory window of 128Kbyte.

Table 8: The Memory Map

Address Offset	Device	Access	Comments
0x00000	PCI-FPGA	16 Bit r/w	Board Configuration and Status Registers
0x00040	FPGA-PROM	16 Bit r/w	Register Interface to Access FPGA-PROM
0x04000	TSI-FPGA	16 Bit r/w	H.110 Controller and Timeslot Multiplexer
0x08000	Arrow-155-A	16 Bit r/w	Sonet/SDH Framer – A Ring
0x0c000	Arrow-155-B	16 Bit r/w	Sonet/SDH Framer – B Ring
0x10000	Temux84-A	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -
0x14000	Temux84-B	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -
0x18000	Temux84-C	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -
0x1c000	Temux84-D	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -

For a detailed description of the Temux84 and Arrow-155 registers, please refer to the respective manuals of these chips.

The board configuration and status registers which are contained in the Altera FPGA are described within the following sections.



5.1 Board Configuration and Status Registers

5.1.1 Register Overview

The following table gives an overview of all registers contained in the Altera FPGA:

Table 9: FPGA Registers

Address	Reset Value	Name	Description
0x00	0x0000	MISC	Misc Control and Status
0x02	0x0000	VER	Version Register
0x04	0x0000	IRQ_Mask	Interrupt Mask Register
0x06	0x0000	IRQ_Stat	Interrupt Status Register
0x08	0x0000	PLL_CSR	PLL Control/Status Register
0x0A	0x1110	LED	Led Control Register

5.1.2 MISC - Misc Control and Status Register

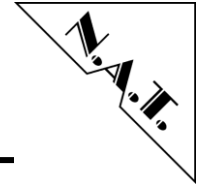
The MISC register contains some general purpose control and status registers

Table 10: MISC Control Register

MISC - Address 0x00																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Reset

Table 11: MISC Register Bits

Bit	Name	Function
0	Reset	Write 1 to initiate a Reset to all onboard devices; the reset bit should be set for at least 100ms before clearing it again



5.1.3 Version Register

The Version Register shows the actual PCB and FPGA releases.

Table 12: Version Register

Version - Address 0x02																
Default value 0x2110																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	PCB Version								FPGA Version							

5.1.4 IRQ_Mask - Interrupt Mask Register

The Interrupt Mask Register allows the individual masking of the interrupt sources. Interrupt sources which are enabled are wired or'ed to the PCI INTA pin, thus leading to a PCI interrupt. The source for the interrupt can be read from the IRQ_Stat register.

The meaning of the individual bits is explained in the following table.

Table 13: IRQ_Mask Register

IRQ_Mask - Address 0x04																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	-	-	-	-	-	-	-	-	IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1	IRQ 0

0 = Interrupt is disabled

1= Interrupt is enabled

5.1.5 IRQ_Stat - Interrupt Status Register

By means of the IRQ_Stat register the status of the interrupt lines of the individual onboard interrupt sources can be determined. The value of a bit does not depend on the setting of the corresponding bit in the IRQ_Mask register. If a bit in the IRQ_Stat register is set and the corresponding bit in the IRQ_Mask register is enabled, the PCI interrupt line INTA will be activated.

The following table shows the assignment of the register bits.

Table 14: IRQ_Stat Register

IRQ_Stat - Address 0x06																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	-	-	-	-	-	-	-	-	IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1	IRQ 0

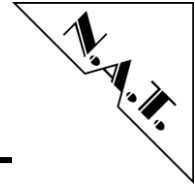


Table 15: IRQ_Stat Register Bits

Bit	Name	Function
0	IRQ0	Arrow-A interrupt active
1	IRQ1	Arrow-B interrupt active
2	IRQ2	Temux-84-A interrupt active
3	IRQ3	Temux-84-B interrupt active
4	IRQ4	Temux-84-C interrupt active
5	IRQ5	Temux-84-D interrupt active
6	IRQ6	TSI interrupt active. This bit is cleared by any write operation to the IRQ_STAT register.
	IRQ7	PLL State change, any change in bits HOLDOVER, LOCK, PRIOR, SECOR will lead to an interrupt. This bit is cleared by any write operation to the IRQ_STAT register.

5.1.6 PLL Control and Status Register

The PLL Control Register configures the main 77.76MHz Telecom clock configuration. The status of the PLL can be read on the upper half of the register.

Table 16: PLL_CSR Register

Clk_Cntr - Address 0x08																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-		Secor	Prior	HoldOver	Lock	-	EXT_REF			PLL_Mode		CLK77_REF	

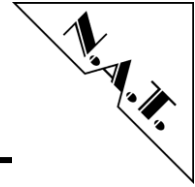


Table 17: PLL_CSR - Register Bits

Bit	Name	Function
[1..0]	CLK77_REF	Reference select for the internal 77.6MHz master clock 0x0 - 77.6MHz Crystal Oscillator – free running 0x1 - Arrow-A 0x2 - Arrow-B 0x3 - EXT_REF
[3..2]	PLL_Mode	Main PLL Mode Selection 0x0 - Normal Mode 0x1 - Holdover Mode 0x2 - Free running Mode 0x3 - reserved
[6..4]	EXT_REF	0x0 - CT_C8_A 0x1 - CT_C8_B 0x2 - CT_NetR1 0x3 - CT_NetR2 0x4 - SC_SCLK 0x5 - SC_SREF_8K 0x6 - unused 0x7 - unused
8	Lock	PLL is locked to primary or secondary reference clock
9	Hold Over	PLL is in transition state (lock not yet achieved)
10	Prior	Primary clock out of lock m(see Note*)
11	Secor	Secondary clock out of lock (see Note*)

***) Note:** The primary PLL clock input selection is made by bits CLK77_REF, the secondary PLL clock input is used for the external reference signals (CLK77_REF=3).

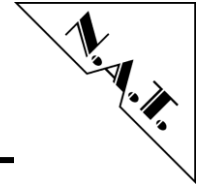
5.1.7 LED-Control Register

The LED-Control Register is used to switch on/off the 8 front panel leds.

Table 18: LED Control Register

LED - Address 0x0A																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acc.	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	Led 8	Led 7	Led 6	Led 5	Led 4	Led 3	Led 2	Led 1

1 = Led is on
0 = Led is off



5.2 FPGA-PROM Access

The FPGA’s configuration PROM holds the bit stream that configures the FPGA at power-up. The free space above this configuration bit stream is used to store the board’s serial and identification number. The PROM can be read indirectly via the register interface described below.

Table 19: Memory Map

Register	Address Offset Byte 4-Byte aligned	Function
Addr_0	0x0 / 0x00	Address bits[7..0]
Addr_1	0x1 / 0x04	Address bits[15..8]
Addr_2	0x2 / 0x08	Address bits[23..16]
Data_Wr	0x3 / 0x0C	Data to be written in AS-PROM (when asserting shift_in-, and then write trigger)
CSR	0x4 / 0x10	Control Status Register, can be written to trigger actions, can be read to read Info-bits
Data_Rd	0x5 / 0x14	Last Data read from AS-PROM (after read trigger)
Chip_Status	0x6 / 0x18	Last (Chip-internal) Status Register content read from AS-PROM (after read_status trigger)
Chip_Id	0x7 / 0x1C	Silicon-Id of AS-PROM (after read_sid trigger)

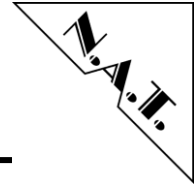
Reading bytes from the PROM is done by executing the following sequence on the registers:

First, the desired address within the PROM has to be written to the three address registers. Then the Control/Status Register (CSR) must be written with 0x10 to trigger reading from the device. By polling for the busy-bit (reading bit 0 of the CSR) completion of the read cycle can be determined. The addressed byte can then be read from the Data_Rd register.

Refer to the chapters below for a detailed description of every register.

NOTE:

Write operations to the PROM are only possible after a special unlock sequence has been executed. **Please do NOT write to the PROM, because this would corrupt the FPGA’s configuration bit stream.**



5.2.1 CSR Register

Writing a '1' to **one** of the bits in the Trigger/Info register triggers one of the actions described below.

Reading the Trigger/Info register returns the values of the Info-bits described below.

Table 20: CSR Register

CSR - Address 0x4 / 0x10			
Bit Number	Mask for Access	Read Access	Write Access
7	0x80	-	shift_in
6	0x40	buffer_len[2]	read_sid
5	0x20	buffer_len[1]	read_status
4	0x10	buffer_len[0]	read
3	0x08	illegal_erase	write
2	0x04	illegal_write	sector_protect
1	0x02	data_valid	sector_erase
0	0x01	busy	bulk_erase

Table 21: Control bits

Trigger bit	Triggered Action
shift_in	Initiates shifting in the data-byte previously written to the Data_In register into the write-buffer.
read_sid	Initiates reading the Silicon-ID from the AS-PROM and storing it in the Id_Out register.
read_status	Initiates reading the Status-Register from the AS-PROM and storing it in the Status_Out register.
read	Initiates reading of the byte addressed via the Addr_In_0/1/2 registers and storing it in the Data_Out register.
write	Initiates writing the bytes previously shifted into the write buffer to start-address present in the Addr_In_0/1/2 registers.
sector_protect	Initiates protecting/unprotecting AS-PROM sectors dependant on the value stored in the Data_In register.
sector_erase	Initiates erasing of the AS-PROM sector the address stored in Addr_In_0/1/2 is within.

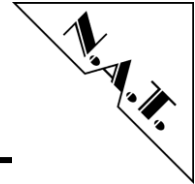


Table 22: Status bits

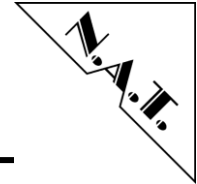
Trigger bit	Triggered Action
buffer_len[2..0]	The static value read in these bits determines the length of the write buffer: length = 2 exp (buffer_len + 1)
illegal_erase	A '1' in conjunction with the busy-bit being active shows that the current erase-action tries to erase a protected sector.
illegal_write	A '1' in conjunction with the busy-bit being active shows that the current write-action tries to write to a protected sector.
data_valid	A '1' shows that the Data_Out register contains valid data from the AS-PROM.
busy	A '1' shows that the device is still busy with processing the last command.

5.2.2 Chip_Status Register

This register holds the content of the AS-PROM's Status-Register after a read_status command has been executed.

Table 23: Chip_Status Register

Chip_Status - Address 0x6 / 0x18		
Bit Number	Shortcut	Description
7	-	-
6	-	-
5	-	-
4	BP2	Block Protect 2
3	BP1	Block Protect 1
2	BP0	Block Protect 0
1	WEL	Write Enable Latch
0	WIP	Write In Progress



5.2.3 Data_Wr Register during sector_protect

If the sector_protect command is triggered, the value stored in the Data_Wr Register determines which sectors to protect/unprotect.

NOTE:

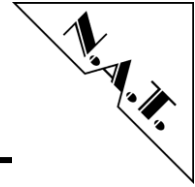
It is bit-reversed compared to the Chip_Status register (due to bit-reversal in Altera-Code).

Table 24: Data_Wr during sector_protect

Data_Wr - Address 0x3 / 0x0C		
Bit Number	Shortcut	Description
7	X	-
6	X	-
5	BP0	Block Protect 0
4	BP1	Block Protect 1
3	BP2	Block Protect 2
2	X	-
1	X	-
0	X	-

Table 25: BP[2..0] values for EPCS4 and EPCS16

BP[2..0]	EPCS4		EPCS16	
	Protected Memory Area	Unprotected Memory Area	Protected Memory Area	Unprotected Memory Area
000	none	all sectors (0 to 7)	none	all sectors (0 to 31)
001	sector 7	sectors 0 to 6	sector 31	sectors 0 to 30
010	sectors 6 and 7	sectors 0 to 5	sector 30 and 31	sectors 0 to 29
011	sectors 4 to 7	sectors 0 to 3	sectors 28 to 31	sectors 0 to 27
100	all sectors (0 to 7)	none	sectors 24 to 31	sectors 0 to 23
101	all sectors (0 to 7)	none	sectors 16 to 31	sectors 0 to 15
110	all sectors (0 to 7)	none	all sectors (0 to 31)	none
111	all sectors (0 to 7)	none	all sectors (0 to 31)	none



5.3 TSI FPGA

The TSI FPGA replaces the Zarlink TSI chip of version V1.x. The timeslots are routed from the SBI bus interface of the 4 Temux chips to the H.110 bus and vice versa. On the one side the TSI FPGA directly connects to the SBI bus of the TEMUX devices and on the other side to the H.110 backplane bus.

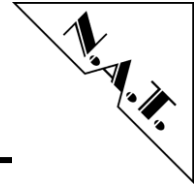
The SBI bus operates in synchronous mode only in the application.

5.3.1 TSI FPGA Register Overview

The following table gives an overview of all registers contained in the TSI FPGA:

Table 26: FPGA Registers

Address	Reset Value	Name	Description
0x00	0x0000	VER	Version Register
0x02	0x0000	MISC	Misc. Control Register
0x04	0x0000	SBIA	SBI TS Address
0x06	0x0000	CTOE	CTbus/H.110 bus Timeslot OE control
0x08	0x0000	SYNC_CNT	SYNC Align Count
0x0A	0x0000	-	-
0x0C	0x0000	IDLE	IDLE Pattern Register
0x0E	0x0000	-	Unused
0x10	0x0000	Drop Bus TS Routing Reg. A	Drop Routing Data Register for Temux A
0x12	0x0000	Drop Bus TS Routing Reg. B	Drop Routing Data Register for Temux B
0x14	0x0000	Drop Bus TS Routing Reg. C	Drop Routing Data Register for Temux C
0x16	0x0000	Drop Bus TS Routing Reg. D	Drop Routing Data Register for Temux D
0x18	0x0000	Add Bus TS Routing Reg. A	Add Routing Data Register for Temux A
0x1A	0x0000	Add Bus TS Routing Reg. B	Add Routing Data Register for Temux B
0x1C	0x0000	Add Bus TS Routing Reg. C	Add Routing Data Register for Temux C
0x1E	0x0000	Add Bus TS Routing Reg. D	Add Routing Data Register for Temux D



5.3.2 FPGA Type Register

The Type Register shows the FPGA type related to its functionality. Until now the following types are available:

- 0x0: regular TSI implementation
- 0x2: substrate TSI implementation
- 0x3: TSI over PCI DMA engine implementation

Table 27: Version Register

Version - Address 0x00																
Default value 0x1110																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func									FPGA Type							

5.3.3 MISC - Misc Control and Status Register

The MISC register contains some general purpose control and status registers

Table 28: MISC Control Register

MISC - Address 0x02																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	bu sy	-	-	-	-	-	-	-	EN _S RE F8 K	EN _S CL K	CLK _RE F1	CLK _RE F0	EN_ NET R2	EN_ NET R1	EN_ C LK_ B	EN_ CLK _A

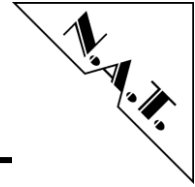


Table 29: MISC Register Bits

Bit	Name	Function
15	BUSY	A read operation on the routing memory is pending. The operation is complete when this bit is cleared, the result of the read operation is available when this bit is cleared. A read operation is initiated by writing an address to the <i>SBI Address Register</i>
7	EN_SREF_8K	Enable driving of SREF_8K Signal to SCbus
6	EN_CLK_S	Enable driving of SCLK and FSYNC to SCbus
5..4	CLK_REF [1..0]	H.110 Clock Reference selection: 11: H.110 clocks B 10: H.110 clocks A 01: SC_SCLK 00: internal clock – free running or OC-3 reference
3	EN_NETR2	Enable driving of NETR2 signal to H.110 bus
2	EN_NETR1	Enable driving of NETR1 signal to H.110 bus
1	EN_CLK_B	Enable driving of B Clocks to H.110 bus
0	EN_CLK_A	Enable driving of A Clocks to H.110 bus

5.3.4 SBI Address Register

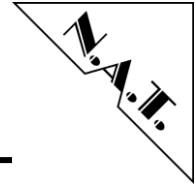
The SBI Address register defines the address of a timeslot on the SBI bus for a succeeding read or write command to the routing memory via register [10..18]. The routing memory for each Temux84 is divided into 9 rows of 270 columns each. Columns 0-13 cannot be addressed as they are not used on the SBI bus. So the effective address [C7..C0] = 0 selects TS14 (counting from zero).

Table 30: SBI Address Register

SBIA - Address 0x04																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	R3	R2	R1	R0	C7	C6	C5	C4	C3	C2	C1	C0

Table 31: SBI Address Register Bits

Bit	Name	Function
[R3..R0]	Row Addr	SBI TS row address [0..8]
[C7..C0]	Column Addr	SBI TS Column address [0..255] = TS[14..269]



5.3.5 H.110 Output Control Register

By means of the H.110 Output Control Register a certain TS on the H.110 can be defined as an output or input.

Table 32: CTOE Register

CTOE Register - Address 0x06																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 33: CTOE Control Register Bits

Bit	Name	Function
EN	Enable	1= TS is Output 0 = TS is Input / Unused
P[4..0]	Port	H.110 Port number (0..31)
[TS6..TS0]	TS Num	H.110 TS number (0..127)

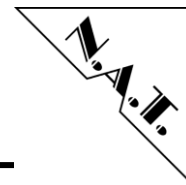
5.3.6 Idle Pattern Register

The Idle Pattern Register defines a value to be sent to the SDH-Add bus in all unused timeslots.

Table 34: Idle Pattern Register

IDLE - Address 0x0C																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	-	-	-	-	-	-	-	-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit[7..0] = Idle pattern to be used



5.3.7 Add/Drop Bus Timeslot Routing Register

The Add/Drop Bus Timeslot Routing Register together with SBI Address Register defines the routing of timeslots between the SBI bus and the H.110 bus. The register contains the Timeslot/Port on the H.110 where the data from the SBI bus shall be placed (Drop) or taken from and send to the SBI bus (Add).

The timeslot location on the SBI bus is defined by the SBI Address Register.

In case of a read command the data is not valid before the BUSY bit in the MISC register is cleared.

There are 4 DROP routing data registers and 4 ADD routing data registers. The SBI bus contains the multiplexed data of 4 Temux devices. Each pair of Drop and Add routing data registers is assigned to one of the 4 Temux devices.

The meaning of the individual bits is explained in Table 43:

Table 35: Drop Bus TS Routing Register - Temux A

DTSRA - Address 0x10																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 36: Drop Bus TS Routing Register - Temux B

DTSRB - Address 0x12																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 37: Drop Bus TS Routing Register - Temux C

DTSRC - Address 0x14																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

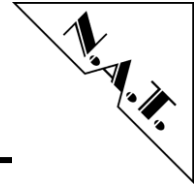


Table 38: Drop Bus TS Routing Register - Temux D

DTSRD - Address 0x16																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 39: Add Bus TS Routing Register - Temux A

ATSRA - Address 0x18																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 40: Add Bus TS Routing Register - Temux B

ATSRB - Address 0x1A																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 41: Add Bus TS Routing Register - Temux C

ATSRC - Address 0x1C																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 42: Add Bus TS Routing Register - Temux D

ATSRD - Address 0x1E																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W	R/ W
Func	EN	-	-	P4	P3	P2	P1	P0	-	TS6	TS5	TS4	TS3	TS2	TS1	TS0

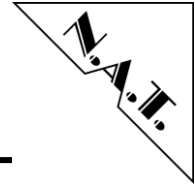
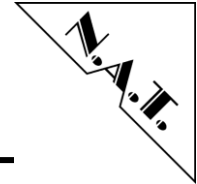


Table 43: Add/Drop TS Routing Register Bits

Bit	Name	Function
EN	Enable	1= TS is Output 0 = TS is Input / Unused
P[4..0]	Port	H.110 Port number (0..31)
[TS6..TS0]	TS Num	H.110 TS number (0..127)



6 Board Specification

Table 44: NPMC-STM1 – Features

PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to local bus bridge	Altera EP2C35F484 FPGA, 33MHz PCI Clock, 3.3V Signaling
STM1 Interface	2 Fiber Optic Interfaces for STM1 / OC-3/12 155/622 Mbit/sec, front-panel connectors
Add/drop Multiplexer	2 x 63E1 Channels or 2 x 84 T1 channels
H.110 Bus	H.110 Universal timeslot Interchange on PMC-I/O connector or PTMC connector (P13)
Firmware	n.a.
Power consumption	5.0V: 0.5A 3.3V: 2A (fully equipped)
Operating Temperature	0° C - +50 °C, forced air cooling required
Storage Temperature	-10 °C - +85°C
Humidity	10 % - 90 % non-condensing
Standards compliance	PCI Rev. 2.1 P1386.1 / Draft 2.0

6.1 NPMC-STM1 Order Codes

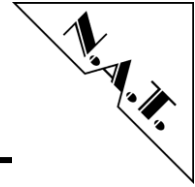
The order codes for **NPMC-STM1** are organized according to the following scheme:

NPMC-STM1-I-N-P

The following table shows the meanings of the used abbreviations:

Table 45: NPMC-STM1 – Order Codes

Abbreviation	Description	Option
I	Optical Interface Type	M=Multi Mode S= Single Mode
N	Number of add/drop Multiplexers	1= Single Temux equipped, second optical interface used as backup 2= Dual Temux equipped (Monitoring Version) (* see Note)
P	PTMC Option	P=PTMC Connector (P13) equipped



7 Installation

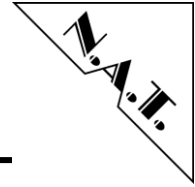
7.1 Safety Note

To ensure proper operation of the **NPMC-STM1** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and removal can damage the circuits or shorten their lifetime.

- Before installing or deinstalling the **NPMC-STM1**, read the Installation Guide and the User's Manual for the PMC carrier board
- Before touching integrated circuits, take all the necessary precautions for handling electrostatic devices.
- Ensure that the **NPMC-STM1** is connected to the carrier board with all three PMC connectors properly seated and that the power is available (GND, +5V, and +3.3V).
- 3.3V signaling is mandatory for the PCI interface as well as for the H.110 interface.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is screwed to the front panel, VME or cPCI rack and
 - shielded by a closed housing.



7.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-STM1**
- power supply

7.2.2 Power supply

The power supply for the **NPMC-STM1** must meet the following specifications:

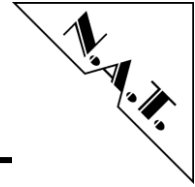
- required for the module:
 - +3,3V / 2.0A typical (fully equipped)
 - +5,0V / 0.5A typical

7.2.3 Automatic Power Up

In the following situations the **NPMC-STM1** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
 - when +5V voltage level drops below 4,4V *
 - when +5V voltage level rises above 5,6V *
 - when +3.3V voltage level drops below 2,65V *
 - when +3.3V voltage level rises above 3,9V *
 - or when the carrier board signals a PCI Reset
- Watchdog (if enabled)

* defined by: "PCI Specification Revision 2.2, Section 4.2.1.1 and Section 4.3.2"



7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

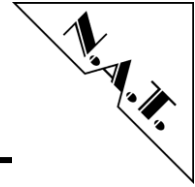
Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronic equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.



If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

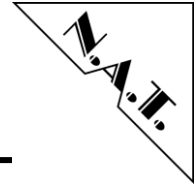
Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies to EN60950 and UL1950.

7.3.5 Compliance to REACH

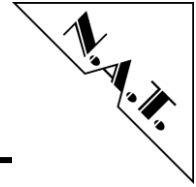
The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.



Appendix A: Version 1.x to 2.x Hardware Differences

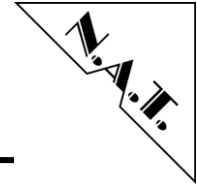
The NPMC-STM1 V2.x Hardware differs from version V1.x on the following items:

- New FPGA based TSI chip (replaces Zarlink + MVIP FPGA)
- Support for up to 4 Temux chips (OC-12)
- T1 routing limitations of Zarlink TSI chip removed due to new FPGA



Appendix B: Reference Documentation

- [1] Zarlink: MT90866 Data Sheet
- [2] PMC Sierra: PM8316 - TEMUX84 Register Description, Issue March 2004
- [3] PMC Sierra: PM8316 - TEMUX84 Programmers Guide, Issue No. 4: Sep. 2003
- [4] PMC Sierra: PM5318/5320 - Arrow622/155 Operation and Configuration Guide Issue No.2, Jul 2004
- [5] PMC Sierra: PM5318/5320 - Arrow155 Register Description, Issue No.2, Jul 2004



Appendix C: Document's History

Version	Date	Description	Author
1.0	1.7.04	Initial Version	hl
1.1	31.1.2005	Reworked	hl
1.2	1.12.2005	Added change for NPMC-STM1 V2.0	hl
2.0	1.3.2006	V2.x Hardware manual separated from V1.x	hl
2.1	10.11.2006	Added documentation for FPGA PROM access	te
2.2	15.2.2008	Added SCBus Clock Control Bits	hl
2.3	25.6.2008	Added SC_SREF_8K as reference input Removed obsolete note on usage of sec PLL input	hl
2.4	19.03.2009	Fixed documentation of FPGA type/version register	Te
	4.09.2013	Adaption to new layout, typo correction Added chapter 7.2 and 7.3	Se
	24.10.2013	Added location diagram and connector overview, Added chapter "Front Panel and LEDs" Updated connector information	Se
	28.04.2014	Update Chapter 7.3 "Statement on Environmental Protection"	se