NPMC-860-2E1/T1
Telecom PMC Module
Technical Reference Manual V1.9
HW Revision 2.0, 2.1, 2.2

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
b	bit
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 1000000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
MPC860	Embedded processor from Motorola
PowerQUICC	MPC860
QSpan II	Tundra PCI-Bus Controller
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SRAM	Static RAM
T1	1,544 Mbit G.703 Interface
ML53812	SCSA controller
SCbus	Time-Slot Interchange Bus of the SCSA
SCC	Serial Communication Controller of the MPC860
SCSA	Signal Computing System Architecture

1 Introduction

1.1 General Information

The **NPMC-860-2E1/T1** module is a high performance telecommunication controller with two E1 / T1 Line interfaces and a SCbus interface. It is implemented as a standard PCI Mezzanine Card Type 1. The **NPMC-860-2E1/T1** module is based on Motorola's PowerQUICC MPC860 which combines an internal RISC I/O processor and a PowerPC™ CPU. The MPC860's internal RISC processor can handle up to 64 HDLC channels, thus an application running on the **NPMC-860-2E1/T1**'s PowerPC™ kernel can support up to 64 simultaneous HDLC connections.

General features:

- Two E1 or T1 line interfaces
- SCbus Interface on PMC P14 connector
- Onboard high performance PowerPC CPU MPC860
- Multiplexer cross connect between internal TDM busses, SCbus and the Time-slot Assigner of the MPC860
- Single-slot VME or Compact PCI solution together with VMEbus or cPCI PMC carrier board
- PCI 2.2 standard compliant bus interface

Features of the Line Interface Circuits:

- Support of T1 and E1 lines by assembly option
- Clock recovery and jitter attenuation
- Line and path performance monitoring
- Extraction/insertion of the ISDN D-channel by HDLC / LAPD interface

E1 Option:

- HDB3 and AMI line code
- CRC-4 multiframe signaling support
- Data extraction/insertion on TS16 for HDLC / LAPD interface
- Indicators for loss of signal, loss of frame alignment, loss of multiframe alignment

T1 Option:

- B8ZS and AMI line code
- Support for frame formats SF, ESF, T1DM(DDS), SLC96
- Loss of signal detection, red, yellow, AIS alarm detection

Features of the Universal Timeslot Interchange (ML53812) circuit:

- Flexible routing of any time slot between the 2 framers, the SCbus backplane and the Timeslot Assigner Interface of the CPU
- Generation of SCbus Clock master signals
- Support of 2/4/8 MHz bus clock
- Master clock selection between any of the four line interfaces or the SCbus backplane,
- optional free running mode.

Features of the PCI Interface:

- PCI V2.2 Standard compliant
- 32 Bit, 33MHz PCI Master/Slave interface
- DMA Capability
- PCI interrupt support
- Programmable address window may map any portion of the local DRAM/SRAM into the PCI memory space

Options:

- Onboard protocol firmware for ISDN and V5.x
- Can handle SS7 and D-SS1 software on-board.
- Standard APIs are available

Table 2: NPMC-860-2E1/T1 Technical Data

PMC-Module	Standard PCI Mezzanine Card Type 1
Processor	PowerQUICC™ MPC860 based Embedded PowerPC™ Architecture 33/40/50/66/80/100 MHz
PCI to QBUS bridge	QSpan II, 32 bit, 40/50MHz
Main Memory	16 Mbytes 32 bit wide EDO DRAM
Fast SRAM	(opt.) 1 MB fast 32 bit wide SRAM
FlashPROM	2/4 Mbytes 8 Bit boot FlashPROM, on-board programmable
SCbus	ML53812 Universal Timeslot Interchange for SCbus, PMC-I/O connector
E1 / T1 – Line	E1 / T1 interfaces with the PM6341 (E1) or PM4341 (T1), front-panel connectors
Serial I/O	RS-232 compatible
Power consumption	3.3V 0.8A (=2.65 VA) 5.0V 0.5A (=2.5 VA)
Environment: Temperature (operating) Temperature (storage) Humidity	 0°C to +50°C -40°C to +85°C 5% to 95% noncondensing
Standards compliance	PCI Rev. 2.2 IEEE P1386.1 / Draft 2.4

1.2 The NPMC-860-2E1/T1 Nomenclature

Table 3: NPMC-860-2E1/T1 Nomenclature

NPMC-860-2E1/T1-SS-SP-OHM-SCSA

Abbreviation	Description	Option
SS	type of line interface	T1 or E1
SP	processor speed	33, 40, 50,66 or 80 MHz
OHM	line impedance	100 Ohm for T1 120 or 75 Ohm for E1
SCSA	SCSA / H.110 bus interface	0: no SCSA-Bus interface 1: SCSA-Bus interface

2 Hardware Installation

2.1 A Safety Note

Electrostatic discharge and incorrect board installation and removal can damage the circuitry or shorten its life.
To ensure proper operation of the **NPMC-860-2E1/T1** during its usual lifetime take the following precautions before handling the board.

- Before installing or deinstalling the board, please read this installation section
- Before installing or deinstalling the **NPMC-860-2E1/T1**, read the Installation Guide and the User's Manual for the PMC carrier board
- Before touching integrated circuits, take all the necessary precautions for handling electrostatic devices.
- Ensure that the NPMC-860-2E1/T1 is connected to the carrier board with all three PMC connectors properly seated and that the power is available (**GND, +5V, and +3.3V**).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is screwed to the front panel or VME/cPCI rack and
  - shielded by a closed housing.

2.2 Prerequisites for Installation

Before powering up, ensure that you have the following prerequisites:

- a VME bus system with a P2 connector for the SCSA bus if SCSA operation is desired, or
- a cPCI bus system with a J4 connector for the H.110 bus if H.110 operation is desired
- a power supply that meets the following specifications
  +3.3V / 0.8 A typical
  +5.0V / 0.5 A typical

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that whereever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly intergrated into larger and more complex envionments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

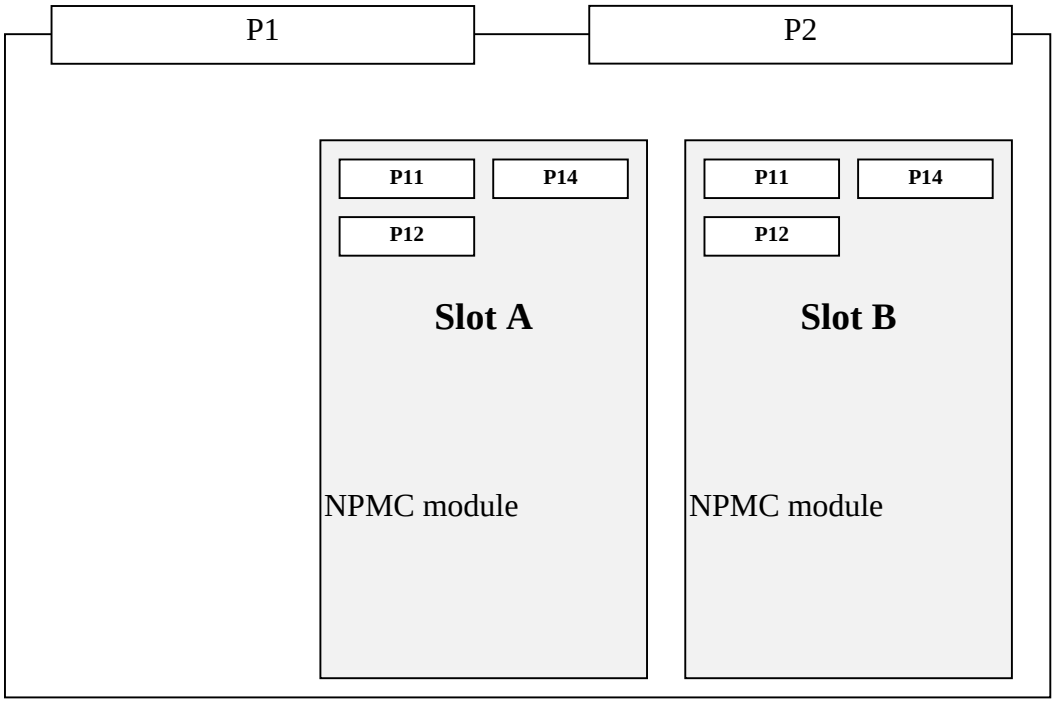
2.3.4 Product Safety

The board complies to EN60950 and UL1950.

2.4 NPMC-860-2E1/T1 used on VMEbus or Compact PCI Carriers

A standard VMEbus or Compact PCI carrier board may carry up to two PMC modules. Special care must be taken regarding the interconnection of the SCbus Signals between the modules and the SCbus backplane for not violating the SCbus specification by the routing of traces on the carrier board.

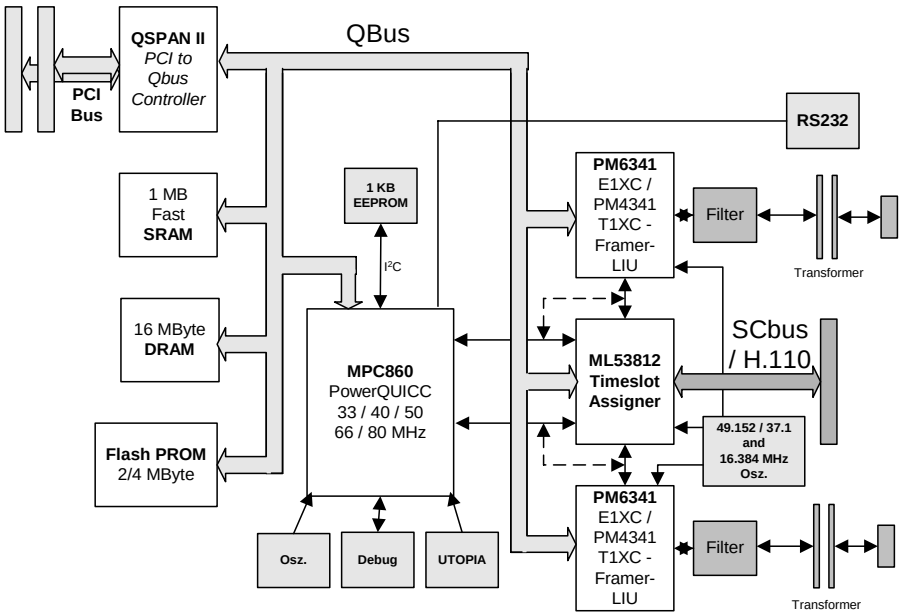
Figure 1: NPMC-860-2E1/T1 on a VMEbus carrier



3 Hardware Overview

The main building blocks of the **NPMC-860-2E1/T1** are the MPC860 PowerQuicc CPU, two framer devices and the universal timeslot interchange unit. The two E1/T1 framers interface directly to the front panel RJ45 connectors. From the backplane interface of the framers the timeslots can either be routed to the PowerQuicc CPU or to the SCbus backplane by the ML53812 device.

Figure 2: NPMC-860-2E1/T1 module block diagram

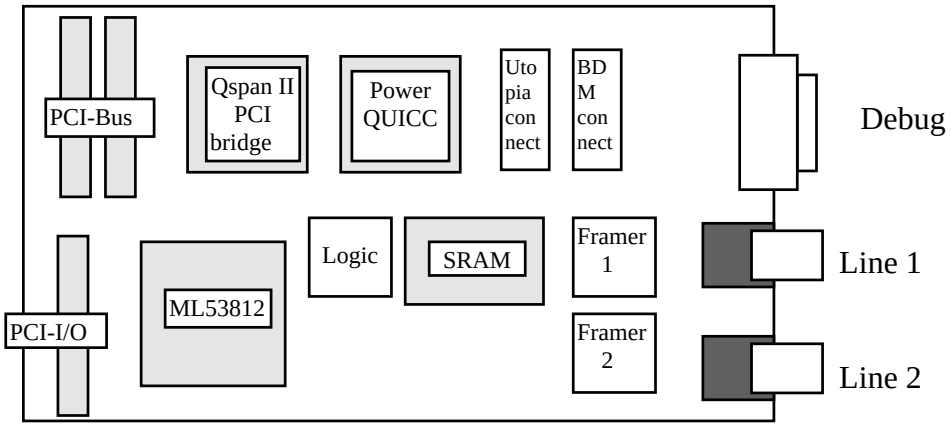


3.1 Location Overview

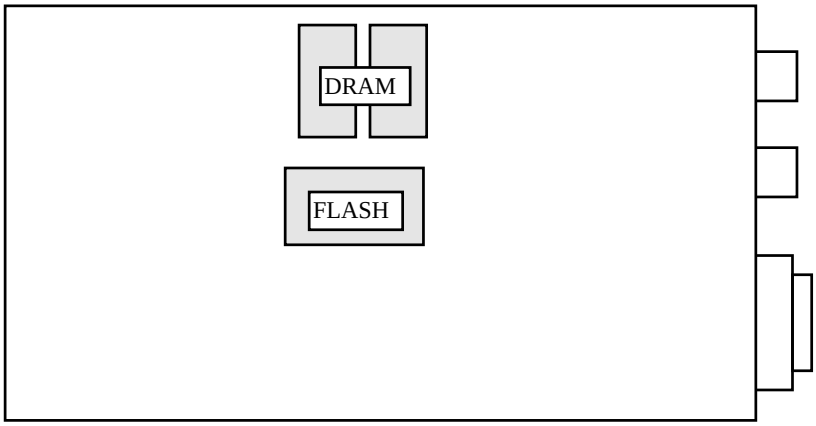
Figure 3 shows the position of the important **NPMC-860-2E1/T1** components. Depending on the board type and configuration, the assembled components may vary.

Figure 3: Location diagram of the **NPMC-860-2E1/T1** module (schematic)

Top view



Bottom view



3.2 The E1 /T1 Framers

The design of the **NPMC-860-2E1/T1** incorporates two E1 or T1 interfaces. For controlling the line interface an integrated Framer / Line Interface Unit (LIU) from PMC Sierra has been chosen. The framer is available as an E1 or T1 version. One side of the framers directly connect to the magnetics / analogue components of the line interface. The other side connects by its backplane interface to the ML53812 time slot interchange unit (ML53812). The backplane interface builds a 2048MHz TDM bus with 32 timeslots, each of 8 bits wide. The backplane interface runs synchronously to the clock / frame sync signals fed back by the ML53812 device.
For detailed information about the E1/T1 framer, please refer to the manufacturers manuals PM6341 (for E1) and PM4341A (for T1) (contact: see Chapter 9).
From N.A.T. drivers for the PM6341 and PM4341A are available. For more detailed information, please contact N.A.T..

3.3 The ML53812 Universal Timeslot Interchange Unit

The ML53812 timeslot interchange unit has got two main purposes:

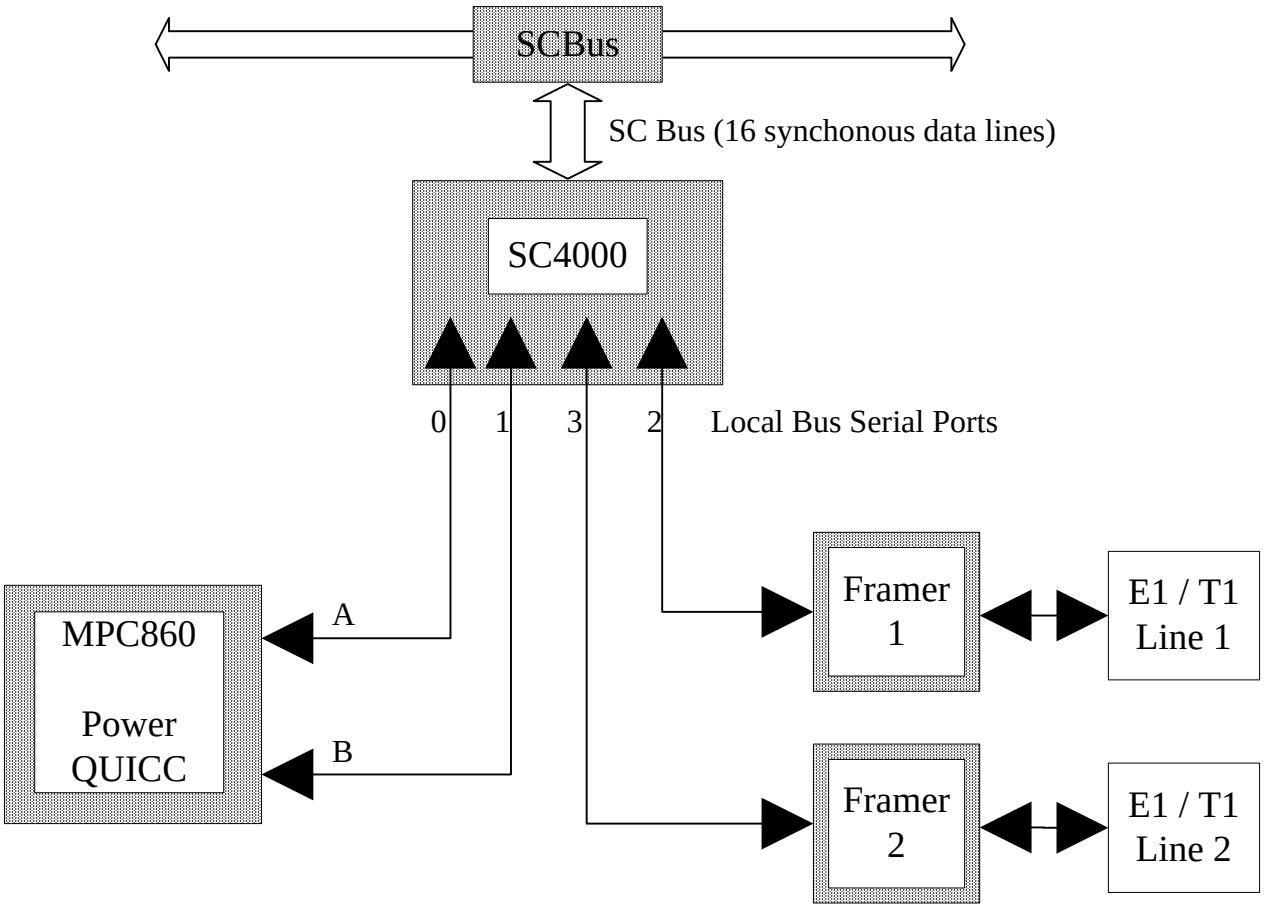
1.) Routing of timeslots between the frames the SCbus backplane and local CPU
2.) Determination of the clock master and supplying the master clock to all onboard devices.

The local interfaces of the ML53812 are directly connected to the backplane interface of the framer chips. The local clock input signals are connected to the framers RFP signal. The RFP signal is the recovered line clock signal, thus running synchronously to the clock supplied by the public network. By programming the corresponding registers, one of the local framer clocks or the backplane clock can be chosen as the master clock. The master clock is than fed back to all framers for use as the transmit and backplane clock.
For the use and functions of the ML53812 please refer to the manufacturers manual of the ML53812 device (see Chapter 9).
From N.A.T. drivers for the ML53812 are available. For more detailed information, please contact N.A.T..

3.4 The Telecom Data Path

The telecom data path connects the onboard line interface circuits / framers, the SCbus controller and the local MPC860 CPU. Figure 4 shows the principal interconnection of the these units.

Figure 4: The Telecom Data Path

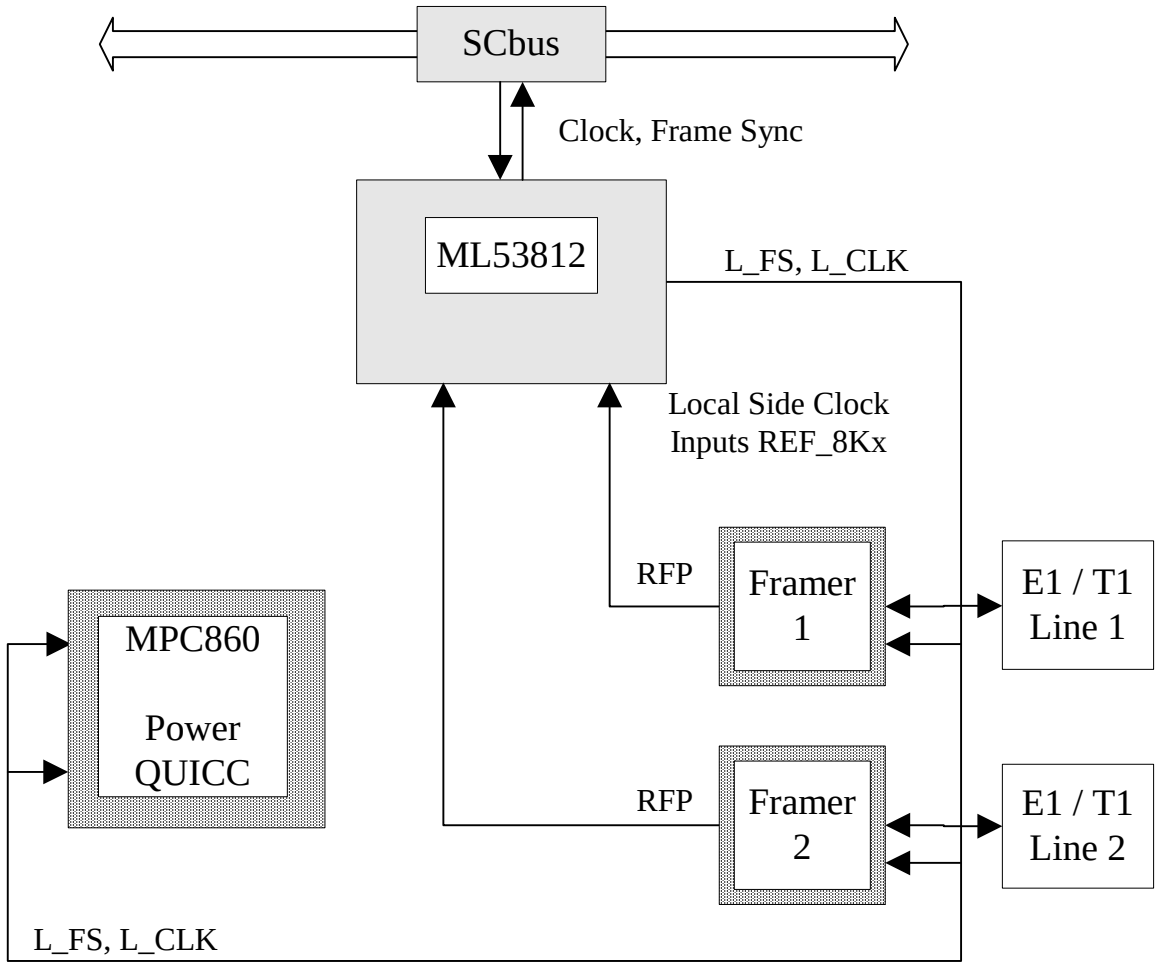


The PowerQUICC has two time-division multiplexed channels with 32 timeslots each (full-duplex). Every E1 framer delivers 32 Timeslots (full-duplex) on ist backplane interface. The ML53812 has 8 local times-slot channels (each with 32 timeslots), 4 of which are used by the 2 framers and by the CPU, and an SCbus interface with 512 timeslots on 16 data lines (at 2.048 MHz).
Every local channel can be routed from the MPC860 PowerQUICC or one of the framers to timeslots on the SCbus or vice versa. It is also possible to route timeslots between the two framers or a framer and the PowerQUICC.

Within such a construct there may be only one clock master. By means of the ML53812 the clock master for the internal devices can be choosen to be either framers 1 or 2, or the SCbus master clock. The ML53812 is also capable of generating the SCbus master clock. The internal master clock is fed back to the framer devices to drive the transmitter section of each framer.

Figure 5 shows the clock distribution network.

Figure 5: Clock distribution network



3.5 DRAM

The access to the DRAM of the NPMC-860-2E1/T1 is controlled by the memory controller of the MPC860 CPU. For details on accessing the DRAM, please refer to the PowerQUICC MPC860 User's Manual , Chapter 16: *Programmable Memory Controller*.
The **NPMC-860-2E1/T1** provides an on-board DRAM (EDO-DRAM). This memory is accessible from the PowerQUICC or the QSpan PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the DRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.
The user can define different timing patterns for the control signals that control the memory device. These patterns define how the external control signals behave in a read-access request, write-access request, burst read-access request, or burst write-access request. The user defines how the external control signals toggle when the periodic timers reach the maximum programmed value for refresh operation.
The memory capacity is 16 Mbytes. The memory is 32 bit wide. The access time of the EDO DRAM is 50nsec for new accesses. The access time within a row is 20nsec (bursting)
Depending on the operating frequency of the MPC860, the user must define different timing patterns. The User Programmable Machine A (UPM A) controls the PowerQUICC and the PCI accesses to the DRAM memory.
In the PowerQUICC RESET-state, access to the DRAM will be inhibited. Parity generation and checking is not supported by the module.

3.6 SRAM

To access the SRAM on the NPMC-860-2E1/T1 the memory controller of the MPC860 is used as well. For details on accessing the SRAM, please refer to the PowerQUICC MPC860 User's Manual , Ch 16: *Programmable Memory Controller*.
The **NPMC-860-2E1/T1** provides optionally an on-board high-speed SRAM. This memory is accessible from the PowerQUICC or the QSpan PCI-bridge chip. The memory controller of the PowerQUICC controls the SRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements
The memory capacity is 1 Mbyte. The memory is 32 bit wide. The access time of the SRAM is 3 clock cycles (60 nsec with a 50 MHz CPU) for every type of access. There is no restriction in accessing the SRAM.
Please note if the processor runs at 50 MHz or more and the application uses 64 B-channels with HDLC protocol, the PowerQUICC must use this SRAM for the HDLC- buffer descriptors.

3.7 Boot Flash

To access the FlashPROM on the NPMC-860-2E1/T1 use the memory controller of the MPC860. For more details please refer to the MPC860 Manual.
The flash memory area is located directly on the PowerQUICC bus, therefore the reset-vector table (in the boot flash) is visible to the CPU after a power-on reset. The boot flash memory has a maximum size of 4 Mbytes and can be directly accessed by the CPU. The FlashPROM memory is organized 8-bit wide. The FlashPROM is a 5V only device. No extra programming voltage is necessary to program the FlashPROM.
The FlashPROM can be programmed in one of two ways:

- Programming the entire flash memory from the PCI-bus. Note: the NPMC-860-2E1/T1 module must be in the RESET-State (refer to 7.2.1.1).
- Programming the flash memory in the RUN-state of the PowerQUICC.

If you wish to down-load software into the FlashPROM of the NPMC-860-2E1/T1 module, please ask N.A.T. for support. An software-download example utility is available for vxWorks.

3.8 Automatic Power Up

The NPMC-860-2E1/T1 module is equipped with a voltage sensor / reset circuit to provide a reliable power up and restart behavior. In any of the following cases, the NPMC-860-2E1/T1 module will be automatically reset and then continue with a normal power-up. If the NPMC-860-2E1/T1 module is in the RESET-state, both green LEDs on the front-panel will blink.

The voltage sensor generates a reset signal when:

- +5V drops below 4.4V *
- +5V goes above 5.6V *
- +3.3V drops below 2.65V *
- +3.3V goes above 3.6V *
- The carrier board signals a PCI Reset

3.9 PowerQUICC Port Pins Usage

Table 4: PowerQUICC Port Pin Usage (Port A)

Signal Function	PowerQUICC Port A Pin	Description
RxD SCC1	PA15	SCC1 Channel Receive
TxD SCC1	PA14	SCC1 Channel Transmit
MC TxD	PA13	Message Channel Transmit
MC RxD	PA12	Message Channel Receive
TDM_B TxD	PA11	TDM B Channel Transmit
TDM_B RxD	PA10	TDM B Channel Receive
TDM_A TxD	PA9	TDM A Channel Transmit
TDM_A RxD	PA8	TDM A Channel Receive
L_CLK	PA7	local TDM bus clock
MC CLK	PA6	Message Channel clock
L_CLK	PA5	local TDM bus clock
not used	PA4	
not used	PA3	
L_CLK	PA2	local TDM bus clock
not used	PA1	
L_CLK	PA0	local TDM bus clock

Table 5: PowerQUICC Port Pin Usage (Port B)

Signal Function	PowerQUICC Port B Pin	Description
/SPISEL	PB31	SPI Select signal
SPI CLK	PB30	SPI bus clock
SPI RX	PB29	SPI bus Receive
SPI TX	PB28	SPI bus Transmit
SDA_PQ	PB27	I^2C data
SCL_PQ	PB26	I^2C clock
SMC1 TxD	PB25	SMC1 Channel Transmit
SMC1 RxD	PB24	SMC1 Channel Receive
not used	PB23	
/SDACK2	PB22	DMA Ack to QSpan II
not used	PB21	
not used	PB20	
RTS SCC1	PB19	SCC1 Channel RTS signal
not used	PB18	
not used	PB17	
not used	PB16	
TXCLAV	PB15	UTOPIA Interface
IMSEL*	PB14	Image Select for QSpan II

Table 6: PowerQUICC Port Pin Usage (Port C)

Signal Function	PowerQUICC Port C Pin	Description
RXCLAV	PC15	UTOPIA Interface
DREQ2	PC14	DMA REQ from QSpan II
UTO5	PC13	UTOPIA Interface
UTO4	PC12	UTOPIA Interface
CTS SCC1	PC11	SCC1 Channel CTS signal
UTO3	PC10	UTOPIA Interface
UTO2	PC9	UTOPIA Interface
UTO1	PC8	UTOPIA Interface
L_FS	PC7	local TDM bus frame sync
L_FS	PC6	local TDM bus frame sync
L_FS	PC5	local TDM bus frame sync
L_FS	PC4	local TDM bus frame sync

Table 7: PowerQUICC Port Pin Usage (Port D)

Signal Function	PowerQUICC Port D Pin	Description
UTPB0 / IMSEL *	PD15	UTOPIA Interface Image Select for QSpan II
UTPB1	PD14	UTOPIA Interface
UTPB2	PD13	UTOPIA Interface
UTPB3	PD12	UTOPIA Interface
RXENB	PD11	UTOPIA Interface
TXENB	PD10	UTOPIA Interface
UTPCLK	PD9	UTOPIA Interface
UTO6	PD8	UTOPIA Interface
UTPB4	PD7	UTOPIA Interface
UTPB5	PD6	UTOPIA Interface
UTPB6	PD5	UTOPIA Interface
UTPB7	PD4	UTOPIA Interface
SOC	PD3	UTOPIA Interface

All port signals are tristate after Power-Up, until programmed differently.

* The IMSEL signal selects one of two possible register images in the Qspan. This signal is connected to PB14, but can be connected to PD15 by a 0 Ohm resistor, if software compatibility with the previous hardware revision 0.3 is desired. As PD15 is used for the UTOPIA interface, this has to be taken into account when deciding which port to use to program IMSEL.
Default: resistor not assembled, PD15 connected to UTOPIA interface.

3.10 LEDs

The NPMC-860-2E1/T1 module is equipped with 6 LEDs which are completely software programmable. Thus there functionality depends very much of the application running on the module.
When using NAT's protocol stack for Primary Rate ISDN, the LED's have the following functions:

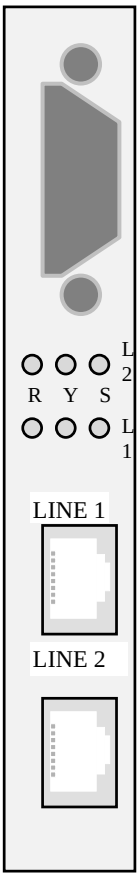


Figure 6: Front Panel and LEDs

LED S	the green LEDs for LINE 1 (L1) and LINE 2 (L2) indicate normal operation both LEDs blinking: reset is active
LED Y	the yellow LEDs for LINE 1 (L1) and LINE 2 (L2) indicate for example a YELLOW ALARM situation on one or both lines
LED R	the red LEDs for LINE 1 (L1) and LINE 2 (L2) indicate for example a RED ALARM situation on one or both lines (e.g. L1 down)

4 Memory Map

4.1 The NPMC-860-2E1/T1 memory map seen from the MPC860

All addresses are set by programming the corresponding Chip-Select (CS) decoder of the MPC860 CPU. Thus the addresses given in the following table can only be treated as an example. The final programming of the addresses associated to the MPC860 CS lines is completely application dependant. Within the I/O area (CS5) there is a subdecoding for the individual devices by hardware. The offset of these devices relatively to CS5 are fixed.

Table 8: NPMC-860-2E1/T1 memory map as seen from the MPC860

Device	Function	CS	Example Addr.	Offset to CS5	Description
Flash PROM	-	CS 0	0xff000000	- not appl. -	2/4 MB, 8 bit wide
DRAM	-	CS 1	0x00000000	- not appl. -	4/16 MB EDO, 32 bit wide
SRAM	-	CS 2	0x01800000	- not appl. -	128/256/512 KB, 32 bit wide
PCI-Bus	PCI bus access	CS 3	0x10000000	- not appl. -	2 PCI images selectable by IMSEL signal (PB14)
QSpan II	Qbus access to QSpan II	CS 4	0x01400000	- not appl. -	Access to the local side of the QSpan II register image
PM6341 / PM4341A	Framer 1	CS 5	0x01000000	0x0000	E1 / T1 framer with LIU
	Framer 2	CS 5	0x01000000	0x0400	E1 / T1 framer with LIU
CPLD	Registers	CS5	0x01000000	0x0800 - 0x1FF	Status/ Control Registers
ML53812	Timeslot assigner	CS 7	0x01000000	- not appl. -	H.110 / SCbus controller

4.2 Register description

4.2.1 PCB Revision Register

There is an 8 bit wide PCB revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, which contains the revision code of the PCB. This code reads decimally-coded in 2 nibbles, i.e. the PCB version V1.0 reads 0x10. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x0800. This register is read-only!

4.2.2 Lattice Revision Register

There is an 8 bit wide Lattice CPLD revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, which contains the revision code of the Lattice CPLD. This code reads decimally-coded in 2 nibbles, i.e. the CPLD version V1.0 reads 0x10. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x0c00. This register is read-only!

4.2.3 SCbus-ID

There is an 8 bit wide Lattice CPLD revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, which contains the SCbus ID code.

Table 9: SCbus ID Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	SCBUS-ID 4	SCBUS-ID 3	SCBUS-ID 2	SCBUS-ID 1	SCBUS-ID 0

SCBUS_ID [4:0]

These bits reflect the SCbus ID when the **NPMC-860-2E1/T1** is placed in a slot of a PMC carrier. These bits directly show the status of the PMC I/O connector P14 (pin 59, 61, 62, 63, and 65). The PMC I/O is available on VMEbus P2 according to the VITA specification in case this is supported by the carrier board. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x1000. This register is read-only!

4.2.4 LED - Control Register

There is an 8 bit wide Lattice CPLD revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, by which the 6 front panel LEDs are programmed. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x1400. This register is read-write.

Table 10: LED Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.c.	n.c.	LED2 red	LED2 yellow	LED2 green	LED1 red	LED1 yellow	LED1 green

If a bit is set to zero, the corresponding LED is turned on.

4.2.5 Reset – I/O - Control Register

There is an 8 bit wide Lattice CPLD revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, by which all I/O devices can be reset by software. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x1800. This register is read-write.

Table 11: Reset – I/O Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESET I/O	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.

By setting bit 7 = 1 the Reset line to the I/O devices (Framers, TSI) is set active. When making use of this function keep in mind that the logic does not make any timing with this bit. Hence, keep it active for some milliseconds, then reset it again in order to remove the reset signal from the connected devices.

4.2.6 Clock / Sync Select - Control Register

There is an 8 bit wide Lattice CPLD revision register implemented in the CPLD onboard the **NPMC-860-2E1/T1**, by which the SYNC and CLOCK signals used for the local TDM bus as timing reference may be chosen. This register is only relevant if the TSI device is not assembled, therefore no timeslot assignment is available, and also the generation of the local clock / sync signals has to be done by logic. By means of these 4 bits the sync / clock outputs of one of the two framers are selectable to be local clock / sync source. The register is addressed by the Register Chip Select CS5 as described in Table 8: with address offset 0x1c00. This register is read-write.

Table 12: Clock/Sync Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.c.	n.c.	n.c.	n.c.	SYNCSEL2	SYNCSEL1	CLKSEL2	CLKSEL1

The following relationship between the setting of SYNCSELx and CLKSELx and the selected framer sync / clock for local sync / clock applies:

Table 13: Clock/Sync Control Register Coding

SYNCSEL2	SYNCSEL1	L_FS
0	0	BRFPO_F1
0	1	RFP_F1
1	0	BRFPO_F2
1	1	RFP_F2

CLKSEL2	CLKSEL1	L_CLK
0	0	TCLKO_F1
0	1	RCLKO_F1
1	0	TCLKO_F2
1	1	RCLKO_F2

F1 refers to framer 1 (line 1), F2 refers to framer 2 (line 2).

5 Interrupt Sources of the MPC860 CPU

The interrupt sources of the onboard I/O devices are connected to interrupt pins of the MPC860 CPU. The following table gives an overview of the routing of the different interrupt sources.

Table 14: The Interrupt Mapping

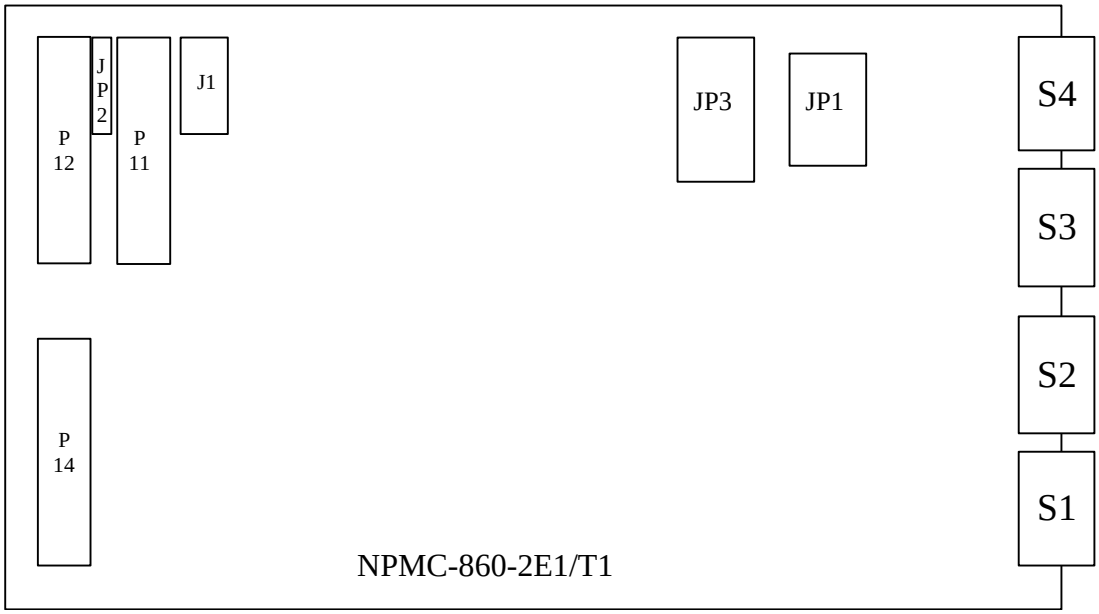
Interrupt Source	PowerQUICC Interrupt Level
QSpan II	IRQ-Level 0 (highest level)
Framer 1	IRQ-Level 1
Framer 2	IRQ-Level 2
Timeslot Assigner	IRQ-Level 3
n.c.	IRQ-Level 4
n.c.	IRQ-Level 5
n.c.	IRQ-Level 6
n.c.	IRQ-Level 7 (lower level)

IRQ pins 6 and 7 are used with their alternate functions FREEZE and RETRY, and hence are not available for IRQ routing. The same applies for the DP0-3 pins, which are used as such and not with their alternate IRQ functionality.

6 Connectors and Switches

6.1 Connector Overview

Figure 7: Connectors of the **NPMC-860-2E1/T1**



6.2 Switch Settings

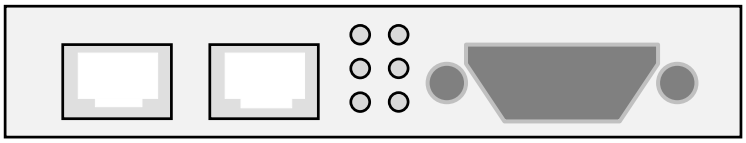
Jumper J1 is used for a Background Debug Mode Tool. This is a Power-Up option. If a BDM tool is to be used, J1 needs to be installed **before** powering up the module.

Default: J1 not installed

6.3 Connectors

6.3.1 E1/T1 Connectors

Figure 8: NPMC-860-2E1/T1 front-panel



LINE 2 LINE 1 DSUB

- LINE1: E1/T1 line interface 1
- LINE2: E1/T1 line interface 2

6.3.1.1 Pin Assignment - Line Connectors

Figure 9: The E1/T1 Connector (viewed from the front side)

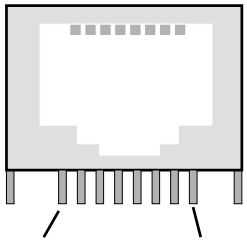


Table 15: Pin Assignment of the E1/T1 connectors (HW Rev. 2.1)

Pin	Signal
6	Tx+ Output
3	Tx- Output
5	Rx- Input
4	Rx+ Input

NOTE: The NPMC-860-2E1/T1 module's pin assignment does not match the usually used PRI pin assignment for RJ 45 in TE configuration.

Please refer to chapter 9 for description of a known bug concerning the pin assignment of HW Rev. 2.0 boards.

6.3.2 RS232 Port

The RS232 port is based on with the PowerQUICC serial communication controllers SCC1 or SMC1. As both port pins for SCC1 and SMC1 are connected, please keep in mind to tristate the port pins of the interface, which is not used.

Table 16: Pin Assignment of the Mini Sub D-9 connector

Pin	Signal
2	RxD
3	TxD
5	GND
7	/RTS
8	/CTS

NOTE: In case that the NPMC-860-2E1/T1 module is supplied with firmware the standard settings to get data from the port are :

- baudrate: 19200
- data bits: 8
- parity: none
- stop bits: 1

6.3.3 Connector JP2: Lattice Programming Port

Connector JP2 connects the JTAG- or programming-port of the Lattice CPLD device.

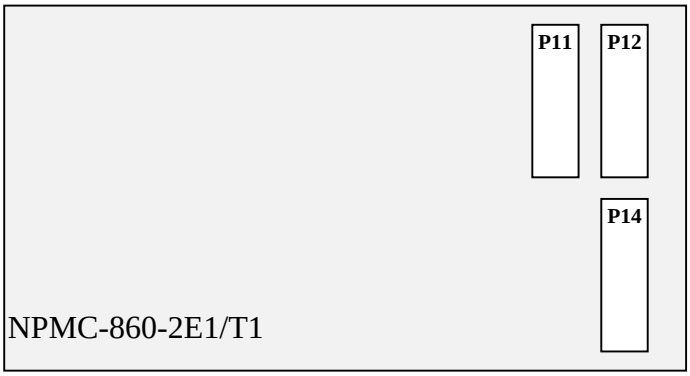
Table 17: Lattice Programming Port

Pin No.	**Signal**	**Signal**	**Pin No.**
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	/ENABLE	10

6.3.4 PMC Connectors

The following pages specify the pin assignment of the PMC connectors of the **NPMC-860-2E1/T1**. While P11 and P12 are specified in the PMC, resp. PCI specification, P14 is manufacturer specific and reserved for proprietary I/O signals. In the case of the **NPMC-860-2E1/T1** P14 supports the SC-Bus.

Figure 10: The PMC connectors on the **NPMC-860-2E1/T1**



Please refer to the following tables to look up the pin assignment of the P11, P12 and P14 of the NPMC-860-2E1/T1.

6.3.4.1 Pin Assignment of the PMC Connector -- P11

Table 18: Pin Assignment of the PMC Connector -- P11

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	TCK	-12V	2	n.c.
GND	3	GND	/INT A	4	/IRQ-QSpan
n.c.	5	/INT B	/INT C	6	n.c.
BUSMODE1	7	BUSMODE1	+5V	8	+5V
n.c.	9	/INT D	PCI_RSV1	10	n.c.
GND	11	GND	PCI_RSV2	12	n.c.
CLK	13	CLK	GND	14	n.c.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
V (I/O)	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
V (I/O)	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	n.c.
n.c.	41	/SDONE	/SB0	42	n.c.
PAR	43	PAR	GND	44	GND
V (I/O)	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
V (I/O)	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	n.c.

6.3.4.2 Pin Assignment of the PMC Connector -- P12

Table 19: Pin Assignment of the PMC Connector -- P12

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	+12V	/TRST	2	n.c.
n.c.	3	TMS	TDO	4	n.c.
n.c.	5	TDI	GND	6	GND
GND	7	GND	PCI_RSV3	8	n.c.
n.c.	9	PCI_RSV	PCI_RSV4	10	n.c.
n.c.	11	BUSMODE2	+3.3V	12	+3.3V
/RST	13	/RTS	BUSMODE 3	14	BUSMODE 3
+3.3V	15	+3.3V	BUSMODE 4	16	BUSMODE 4
n.c.	17	PCI_RSV	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESVD	34	n.c.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	n.c.
+3.3V	53	+3.3V	PCI_RESV	54	n.c.
n.c.	55	PCI_RESV	GND	56	GND
n.c.	57	PCI_RESV	PCI_RESV	58	n.c.
GND	59	GND	PCI_RESV	60	n.c.
n.c.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	n.c.

6.3.4.3 Pin Assignment of the PMC Connector -- P14 (PMC I/O)

Table 20: Pin Assignment of the PMC Connector -- P14

Ext. signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
MC	1	I/O	I/O	2	SD_15
SD_14	3	I/O	I/O	4	SD_13
SD_12	5	I/O	I/O	6	GND
SD_11	7	I/O	I/O	8	SD_10
SD_09	9	I/O	I/O	10	SD_8
SD_07	11	I/O	I/O	12	GND
SD_06	13	I/O	I/O	14	SD_5
SD_04	15	I/O	I/O	16	SD_3
SD_02	17	I/O	I/O	18	SD_1
GND	19	I/O	I/O	20	SD_0
CLKFAIL	21	I/O	I/O	22	FSYNCN
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	SCLKx2N
SL_4	27	I/O	I/O	28	/C16+
SL_2	29	I/O	I/O	30	SL_3
SL_0	31	I/O	I/O	32	SL_1
/SPISEL	33	I/O	I/O	34	SPIMISO
SPIMOSI	35	I/O	I/O	36	SPICLK
/C16-	37	I/O	I/O	38	CT_FRAME_B
CT_FRAME_A	39	I/O	I/O	40	CT_NETR2
CT_NETR1	41	I/O	I/O	42	/C4
C2	43	I/O	I/O	44	GND
CT_C8_B	45	I/O	I/O	46	CT_C8_A
CT_D16	47	I/O	I/O	48	CT_D17
CT_D18	49	I/O	I/O	50	CT_D19
GND	51	I/O	I/O	52	CT_D20
CT_D21	53	I/O	I/O	54	CT_D22
CT_D23	55	I/O	I/O	56	CT_D24
GND	57	I/O	I/O	58	CT_D25
CT_D26	59	I/O	I/O	60	CT_D27
CT_D28	61	I/O	I/O	62	CT_D29
CT_D30	63	I/O	I/O	64	CT_D31

The following table describes the P14 signals and their correspondence to the VITA SCSA and ECTF H.110 specifications. For more details please refer to the *ML53812-2 User´s Manual*, to VITA *Extensions to ANSI/VITA 6 - 1994 SCSA*, and to *CTCF H.110 Hardware Compatibility Specification: CT Bus*

Table 21: Description of P14 Signals

Signal	Description VITA Spec.	Description H.110 Spec.	General Description
MC	identical	identical	SCbus message channel
SD_15	identical	CT_D15	SCbus serial data stream 15
SD_14	identical	CT_D14	SCbus serial data stream 14
SD_13	identical	CT_D13	SCbus serial data stream 13
SD_12	identical	CT_D12	SCbus serial data stream 12
SD_11	identical	CT_D11	SCbus serial data stream 11
SD_10	identical	CT_D10	SCbus serial data stream 10
SD_9	identical	CT_D9	SCbus serial data stream 9
SD_8	identical	CT_D8	SCbus serial data stream 8
SD_7	identical	CT_D7	SCbus serial data stream 7
SD_6	identical	CT_D6	SCbus serial data stream 6
SD_5	identical	CT_D5	SCbus serial data stream 5
SD_4	identical	CT_D4	SCbus serial data stream 4
SD_3	identical	CT_D3	SCbus serial data stream 3
SD_2	identical	CT_D2	SCbus serial data stream 2
SD_1	identical	CT_D1	SCbus serial data stream 1
SD_0	identical	CT_D0	SCbus serial data stream 0
GND	identical	identical	Ground
CLKFAIL	identical	identical	SCbus System Clock Fail signal
SREF_8K	SREF8k	n.a.	SCbus 8 kHz Reference
SL_0	identical	n.a.	SCbus ID
SL_1	identical	n.a.	SCbus ID
SL_2	identical	n.a.	SCbus ID
SL_3	identical	n.a.	SCbus ID
SL_4	identical	n.a.	SCbus ID
SCLKx2N	/SCLKx2	/SCLKx2	This is a SCbus system clock x 2.
SCLK	identical	identical	This is a SCbus system clock.
FSYNCN	/FSYNC	/FSYNC	This is a SCbus 8 kHz frame signal
CT_D31 – CT_D16	n.a.	identical	CT Bus serial data stream 31 - 16
/CT_FRAME_A	n.a.	identical	This is a CT Bus 8 kHz frame signal
/CT_FRAME_B	n.a.	identical	This is a CT Bus 8 kHz frame signal
CT_NETREF1	n.a.	identical	CT Bus 8 kHz Reference
CT_NETREF2	n.a.	identical	CT Bus 8 kHz Reference
CT_C8A	n.a.	identical	CT Bus 8 MHz clock signal
CT_C8B	n.a.	identical	CT Bus 8 MHz clock signal
C16+	n.a.	n.a.	differential 16 MHz clock signal
C16-	n.a.	n.a.	differential 16 MHz clock signal
C2	n.a.	n.a.	2 MHz clock signal
/C4	n.a.	n.a.	4 MHz clock signal
/SPISEL	n.a.	n.a.	MPC860 SPI bus select line
SPICLK	n.a.	n.a.	MPC860 SPI bus clock line
SPIMISO	n.a.	n.a.	MPC860 SPI bus data out line
SPIMOSI	n.a.	n.a.	MPC860 SPI bus data in line

6.3.4.4 SCbus IDs

In a SCSA system each SCSA device needs to have a unique ID. The NPMC-860-2E1/T1 supports the setting of SC IDs by jumpers or switches on the VMEbus backplane.
The signals **SL_0** to **SL_4** refer to the NPMC-860-2E1/T1 placed on a VMEbus or cPCI carrier with SCSA bus extension.

6.3.4.5 SPI Bus

Additional to the SCbus / H.110 bus signals the SPI interface of the MPC860 has been routed to the P14 connector for user applications.

6.3.5 BDM / JTAG Interface

The PowerQUICC BDM/JTAG port is available on a 16 pin SMD micro connector (see Figure 3). The mode of operation of this interface is selected at power up. To select the JTAG mode, jumper J1 must not be closed (default) during power up. Otherwise the development port or BDM mode is enabled. Refer also to chapters 5.1 and 5.2.

Table 22: Development Port / BDM and IEEE 1149.1 Connector JP1 Pin-out Options

JTAG	BDM Port	PIN				
VFLS0	**VFLS0**	**1**		**2**	**/SRESET**	**/SRESET**
GND	**GND**	**3**		**4**	**DSCK**	**TCK**
GND	**GND**	**5**		**6**	**VFLS1**	**VFLS1**
/HRESET	**/HRESET**	**7**		**8**	**DSDI**	**TDI**
+5V	**+5V**	**9**		**10**	**DSDO**	**TDO**
/ABORT	**/ABORT**	**11**		**12**	**--------**	**TMS**
--------	**FRZ**	**13**		**14**	**+3.3V**	**+3.3V**
/JT/DBG	**/JT/DBG**	**15**		**16**	**GND**	**GND**

6.3.6 UTOPIA Connector

Table 23: The UTOPIA Connector JP3

Pin No.	Signal Name
1	GND
2	UTPCLK
3	GND
4	UTPB0
5	/TXENB
6	UTPB1
7	/RXENB
8	UTPB2
9	NC
10	UTPB3
11	NC
12	UTPB4
13	+5V
14	UTPB5
15	+3.3V
16	UTPB6
17	TXCLAV
18	UTPB7
19	RXCLAV
20	SOC
21	UTD_1
22	UTD_2
23	UTD_3
24	UTD_4
25	UTD_5
26	UTD_6

The utopia connector is only assembled if CPU option SAR was chosen.

7 Programmer's Reference

7.1 QSPAN II

7.1.1 Host Setup of the QSpan II PCI Bridge

In order to configure the **NPMC-860-2E1/T1** to work on the PCI-bus, the following steps must be taken:

1. Look up the address of the PCI-bus controller of the **NPMC-860-2E1/T1** in the ***Configuration Space*** of the PCI-bus of the carrier board (please refer to the manual for the carrier board).
The PCI-bus controller of the **NPMC-860-2E1/T1** occupies 256 Bytes in the ***Configuration Space*** and you should see the following address map (first 64 bytes according to PCI specification 2.2):

Table 24: NPMC-860-2E1/T1 memory map in the configuration space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address configuration space
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
...	...	...
0x003c	PCI_MISC1	miscellaneous 1

For more details regarding the QSpan registers of the **NPMC-860-2E1/T1**, please refer to the QSpan manual's register map (table A.1, Appp. A-2).

2. Now write - to the offset address 0x0010 (QSpan register PCI_BSM, 32 bit) - the start address of the **NPMC-860-2E1/T1** where it should appear in the ***memory space*** of the carrier board's PCI-bus. Please note, that all PCI register accesses have to be done in little endian format.
The register image of the QSpan should now be visible in the PCI memory space.

Table 25: NPMC-860-2E1/T1 memory map in the PCI memory space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address QSpan register
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	Class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
0x0014	-	QSpan unimplemented
...	...	...
0x003c	PCI_MISC1	miscellaneous 1
...	...	...
0x800	MISC_CTL	miscellaneous control
0x804	EEPROM_CS	EEPROM control
...	...	...
0x0ffc	-	QSpan reserved

3. Initialize the register PBTI0_CTL for target image 0 and set the necessary parameters:
The longword read/write access must be enabled by writing the PBTI0_CTL at offset 0x0100 (image enable, block size BS[3:0] = 0110 = 4 MB, or BS[3:0] = 1000 = 16 MB, Q-bus destination port size DSIZE[1:0] = 00 = 32 bit).

4. Set address translation decoding on register PBTI0_ADD at offset 0x0104 (host system dependent):
Write the start address where the memory of the NPMC-860-2E1/T1 module should appear in the ***Memory Space*** of the PCI bus.

5. Make certain that there are no address conflicts in your systems (set/check the amount of the memory occupied by the **NPMC-860-2E1/T1** in the PCI memory space).

7.1.2 Q-Bus Configuration

Through the MISC_CTL register parameters for configurating the local bus (Q-Bus) are set. The settings to be performed are system dependant. But, the following aspect has to be taken into account in any case:

Setting of bit 0 (SW-RST) will cause a RESET on the Q-Bus, if the Q-BUS HRESET signal is connected to the RESETO pin of the QSPAN (like for this module). The RESETO signal follows the programming of the SW-RST bit directly, i.e. without any delay in time. Therefore, if the MPC860 is to be reset by this means, the minimum time period necessary to perform an orderly hardware reset of the MPC860 has to be strictly obeyed. Otherwise the MPC860 may enter an undefined state. A time period of 100ms is recommended between the setting and resetting of this bit. In time-critical applications this period may be reduced. Any value longer than 1ms should be suuficient. 100ms is a period of time which is suitable and safe for resetting the Q-Bus in all cases and for all CPU operating frequencies.

7.1.3 EEPROM Configuration

By means of register EEPROM_CS the Configuration-EEPROM may be read and reprogrammed, which the QSPAN II uses for Power-Up – initialialisation. Please be aware of the fact that programming the EEPROM with unsuitable values may cause the PCI-Bus to hang completely.

NOTE: For more information, please refer to the QSpan II manual. Please make certain that you use the correct endian format when writing into the QSpan II registers.

7.2 Framer Initialisation

7.2.1 E1 120/75 Ω and T1 100 Ω Interface

N.A:T. recommends a certain initialisation for the framer DACs in the various waveform templates (E1/120Ω, E1/75Ω, T1/100Ω). As the default set up of the framers does not show the optimum pulse mask for this hardware combination (filters, transformers, EMC components), the following tables have been determined to show best results for pulse mask shapes for distances below 100 ft. Amend these as necessary for your applications.

E1 120 Ω Interface

- Set up framer register "XPLS Line Length Configuration" to be 0xe0.
- Write the following values to the XPLS internal CODE registers:

Table 26: Programming the Waveform Template for E1/120Ω

Address	Value
0x0	0x0d
0x1	0x0a
0x2	0x0a
0x3	0x0a
0x4	0x02
0x5	0x00
0x6	0x00
0x7	0x00

E1 75 Ω Interface

- Set up framer register "XPLS Line Length Configuration" to be 0xe0.
- Write the following values to the XPLS internal CODE registers:

Table 27: Programming the Waveform Template for E1/75Ω

Address	Value
0x0	0x0f
0x1	0x0b
0x2	0x0a
0x3	0x0a
0x4	0x04
0x5	0x00
0x6	0x00
0x7	0x00

T1 100 Ω Interface

- Set up framer register "XPLS Line Length Configuration" to be 0xd0.
- Write the following values to the XPLS internal CODE registers:

Table 28: Programming the Waveform Template for T1/100Ω

Address	Value
0x0	0x0e
0x1	0x0b
0x2	0x0b
0x3	0x0b
0x4	0x02
0x5	0x00
0x6	0x00
0x7	0x00

7.3 On-board Firmware

7.3.1 Boot Software

After a power-up or reset, the on-board firmware starts automatically with the basic memory and I/O tests. Each test that is successfully passed will be indicated by an LED on the front-panel of the NPMC-860-2E1/T1.

7.3.2 The Board Support Packages

If the NPMC-860-2E1/T1 is delivered with a vxWorks BSP, please refer to the vxWorks BSP Readme file for the implementation details of this BSP.

7.3.3 ISDN Software

If the NPMC-860-2E1/T1 is delivered with ISDN software, please refer to the ISDN software manual for detailed information on how to set-up the NPMC-860-2E1/T1 with the ISDN software (NFAPI Manual).

7.3.4 No on-board Operating System, nor Application Software

If the NPMC-860-2E1/T1 is delivered without operating system or protocol software, please take the following steps:

- Refer to the MPC860 manual for information on how to generate your boot code
- Configure the local memory map (see Figure 7), the interrupt registers of the MPC860, ...
- Load your boot code into the FlashPROM of the NPMC-860-2E1/T1 while the MPC860 is in RESET-mode, and start the code.

8 Introduction to Onboard Devices

8.1 PowerQUICC MPC860 CPU

For the use and functions of the PowerQUICC MPC860 CPU please refer to the MPC860 Manual.
The MPC860 PowerPC™ Quad Integrated Communications Controller (PowerQUICC) is a versatile one-chip integrated microprocessor and peripheral controller combination that can be used in a variety of applications. It particularly excels in both communications and networking systems.
The MPC860 is a PowerPC™-based derivative of Motorola's MC68360 (Quad Integrated Communications Controller(QUICC™). The MPC860 CPU is a 32-bit PowerPC™ implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) has been enhanced with the addition of the interprocessor-integrated-controller (I^2C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs). Overall systems functionality is completed with the addition of a PCMCIA socket controller supporting up to two sockets and a real time clock.

The following is a list of the MPC860´s important **processor features**:

- PowerPC™ single issue integer core
- Precise exception model
- Extensive system development support
- High performance (52 K Dhrystone 2.1 MIPS @ 50MHZ, 3.3V, 1.3W total power)
- MPC860 PowerPC™ system interface, including a periodic interrupt timer, a bus monitor, and real-time clocks
- Fully static design
- 32-bit address and data busses
- Flexible memory management
- 4-kbyte physical address, two-way, set-associative data cache
- 4-kbyte physical address, two-way, set-associative instruction cache
- Eight-bank memory controller
- System interface unit

The following is a list of the MPC860´s important **I/O features**:

- Communications processor module
- Ethernet / IEEE 802.3 CS/DMA
- HDLC2 / SDLC and HDLC bus
- AppleTalk
- Signaling system #7 (RAM microcode only)
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Binary synchronous (BiSync) communications
- Totally transparent
- Totally transparent with CRC
- Profibus (RAM microcode only)
- Asynchronous HDLC
- DDCMP
- V.14 (RAM microcode only)
- X.21 (RAM microcode only)
- V.32bis data-pump filters
- IrDA serial infrared
- Basic rate ISDN (BRI) in conjunction with SMC channels
- Primary rate ISDN (MH-Chip version only)
- Two-card PCMCIA 2.1 master interface

8.2 QSpan II™ Bus Bridge

For the use and functions of the QSpan II™ Bus Bridge please refer to the QSpan II Manual. For NPMC-860-2E1/T1 module V1.0 following QSpan II version is used:

QSpan II CA91C862 – 50CQ

The QSpan II™ chip is a member of Tundra Semiconductor Corporation's family of PCI-bus-bridging devices enabling board designers to bring PCI-based embedded products to market faster and more economically.
The QSpan II™ is designed to gluelessly bridge the QUICC™ (MC68360), the PowerQUICC™ as well as the MPC801 embedded controllers to PCI.
The QSpan II™ has the following features:

- A direct connect interface to the PCI-bus for Motorola's QUICC (MC68360), PowerQUICC(MPC860), M68040, the PMC821 and the MPC861 embedded controllers;
- 32-bit PCI interface compliant with PCI Revision 2.2;
- Decoupled transfer technology: three 16-entry deep FIFOs buffer multiple transactions in both directions, allowing zero wait state bursting on the PCI and Motorola buses;
- IDMA peripheral support for QUICC and PowerQUICC;
- Flexible address space mapping and translation between the PCI and Motorola buses;
- Programmable endian byte ordering;
- Two user-programmable slave images available for PCI access to the Motorola buses;
- QSpan™ control and status registers accessible from both PCI and Motorola buses;
- PCI-bus and Motorola buses can be operated at different clock frequencies;

8.3 ML53812-2 Universal Timeslot Interchange

The ML53812-2 is a complete CT Bus system interface and time slot interchange device that provides a cost-effective connection between a computer board's telephony interfaces or signal processing resources and the CT Bus. The ML53812-2 is an evolution of existing time-slot interchange ICs which offers seamless interoperability with SCbus devices.
A key element in computer telephony (CT) equipment is the auxiliary telecom bus. Most manufacturers of high-capacity CT equipment have used one or more types of telecom buses to transport and switch low-latency communications traffic between boards within the computer, bypassing the computer's main I/O and memory buses. To simplify the integration of devices that incorporate a telecom bus, the Enterprise Computer Telephony Forum (ECTF) developed a standard bus (H.100/H.110 CT Bus™) that provides compatibility modes with the most prevalent telecom buses today (SCbus™ and MVIP-90™), as well as the capacity and feature set needed to support the next generation of high capacity CT servers.
The new CT Bus is embraced by Dialogic under the Signal Computing System Architecture™ (SCSA™) umbrella of open standards for building interoperable CT systems.
The ML53812-2 runs in both 4 MHz and 8 MHz SCbus modes and supports the switching features needed to integrate CT Bus devices with 4 MHz SCbus, 8 MHz SCbus, and 2 MHz MVIP-90 devices. Because the H.100/H.110 CT Bus uses an identical switching model and clock speeds to that used for the SCbus, developers have unparalleled flexibility in integrating these two types of devices, or in transitioning from one type to the other.
The ML53812-2 takes full advantage of the mandatory and optional features defined in the ECTF H.100 and H.110 interoperability specifications. It is a non-blocking 512 x 4096 time slot switch, interfacing up to 512 ports on its parent device to any of the 4096 time slots on the new CT Bus.

FEATURES

- High functionality, low cost implementation of the ECTF H.100/H.110 interoperability specifications.
- Up to 512 programmable connections (256 transmit and 256 receive) to any of the 4096 time slots on the H.100/H.110 CT Bus.
- 8-channel stream-to-stream switching for data stream connections at variable rates.
- Implementation of all compatibility signals for complete interoperability with existing 4 MHz SCbus™, 8 MHz SCbus, 2 MHz MVIP-90™ devices, and H-MVIP™.
- Provides reliable clock synchronization for network-grade connection to digital network interfaces.
- Supports all H.100/H.110 CT Bus clock fallback features.
- Choice of constant or minimum switching delay on a per time slot basis.
- Supports CT Bus optional message channel interface, for both H.100 (PCI) and H.110 (cPCI) applications.
- Supports a variety of framing formats via a configurable local bus.
- Efficient microprocessor interface access to Local and CT Bus data streams through direct parallel access to/from transmit and receive switch.

Drivers for the ML53812 are available from N.A.T..

8.4 E1 /T1 Framer

For detailed informations about the E1/T1 framer, please refer to the PM6341 Manual (for E1) and PM4341 Manual (for T1). From N.A.T. drivers for the PM6341 and PM4341 are available.

8.4.1 Introduction to the E1 Framer

The PM6341 E1 Framer/Transceiver (E1XC) is a feature-rich device suitable for use in a variety of E1 Systems (such as CSU, DSU, CH BANK, MUX, DPBX, DACS, and ESDX) with a minimum of external circuitry. The E1XC is software configurable, thus features can be selected without wiring changes.
On the receiver side, the E1XC recovers clock and data. It can be configured to frame to a basic G.704 2048 Kbits/s signal, to the signaling multiframe alignment signal, or the CRC multiframe alignment signal. Using only an external transformer and passive components, the built-in analog circuitry supports direct reception of a G.703 2048kbit/s signal with a loss of not more than 6dB.
The E1XC also supports detection of various alarm conditions such as loss of signal, loss of frame, loss of signaling multiframe, loss of CRC multiframe, and reception of a remote alarm signal, remote multiframe alarm signal, alarm indication signal, and times-slot 16 alarm indication signal. The E1XC detects and indicates the presence of remote alarm and AIS patterns and also integrates RED and AIS Alarms as per industry specifications.
Support is provided for performance monitoring with accumulation of CRC-4 errors, far-end block errors, framing bit errors, and line code violations. The E1XC also detects and terminates HDLC messages on a data link. The data link may be extracted from times-slot 16 and used for common channel signaling or may be extracted from the national bits.
An elastic store for slip buffering and adaptation to backplane timing is provided, as is a channel associated signal extractor that supports signaling debounce, signaling freezing, idle code substitution, and data inversion on a per-times-slot basis. Receive side data and signaling trunk conditioning is also provided.
On the transmitter side, The E1XC generates framing for a basic G.704 2048kbit/s signal, or framing can be optional disabled. The signaling multiframe alignment signal may be optionally inserted. Further, the CRC multiframe structure may be optionally inserted.
Internal analog circuitry allows direct transmission of a G.703 2048 Kbits/s signal into either a 75 Ohm or 120 Ohm line using only an external transformer.
Support is also provided for channel associated signaling insertion, idle code substitution, digital milliwatt tone substitution and data inversion on a per times-slot basis. The chip also supports transmit side data and signaling trunk conditioning.
HDLC messages on a data link can be transmitted. The data link may be inserted into times-slot 16 and used for common channel signaling or may be inserted into the national bits. The E1XC can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter attenuation, the full or empty status of this FIFO is made available to facilitate higher-order multiplexing applications by controlling bit-stuffing logic.
It integrates a full-featured E1 transceiver in a single device with analog circuitry for receiving and transmitting G.703 2048 Kbits/s compatible signals and digital circuitry for terminating the digital duplex signal.

The receiver section

- Provides analog circuitry for receiving a G.703 2048 Kbits/s signal with up to 6dB of cable attenuation. Direct digital inputs are also provided to allow bypassing the analog front-end.
- Recovers clock and data using a digital phase-locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be bypassed
- Accepts dual-rail or single-rail digital PCM inputs
- Supports HDB3 or AMI line code
- Accepts gapped data streams to support higher rate demultiplexing
- Frames to a G.704 2048kbit/s signal within 1ms.
- Frames to the signaling multiframe alignment when enabled
- Frames to the CRC multiframe alignment when enabled
- Provides loss of signal detection, and indicates loss of frame alignment (OOF), loss of signaling multiframe alignment and loss of CRC multiframe alignment.
- Supports line and path performance monitoring according to ITU-T recommendations.
- Indicates the reception of remote alarm and remote multiframe alarm
- Indicates the reception of alarm indication signal (AIS) and times-slot 16 AIS
- Declares RED and AIS alarms using Q.516 recommended integration periods
- Provides an HDLC/LAPD interface for terminating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface
- Optionally extracts the data link from times-slot 16 (64kbit/s), which may be used to receive common channel signaling, or from any combination of the national bits in times-slot 0 of non-frame alignment signal frames (4kbit/s-20kbit/s)
- Provides a two frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction
- Provides channel associated signaling extraction, with optional data inversion, programmable idle code substitution, an up to 3 multiframes of signaling debounce on a per-times-slot basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning an all timeslots or on selected timeslots
- Optionally provides dual-rail digital PCM output signals to allow BPV transparency
- Supports transfers of received PCM and signaling data to 2048kbit/s backplane buses

The transmitter section:

- Supports transfer of transmitted PCM and signaling data from 2048 Kbits/s backplane buses
- Formats data to create a G.704 2048kbit/s signal. Optionally inserts signaling multiframe alignment signal. Optionally inserts CRC multiframe structure including optional transmission of far end block errors
- Optionally accepts dual-rail digital PCM inputs to allow BPV transparency. Also supports unframed mode.
- Provides channel associated signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per times-slot basis
- Provides trunk conditioning, which forces programmable trouble code substitution and signaling conditioning on all timeslots or on selected timeslots.
- Supports transmission of the alarm indication signal (AIS), times-slot 16 AIS, remote alarm signal or remote multiframe alarm signal
- Provides an HDLC/LAPD interface for generating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface
- Optionally inserts the data link into times-slot 16 (64kbit/s), which may be used to transmit common channel signaling, or into any combination of the national bits in times-slot 0 of non-frame alignment signal frames (4kbit/s-20kbit/s)
- Provides a digital phase-locked loop for generation of a low jitter transmit clock
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows bit-stuffing in higher rate multiplexing applications
- Supports HDB3 or AMI line code
- Provides analog circuitry for transmitting a G.703 compatible 2048 Kbits/s signal on a 75 OHM coaxial line or a 120 OHM symmetrical line. Digitally programmable line build out is provided
- Provides dual or single-rail digital PCM output signals

8.4.2 Introduction to the T1 Framer

The PM4341A single T1 Framer/Transceiver (T1XC) is a feature-rich device suitable for use in a variety of T1 Systems with a minimum of external circuitry. The T1XC is software configurable, allowing feature selection without changes to external wiring.
On the receiver side, the T1XC recovers clock and data and can be configured to frame to any of the common DS-1 signal formats: SF, ESF, T1DM(DDS). or SLC96. Analog circuitry is provided to allow direct reception of a DSX-1 compatible signal with up to 655 feet from the cross-connect by using only an external transformer and passive components.
The T1XC also supports detection of various alarm conditions such as loss of signal, loss of frame, pulse density violation, RED alarm, YELLOW alarm, and AIS alarm.
The T1XC detects and indicates the presence of YELLOW and AIS patterns and also integrates YELLOW, RED, and AIS alarms as per industry specifications.
Performance monitoring with accumulation of CRC-6 error, loss of frame events, framing bit errors, and line code violation is provided. The T1XC also detects the presence of in-band loopback codes, ESF bit-oriented codes, detects and terminates HDLC messages on the ESF data link.
An elastic store for slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-times-slot basis. Receive side data and signaling trunk conditioning is also provided.
On the transmitter side, the T1XC generates framing for SF, ESF, T1DM(DDS), and SLC96 DS1 formats, or framing can be optional disabled.
Internal analog circuitry allows direct transmission of a DSX-1 compatible signal using only an external transformer. Digitally programmable line build out allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect. The T1XC also supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per channel basis. The zero code suppression is selectable to Bell (bit7), GTE, or DDS standards, and can also be disabled. Transmit side-data and signaling trunk conditioning is provided.
The T1XC can also generate in-band loopback codes, ESF bit-oriented codes, and transmit HDLC messages on the ESF data link.
The T1XC generates a low jitter transmit clock and also provides a FIFO for attenuation of transmit jitter. When not used for jitter attenuation, the full or empty status of this FIFO is made available to facilitate higher-order multiplexing applications by controlling bit-stuffing logic.
Following features are supported by the T1XC:

The receiver section

- Provides analog circuitry for receiving a DSX-1 signal with up to 655 feet from the cross-connect. Direct digital inputs are also provided to enable by-passing the analog front-end.
- Recovers clock and data using a digital phase-locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be by-passed
- Accepts dual-rail or single-rail digital PCM inputs
- Supports B8ZS or AMI line code
- Accepts gapped data streams to support higher rate demultiplexing
- Frames to SF, ESF, T1DM(DDS) and SLC96 format DS1 signals.
- Provides loss of signal detection, and RED, YELLOW, and AIS alarm detection. RED, YELLOW, and AIS alarms are integrated as per industry specifications.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window
- Provides programmable in-band loopback code detection
- Supports line and path performance monitoring according to AT&T and ANSI specifications.
- Provides ESF bit-oriented code detection, and an HDLC/LAPD interface for terminating the ESF data link
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface
- Extracts the data link in ESF, T1DM(DDS) or SLC96 modes. Extracts the D-channel for Primary Rate interface.
- Provides a two frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction
- Provides robbed bit signaling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and 2 super-frames of signaling debounce on a per-channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Optionally provides dual-rail digital PCM output signals to allow BPV transparency. Also supports unframed mode.
- Supports transfers of received PCM and signaling data to 1.544 Mbit/s backplane buses or to 2048kbit/s backplane buses

The transmitter section:

- Supports transfer of transmitted PCM and signaling data from 1.544 Mbits/s or 2048 Kbits/s backplane buses.
- Formats data to SF, ESF, T1DM(DDS) and SLC96 format DS1 signals
- Optionally accepts dual-rail digital PCM inputs to allow BPV transparency. Also supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides channel associated signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides minimum ones-density through Bell (bit 7), GTE or DDS zero-code suppression on a per-channel basis.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window or optionally stuffs ones to maintain minimum ones-density.
- Allows insertion of framed or unframed in-band loopback code sequences.
- Allows insertion of a data link in ESF, T1DM(DDS), or SLC96 modes. Allows insertion of the D-channel for primary rate interfaces.
- Supports transmission of the alarm indication signal (AIS), or the YELLOW alarm signal in all formats.
- Provides ESF bit-oriented code generation and an HDLC/LAPD interface for generating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Provides a digital phase-locked loop for generation of a low jitter transmit clock
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications
- Supports B8ZS or AMI line code
- Provides analog circuitry for transmitting a DSX-1signal. Digitally programmable line build out is provided. Direct digital outputs are also provided.
- Provides dual or single-rail digital PCM output signals

9 Known Bugs

Please note that for boards with HW Rev. 2.0 the Receive/Transmit signals at the S1/S2 RJ45 connectors are swapped. This was corrected in HW Rev. 2.1.

Table 29: Pin Assignment of the E1/T1 connectors for HW Rev. 2.0

Pin	Signal
6	Rx+ Output
3	Rx- Output
5	Tx- Input
4	Tx+ Input

Appendix A: Reference Documentation

PCI Interface Chip

Company: TUNDRA
Title: QSPAN II (CA91CC862) PCI to Motorola Processor Bridge Manual

MPC860 PowerQUICC

Company: Motorola Inc.
Title: MPC860 PowerQUICC User's Manual

Timeslot Switching Interface Chip

Company: Oki
Title: ML53812-2 H.100/H.110 CT Bus System Interface and Time-Slot Interchange User's Manual

E1 Line Interface Chip

Company: PMC-Sierra Inc.
Title: PM6341 E1 Framer / Transceiver User's Manual

T1 Line Interface Chip

Company: PMC-Sierra Inc.
Title: PM4241A T1 Framer / Transceiver User's Manual

Appendix B: Document's History

Revision	Date	Description	Name
1.0	1997	initial revision	
1.1	01.06.1998	Portation of initial FrameMaker version to Wordfile	mz
	01.07.1999	Correcting information about REV-bit - "0" means Rev. 1.0 or higher (chapter 7.2.3.1.)	ga
	22.07.1999	Layout improvements	as
1.2	27.10.1999	General Update, adapted to HW Rev. 1.0	ga, as
	19.11.1999	Added PowerQUICC Frequency definitions in chapter 7.3.2.	mz
	20.11.1999	E1/T1 Framer Programming modified	ga
	06.12.1999	Layout corrections	as
1.3	22.02.2000 25.07.2000 28.12.2000	overworked entire manual, checked address values restructured corrected SCIDU bit values (chapter 7.2.1.)	cg hl ga
1.4	22.06.2001	QSPAN programming description extended	ga
1.5	10.08.2003	MPC860 Port Pin Usage added, figures 7 and 10 corrected	ga
1.6	05.09.2003	adapted to HW revision 2.0	ga
1.7	24.08.2005	adapted to HW revision 2.1	ga
1.8	10.02.2006	'Statement on Environmental Protection' added	ga
1.9	06.06.2007	adapted to HW revision 2.2, chapters 2.3.3. and 2.3.4. added	ga