

The NPMC-4E1/T1 has been designed by:

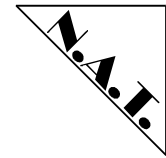
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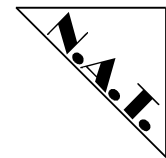
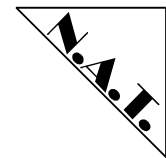


Table of Contents

LIST OF TABLES	1
LIST OF FIGURES	1
1 CONVENTIONS	2
1.1 ABBREVIATIONS:	2
2 INTRODUCTION	3
4.1 GENERAL INFORMATION	3
2.1 THE NPMC-4E1/T1 ORDER CODES	7
2.1.1 NPMC-4E1/T1 – Order Codes – Valid Combinations	8
2.2 SAFETY NOTE	10
3 HARDWARE OVERVIEW.....	11
3.1 LOCATION OVERVIEW.....	12
3.2 THE E1 /T1 FRAMERS.....	13
3.3 THE SC4000 UNIVERSAL TIMESLOT INTERCHANGE UNIT	13
3.4 THE TELECOM DATA PATH.....	14
3.5 THE PCI TO LOCAL BUS BRIDGE	16
3.6 INTERNAL INTERRUPT CHANNELS ON THE PCI-BUS	16
3.7 AUTOMATIC POWER UP	16
3.8 THE SWITCH SETTINGS	16
4 MEMORY MAP.....	17
4.1 PCI ADDRESS WINDOW	17
4.2 THE MEMORY MAP	17
4.3 REGISTER DESCRIPTION	18
4.3.1 <i>IRQ_Reg – Status of Interrupt Lines (address offset 0x500, read only)</i>	18
4.3.2 <i>SC-Bus-ID (address offset 0x600, read only)</i>	19
4.3.3 <i>LED-Control Register (address offset 0x700, read/write)</i>	20
5 FRONT PANEL ELEMENTS.....	21
5.1 THE E1/T1 CONNECTORS	21
5.1.1 <i>Pin Assignment - Line Connectors</i>	21
5.2 THE LEDS	22
6 CONNECTORS.....	23
6.1 THE PMC CONNECTORS.....	23
6.1.1 <i>Pin Assignment of the PMC Connector -- P11</i>	24
6.1.2 <i>Pin Assignment of the PMC Connector -- P12</i>	25
6.1.3 <i>Pin Assignment of the PMC Connector -- P14 (PMC I/O)</i>	26
6.1.4 <i>Description P14 Signals</i>	27
6.1.5 <i>SC-Bus IDs</i>	28
6.1.6 <i>NPMC-4E1/T1 P14 Specials</i>	28
6.2 THE JN5 CONNECTOR	28
7 HOW TO PROGRAM THE PCI BRIDGE	29
REFERENCE DOCUMENTATION.....	30
7.1 PCI INTERFACE CHIP	30
7.2 E1 OR T1 LINE INTERFACE	30
7.3 SCSA-BUS-INTERFACE.....	30
8 APPENDIX A -- DOCUMENT’S HISTORY.....	31

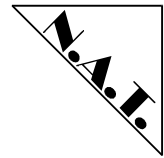


List of Tables

Table 1:	NPMC-4E1/T1 Technical Data.....	6
Table 2:	NPMC-4E1/T1 Order Codes.....	7
Table 3:	NPMC-4E1/T1 – Order Codes:.....	8
Table 4:	The Memory Map.....	17
Table 5:	Pin Assignment of the E1/T1 connectors.....	21
Table 6:	Pin Assignment of the PMC Connector -- P11.....	24
Table 7:	Pin Assignment of the PMC Connector -- P12.....	25
Table 8:	Pin Assignment of the PMC Connector -- P14.....	26
Table 9:	Description P14 Signals.....	27
Table 10:	Description JN5 Signals.....	28

List of Figures

Figure 1:	NPMC-4E1/T1 on a VMEbus carrier.....	5
Figure 2:	NPMC-4E1/T1 block diagram.....	11
Figure 3:	Location diagram of the NPMC-4E1/T1 (schematic).....	12
Figure 4:	The Telecom Data Path.....	14
Figure 5:	Clock distribution network.....	15
Figure 6:	DIP Switch SW1.....	16
Figure 7:	NPMC-4E1/T1 front-panel.....	21
Figure 8:	The E1/T1 Connector.....	21
Figure 9:	The LEDs.....	22
Figure 10:	The Connectors on the NPMC-4E1/T1.....	23

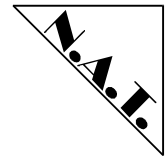


1 Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by a prefix *0x* (i.e. *0x1234*).

1.1 Abbreviations:

Abbreviation	Description
b	bit
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 100000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SRAM	Static RAM
T1	1.544 Mbit G.703 Interface
SC4000	SCSA controller
SC-Bus	Time-Slot Interchange Bus of the SCSA
SCC	Serial Communication Channel of the MPC860
SCSA	Signal Computing System Architecture



2 Introduction

4.1 General Information

The NPMC-4E1/T1 is a high performance telecommunication module with four E1 / T1 line interfaces and a SC-Bus interface.

It is implemented as a standard PCI Mezzanine Card Type 1.

General features:

- Four E1 or T1 line interfaces
- SC-Bus Interface on PMC P14 connector
- Multiplexer cross connect between E1/T1 interfaces and SCBus
- Single-slot VME solution together with VMEbus PMC carrier board
- PCI 2.1 standard compliant bus interface

Features of the Line Interface Circuits:

- Support of T1 and E1 lines by equipment option
- Clock recovery and jitter attenuation
- Line and path performance monitoring
- Extraction/insertion of the ISDN D-channel by HDLC / LAPD interface

E1 Option:

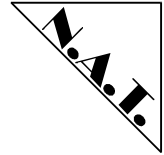
- HDB3 and AMI line code
- CRC-4 multiframe signaling support
- Data extraction/insertion on TS16 for HDLC / LAPD interface
- Indicators for loss of signal, loss of frame alignment, loss of multiframe alignment

T1 Option:

- B8ZS and AMI line code
- Support for frame formats SF, ESF, T1DM(DDS), SLC96
- Loss of signal detection, red, yellow, AIS alarm detection

Features of the Universal Timeslot Interchange (SC4000) circuit:

- Flexible routing of any time slot between each of the 4 framers and the SCbus backplane
- Generation of SCbus Clock master signals
- Support of 2/4/8 MHz bus clock
- Master clock selection between any of the four line interfaces or the SCbus backplane,
- optional free running mode.



Features of the PCI Interface:

- 32 Bit, 33MHz PCI target interface
- 8 bit data, 11 bit address local bus interface
- PCI interrupt support
- Requires only 2 Kbyte address window in PCI memory space

Options:

- Onboard Motorola Coldfire Processor for protocol stack handling
- all line interface signals available on the backplane
- onboard protocol firmware for ISDN and V5.x

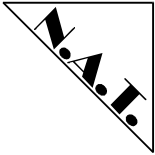
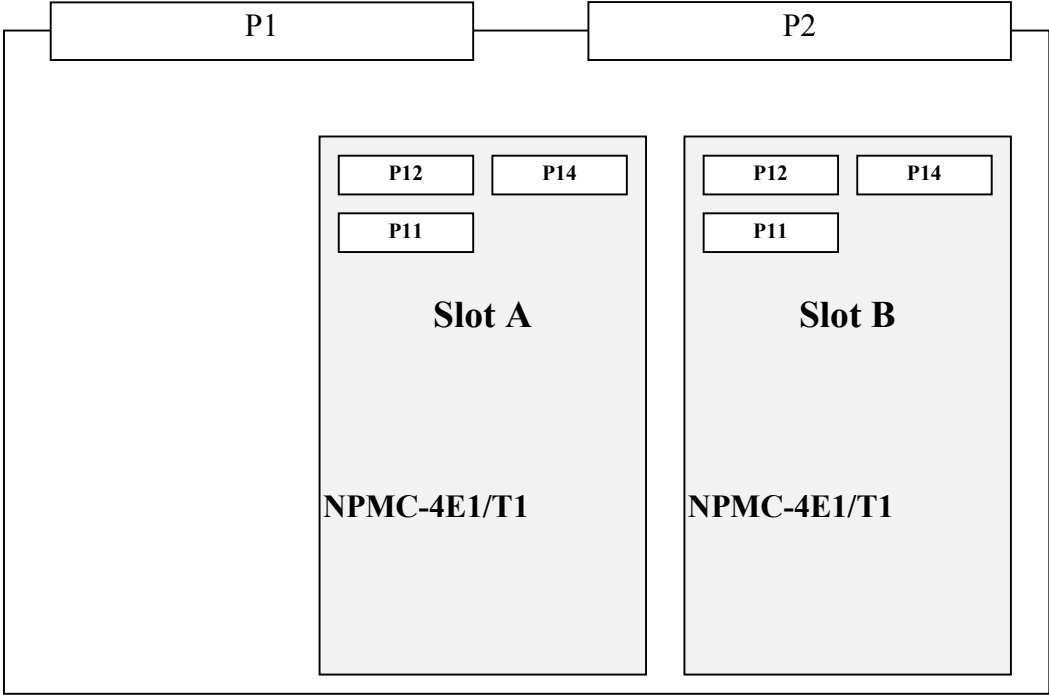


Figure 1: NPMC-4E1/T1 on a VMEbus carrier



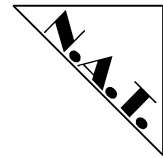
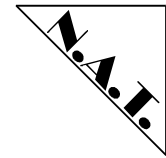


Table 1: NPMC-4E1/T1 Technical Data

PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to ISA bridge	PCI-ISA-001 33MHz
E1 / T1 - Line	Four E1 / T1 interfaces with the PM6341 (E1) or PM4341 (T1), front-panel connectors
SC-Bus	SC4000 Universal timeslot Interchange for SC-Bus, PMC-I/O connector
Firmware	ISDN, V5.1, customer specific
Power consumption	5.0V 1A 3.3V 0.5A
Environment	
Temperature (operating)	0° C to +50 °C
Temperature (storage)	-10 °C to +85°C
Humidity	10 % to 90 % noncondensing
Standards compliance	PCI Rev. 2.1 P1386.1 / Draft 2.0

Please refer to chapter 7 for detailed information about the components mentioned above.



2.1 The NPMC-4E1/T1 Order Codes

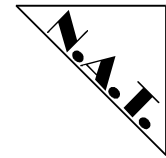
The order codes for NPMC-4E1/T1 are organized according to the following scheme:

NPMC-4SS-OHM-SCSA-A-M

Table 2 shows the meanings of the used abbreviations:

Table 2: NPMC-4E1/T1 Order Codes

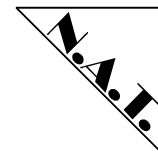
Abbreviation	Description	Option
SS	type of line interface	T1 or E1
OHM	line impedance	100 OHM for T1 120 or 75 OHM for E1
SCSA	SCSA-Bus Interface	0: no SCSA-Bus Interface 1: SCSA-Bus Interface
A	Rear/Front Panel Access	F: Front Panel Access via RJ45 Connectors R: Rear Panel Access via P14
M	Option Coldfire	C: Motorola CPU MCF5206e 4MB DRAM, 2MB EEPROM



2.1.1 NPMC-4E1/T1 – Order Codes – Valid Combinations

Table 3: NPMC-4E1/T1 – Order Codes:
NPMC-4SS-OHM-SCSA-A-M

Product	Name	Description
NPMC-4E1-120-0-R		Interface (I/F): 4x E1 Line Impedance: 120 Ohm SCSA: None I/F Access: Rear Panel Access (front panel access via RJ45 not provided) CPU/Memory: None
NPMC-4E1-120-0-F		Interface (I/F): 4x E1 Line Impedance: 120 Ohm SCSA: None I/F Access: Front Panel Access (rear panel access via P14 not provided) CPU/Memory: None
NPMC-4E1-75-0-R		Interface (I/F): 4x E1 Line Impedance: 75 Ohm SCSA: None I/F Access: Rear Panel Access (front panel access via RJ45 not provided) CPU/Memory: None
NPMC-4E1-75-0-F		Interface (I/F): 4x E1 Line Impedance: 75 Ohm SCSA: None I/F Access: Front Panel Access (rear panel access via P14 not provided) CPU/Memory: None
NPMC-4E1-120-1-R		Interface (I/F): 4x E1 Line Impedance: 120 Ohm SCSA: SCSA-Bus Interface I/F Access: Rear Panel Access (front panel access via RJ45 not provided) CPU/Memory: None
NPMC-4E1-120-1-F-S		Interface (I/F): 4x E1 Line Impedance: 120 Ohm SCSA: SCSA-Bus Interface I/F Access: Front Panel Access (rear panel access via P14 not provided) customer-specific JN5 connector assembled CPU/Memory: None
NPMC-4E1-75-1-F-S		Interface (I/F): 4x E1 Line Impedance: 75 Ohm SCSA: SCSA-Bus Interface I/F Access: Front Panel Access (rear panel access via P14 not provided) customer-specific JN5 connector assembled CPU/Memory: None

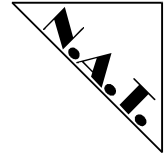


NPMC-4E1-120-1-F	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x E1 120 ohm SCSA-Bus Interface Front Panel Access (rear panel access via P14 not provided) None
NPMC-4E1-75-1-R	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x E1 75 ohm SCSA-Bus Interface Rear Panel Access (front panel access via RJ45 not provided) None
NPMC-4E1-75-1-F	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x E1 75 ohm SCSA-Bus Interface Front Panel Access (rear panel access via P14 not provided) None
NPMC-4T1-100-0-R	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x T1 100 ohm None Rear Panel Access (front panel access via RJ45 not provided) None
NPMC-4T1-100-0-F	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x T1 100 ohm None Front Panel Access (rear panel access via P14 not provided) None
NPMC-4T1-100-1-R	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x T1 100 ohm SCSA-Bus Interface Rear Panel Access (front panel access via RJ45 not provided) None
NPMC-4T1-100-1-F	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x T1 100 ohm SCSA-Bus Interface Front Panel Access (rear panel access via P14 not provided) None
NPMC-4T1-100-1-F-S	Interface (I/F): Line Impedance: SCSA: I/F Access: CPU/Memory:	4x E1 120 Ohm SCSA-Bus Interface Front Panel Access (rear panel access via P14 not provided) customer-specific JN5 connector assembled None

Note:

The ‘Coldfire’ option can be combined with any of the assembly options mentioned above. Example for a T1 board, 100ohm, no SCSA, with front panel access and Coldfire option:

NPMC-4T1-100-0-F-C

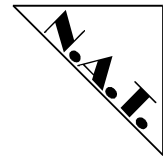


2.2 Safety Note

Electrostatic discharge and incorrect board installation and removal can damage the circuitry or shorten its service life.

To ensure proper operation of the **NPMC-4E1/T1** during its usual lifetime take the following precautions before handling the board.

- Before installing or deinstalling the **NPMC-4E1/T1**, read the Installation Guide and the User's Manual for the PMC carrier board
- Before touching integrated circuits, take all the necessary precautions for handling electrostatic devices.
- Ensure that the **NPMC-4E1/T1** is connected to the carrier board with all three PMC connectors properly seated and that the power is available (GND, +5V, and +3.3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is screwed to the front panel or VME rack and
 - shielded by a closed housing.



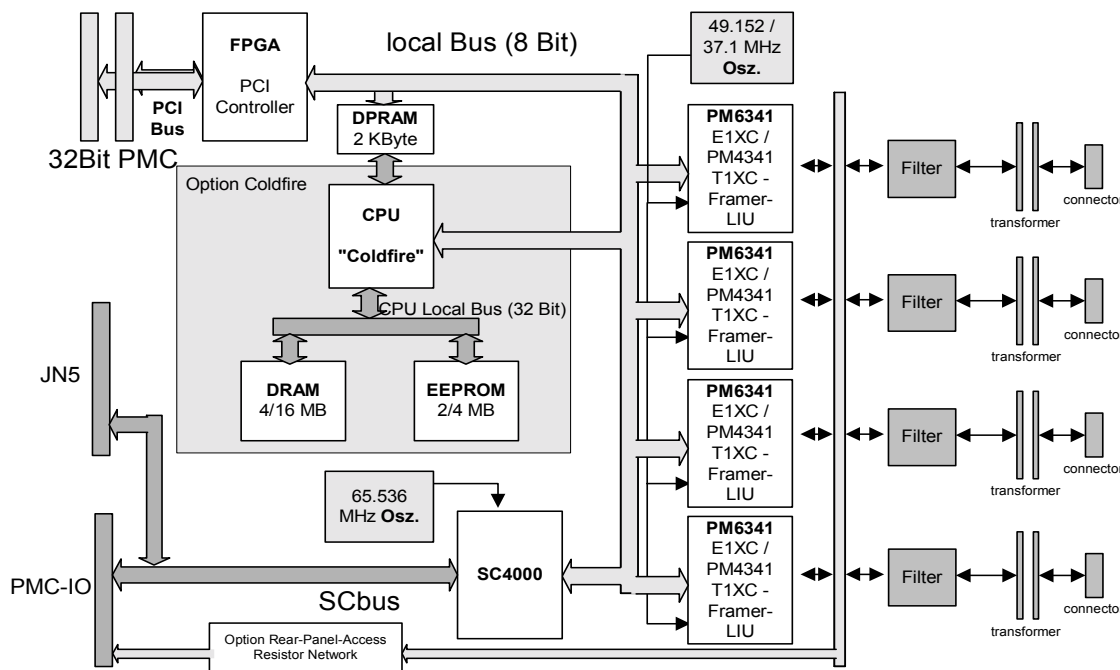
3 Hardware Overview

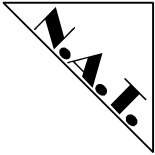
The NPMC-4E1/T1 is a four times primary rate ISDN PMC module. The module contains all components for directly interfacing to a public switched network. All EMC protection logic is included on the board. The board contains four integrated Framer / Line interface units as front ends to the public network. The framer's backside signals are connected to an SC4000 timeslot SCbus controller. The SC4000 enables all timeslots to be routed either between each of the four framers or to the SCbus backplane.

The optional Coldfire CPU enables signaling protocol stack like the ISDN D channel or V5.1 to be processed onboard.

Figure 2 shows a brief overview about the board and its building blocks.

Figure 2: NPMC-4E1/T1 block diagram

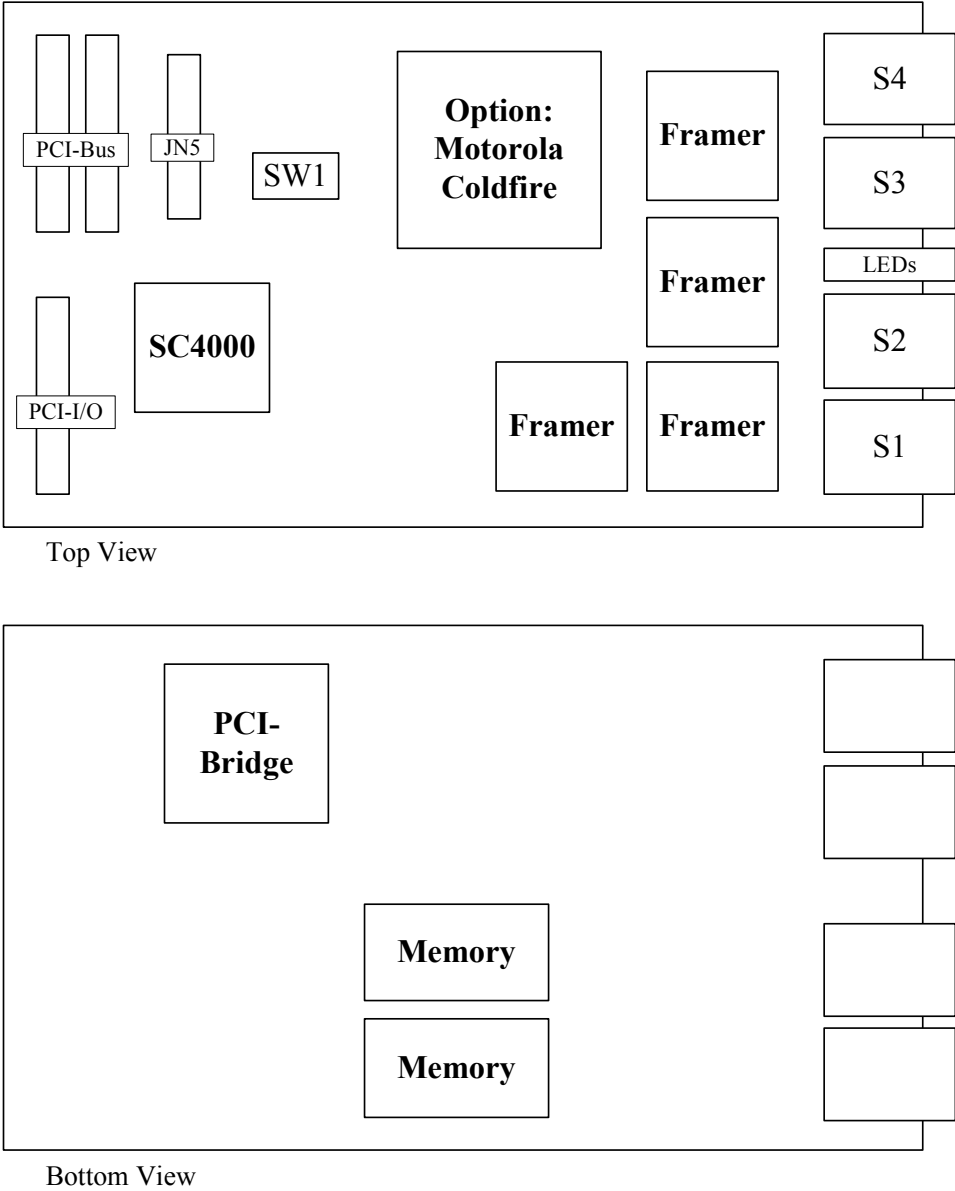


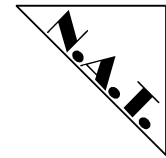


3.1 Location Overview

Figure 3 “Location diagram of the NPMC-4E1/T1” shows the position of the important NPMC-4E1/T1 components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 3: Location diagram of the NPMC-4E1/T1 (schematic)





3.2 The E1 /T1 Framers

The design of the **NPMC-4E1/T1** incorporates up to four E1 or T1 interfaces. For controlling the line interface an integrated Framer / Line Interface Unit (LIU) from PMC Sierra has been chosen. The framer is available as an E1 or T1 version. One side of the framers directly connect to the magnetics / analogue components of the line interface. The other side connects by it's backplane interface to the SC4000 time slot interchange unit (SC4000). The backplane interface builds a 2048MHz TDM bus with 32 timeslots, each of 8 bits wide. The backplane interface runs synchronous to the clock / frame sync signals fed back by the SC4000 device.

For detailed information about the E1/T1 framer, please refer to the manufacturers manuals PM6341 (for E1) and PM4341 (for T1) (contact: see Chapter 9).

From N.A.T. drivers for the PM6341 and PM4341 are available.

For more detailed information, please contact N.A.T..

3.3 The SC4000 Universal Timeslot Interchange Unit

The SC4000 timeslot interchange unit has got two main purposes:

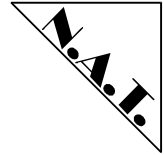
- 1.) Routing of timeslots between the frames and the SCBus backplane
- 2.) Determination of the clock master and supplying the master clock to all onboard devices.

The local interfaces of the SC4000 are directly connected to the backplane interface of the framer chips. The local clock input signals are connected to the framers RFP signal. The RFP signal is the recovered line clock signal, thus running synchronous to the clock supplied by the public network. By programming the corresponding registers, one of the local framer clocks or the backplane clock can be chosen as the master clock. The master clock is than fed back to all framers for use as the transmit and backplane clock.

For the use and functions of the SC4000 please refer to the manufacturers manual of the SC4000 device (see Chpater 9).

From N.A.T. drivers for the SC4000 are available.

For more detailed information, please contact N.A.T..



3.4 The Telecom Data Path

The telecom data path connects the onboard line interface circuits / framers and the SCbus controller. Figure 4 shows the principal interconnection of these units.

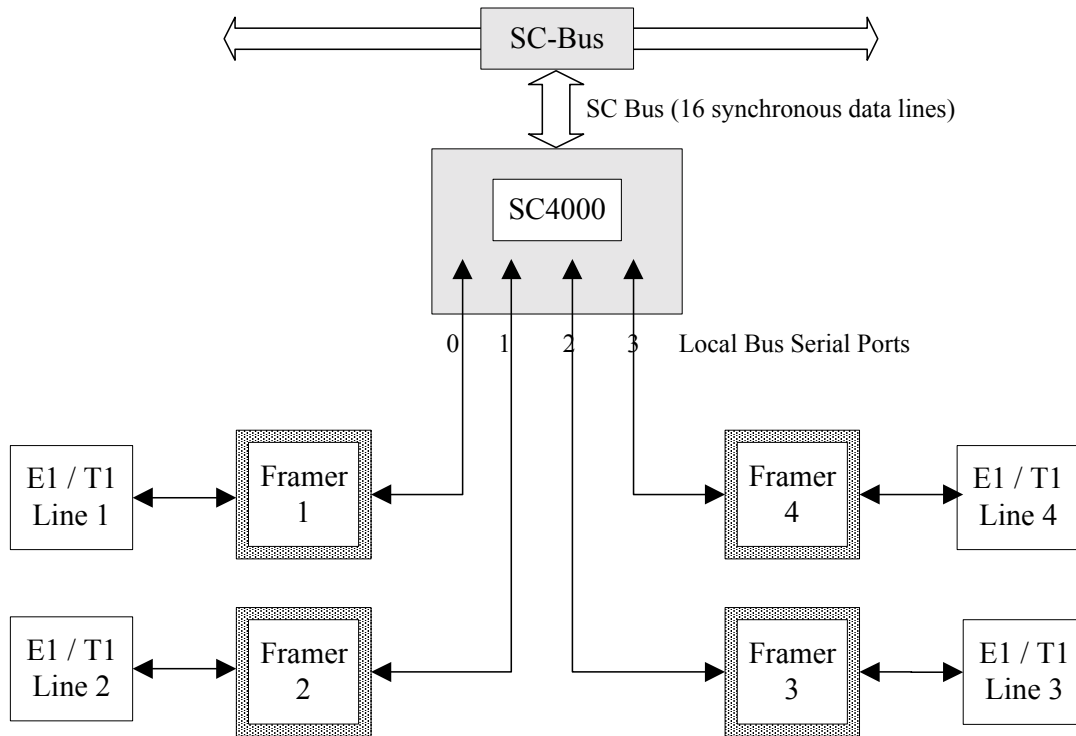
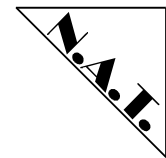


Figure 4: The Telecom Data Path

Every E1/T1 framer utilizes a 32 timeslots (full-duplex) backplane interface at 2.048MHz. When using the T1 framer option only 24 timeslots of the available 32 timeslots are used. The framers backplane interface adapts to SC4000 four local serial ports. Every local B-channel can be routed from the framers to timeslots on the SC-Bus or vice versa. It is also possible to route timeslots between the framers.



Within such a construct there should be only one clock master. By means of the SC4000 the clock master for the internal devices can be chosen to be either Framer1-4 or the SCBus master clock. The SC4000 is also capable of generating the SCBus master clock. The internal master clock is fed back to the framer devices to drive the transmitter section of each framer. Figure 5 shows the clock distribution network.

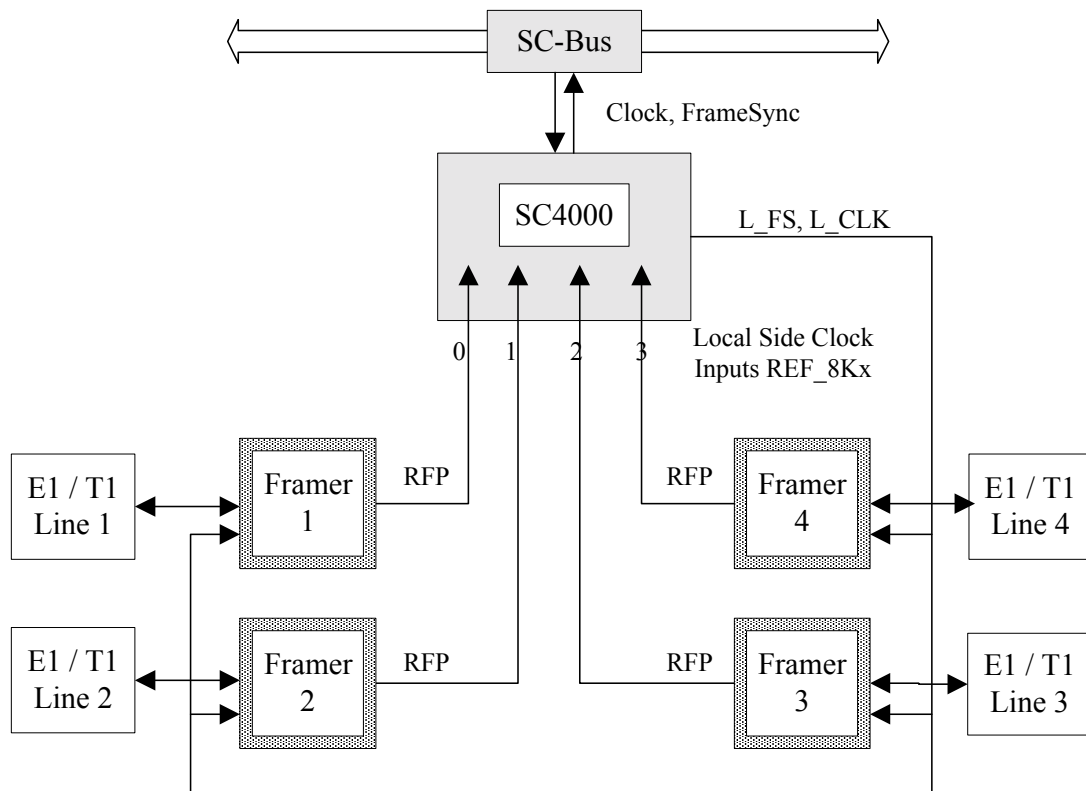
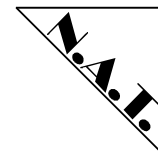


Figure 5: Clock distribution network



3.5 The PCI to Local Bus Bridge

The **NPMC-4E1/T1** is equipped with a standard PCI-to-local bus bridge, which has been implemented in a FPGA. The local bus is directly connected to the onboard devices by glue logic. In case the Coldfire option is equipped the local devices are controlled by the Coldfire CPU and the local side of the PCI bridge connects to a dual port memory. For info on how to program the PCI bridge please refer to Chapter 7.

3.6 Internal Interrupt Channels on the PCI-bus

All internal interrupt sources (SC4000, framers) are logically ORed and connected to the PCI bridge, which routes them to the PCI INTA line. The interrupt disappears as soon as the interrupt is cleared in the interrupt causing device. The source of an interrupt can be determined by reading the IRQ_REG register. For info on how to program the PCI bridge please refer to Chapter 7.

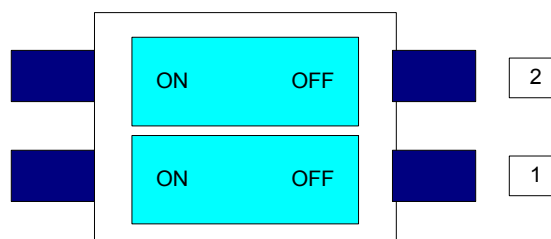
3.7 Automatic Power Up

In case of a PCI Reset the **NPMC-4E1/T1** will automatically put its onboard devices into RESET state. The LEDs on the front-panel will be switched off.

3.8 The Switch Settings

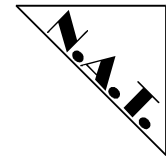
There is a 2-position DIP switch (SW1) on the **NPMC-4E1/T1**, which is used for selection of TSI data routing and FPGA selection.

Figure 6: DIP Switch SW1



Switch no. 1 defines the behavior of the PCI bridge and the internal register interleave for the I/O devices:

- Position ON: All registers of the onboard I/O devices are byte interleaved. The required memory space on the PCI bus for the module is 2 kbyte.
- Position OFF: All registers of the onboard I/O devices are quad byte interleaved. The required memory space on the PCI bus for the module is 8 kbyte.



Switch no. 2 selects the path for the SCbus clock, sync, and data lines D0 – 7. If set to ON, these signals are routed to the PMC I/O connector P14. If set to OFF, these signals are routed to the connector JN5.

4 Memory Map

4.1 PCI Address Window

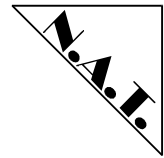
The NPMC-4E1/T1 occupies 8 KByte of address space within the memory space of the PCI bus. Under normal conditions the board will be detected by the BIOS routine of the Host CPU and an appropriate base address and PCI window will be assigned to the board. Due to the amount of locations required for the internal devices (Framers, SC4000 etc.) the device **must** be mapped into PCI memory space.

4.2 The Memory Map

The following table gives a detailed overview of the internal address map of the NPMC-4E1/T1. All addresses are given as offsets to the PCI memory space base address.

Table 4: The Memory Map

Address	Offset	Device	Access	Comments
0x000		Framer 1	byte r/w	
0x100		Framer 2	byte r/w	
0x200		Framer 3	byte r/w	
0x300		Framer 4	byte r/w	
0x400		SC4000	byte r/w	
0x500		IRQ_Reg	byte read only	Source of interrupt
0x600		SC-BusID	byte read only	SCSA Bus ID and configuration bits
0x700		LED-Register	byte r/w	LED and configuration settings register



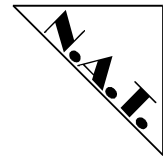
4.3 Register Description

4.3.1 IRQ_Reg – Status of Interrupt Lines (address offset 0x500, read only)

By means of the IRQ_Reg the status of the interrupt lines of the individual devices can be determined. If one of the onboard interrupt sources is active, the PCI_INT_A line is activated as well.

The following table shows the assignment of the IRQ_Reg register bits.

Bit	Function
D0	Framer 1 interrupt active
D1	Framer 2 interrupt active
D2	Framer 3 interrupt active
D3	Framer 4 interrupt active
D4	SC4000 interrupt active



4.3.2 SC-Bus-ID (address offset 0x600, read only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E1 / T1 CONFIG		RES	SCBUS-ID 4	SCBUS-ID 3	SCBUS-ID 2	SCBUS-ID 1	SCBUS-ID 0

- E1 / T1 CONFIG

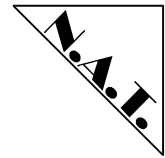
Bit 7	Bit 6	Function
0	0	Reserved
0	1	T1 with 100 Ohm
1	0	E1 with 120 Ohm
1	1	E1 with 75 Ohm

- RES

This bit is reserved for future use

- SCBUS_ID [4:0]

These bits reflect the SC-Bus ID when the **NPMC-4E1/T1** is placed in slot B of a PMC carrier. This bits directly show the status of the PMC I/O connector P14 (pin 27, 30, 29, 32, 31). The PMC I/O is available on VMEbus P2 according to the VITA specification in case this is supported by the carrier board.



4.3.3 LED-Control Register (address offset 0x700, read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	unused	F_SEL2	F_SEL1	LED4	LED3	LED2	LED1

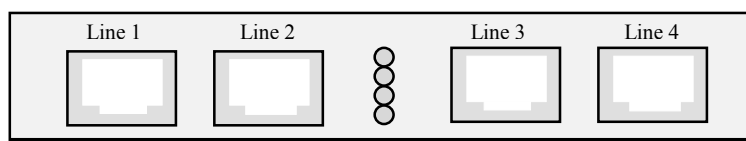
- LED 1-3
These bits control the status of the front panel LEDs.
- FSEL1,2
Frame Pulse and clock select. These bits determine the source of the frame sync and clock signals to be routed to the backplane in case the SC4000 device is not equipped.

There is the possibility of installing bi-coloured LEDs optionally. In this case high and low chooses the colour of the LED. Using a one-colour LED, setting the corresponding bit LOW turns the LED off and setting it HIGH turns it on. If you're using the backplane signals, the function depends of course on the polarity of your LED's connected. Please contact N.A.T., if this feature is desired.

5 Front Panel Elements

5.1 The E1/T1 Connectors

Figure 7: NPMC-4E1/T1 front-panel



- LINE1: E1/T1 line
- LINE2: E1/T1 line
- LINE3: E1/T1 line
- LINE4: E1/T1 line

5.1.1 Pin Assignment - Line Connectors

Figure 8: The E1/T1 Connector

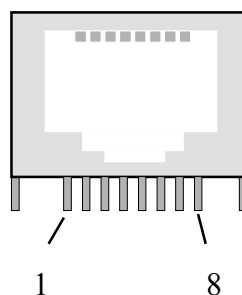
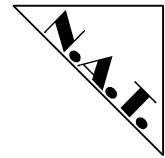


Table 5: Pin Assignment of the E1/T1 connectors

Pin	Signal	
5	Tx+	Output
4	Tx-	Output
2	Rx+	Input
1	Rx-	Input

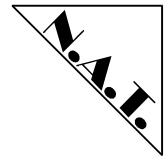


5.2 The LEDs

Figure 9: The LEDs

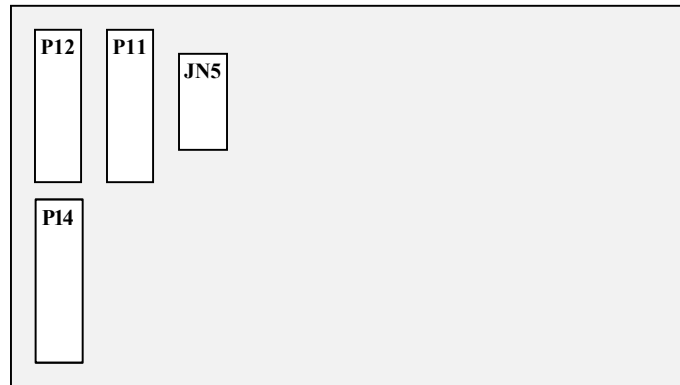
D4
D3
D2
D1

There are four software programmable LEDs on the **NPMC-4E1/T1** to indicate the status of the line interfaces. The LEDs can be programmed by use of the LED control register (see also chapter 4.3.3).



6 Connectors

Figure 10: The Connectors on the NPMC-4E1/T1



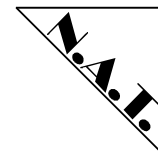
6.1 The PMC Connectors

The following pages specify the pin assignment of the PMC connectors of the NPMC-4E1/T1. While P11 and P12 are specified in the PMC, resp. PCI specification, P14 is manufacturer specific and reserved for proprietary I/O signals.

The NPMC-4E1/T1 P14 supports the SCbus.

P13 is not available on the NPMC-4E1/T1.

Please refer to the following tables to look up the pin assignment of the P11, P12 and P14 of the NPMC-4E1/T1.



6.1.1 Pin Assignment of the PMC Connector -- P11

Table 6: Pin Assignment of the PMC Connector -- P11

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	TCK	-12V	2	n.c.
GND	3	GND	/INT A	4	/IRQ-QSPAN
n.c.	5	/INT B	/INT C	6	n.c.
n.c.	7	bus mode 1	+5V	8	+5V
n.c.	9	/INT D	PCI_RSV1	10	n.c.
GND	11	GND	PCI_RSV2	12	n.c.
CLK	13	CLK	GND	14	n.c.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
n.c.	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
n.c.	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	n.c.
n.c.	41	/SDONE	/SB0	42	n.c.
PAR	43	PAR	GND	44	GND
n.c.	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
n.c.	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	n.c.

6.1.2 Pin Assignment of the PMC Connector -- P12

Table 7: Pin Assignment of the PMC Connector -- P12

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	+12V	/TRST	2	n.c.
n.c.	3	TMS	TDO	4	n.c.
n.c.	5	TDI	GND	6	GND
GND	7	GND	PCI_RSV3	8	n.c.
n.c.	9	PCI_RSV	PCI_RSV4	10	n.c.
n.c.	11	BUS-MODE 2	+3.3V	12	+3.3V
/RST	13	/RTS	BUS-MODE 3	14	n.c.
+3.3V	15	+3.3V	BUS-MODE 4	16	n.c.
n.c.	17	PCI_RSV	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESV D	34	n.c.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	n.c.
+3.3V	53	+3.3V	PCI_RESV	54	n.c.
n.c.	55	PCI_RESV	GND	56	GND
n.c.	57	PCI_RESV	PCI_RESV	58	n.c.
GND	59	GND	PCI_RESV	60	n.c.
n.c.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	n.c.

6.1.3 Pin Assignment of the PMC Connector -- P14 (PMC I/O)

Table 8: Pin Assignment of the PMC Connector -- P14

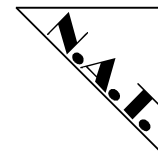
Ext. signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
MC	1	I/O	I/O	2	SD_15
SD_14	3	I/O	I/O	4	SD_13
SD_12	5	I/O	I/O	6	GND
SD_11	7	I/O	I/O	8	SD_10
SD_09	9	I/O	I/O	10	SD_8
SD_07	11	I/O	I/O	12	GND
SD_06	13	I/O	I/O	14	SD_5
SD_04	15	I/O	I/O	16	SD_3
SD_02	17	I/O	I/O	18	SD_1
GND	19	I/O	I/O	20	SD_0
CLKFAIL	21	I/O	I/O	22	FSYN CN
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	SCLKx2N
SL_4L	27	I/O	I/O	28	n.c.
SL_2L	29	I/O	I/O	30	SL_3L
SL_0L	31	I/O	I/O	32	SL_1L
RX1+	33	I/O	I/O	34	TX1+
RX1-	35	I/O	I/O	36	TX1-
RX2+	37	I/O	I/O	38	TX2+
RX2-	39	I/O	I/O	40	TX2-
RX3+	41	I/O	I/O	42	TX3+
RX3-	43	I/O	I/O	44	TX3-
RX4+	45	I/O	I/O	46	TX4+
RX4-	47	I/O	I/O	48	TX4-
GND	49	I/O	I/O	50	GND
LED1a	51	I/O	I/O	52	LED2a
LED3a	53	I/O	I/O	54	LED4a
NC	55	I/O	I/O	56	NC
GND	57	I/O	I/O	58	GND
V24_RX	59	I/O	I/O	60	V24_TX
LED1b	61	I/O	I/O	62	LED2b
LED3b	63	I/O	I/O	64	LED4b

6.1.4 Description P14 Signals

Table 9: Description P14 Signals

Signal	Description VITA Spec.	Description SC4000 Manual	Description General
MC	identical	identical	SC-Bus message channel
SD_15	identical	identical	SC-Bus serial data stream 15
SD_14	identical	identical	SC-Bus serial data stream 14
SD_13	identical	identical	SC-Bus serial data stream 13
SD_12	identical	identical	SC-Bus serial data stream 12
SD_11	identical	identical	SC-Bus serial data stream 11
SD_10	identical	identical	SC-Bus serial data stream 10
SD_9	identical	identical	SC-Bus serial data stream 9
SD_8	identical	identical	SC-Bus serial data stream 8
SD_7	identical	identical	SC-Bus serial data stream 7
SD_6	identical	identical	SC-Bus serial data stream 6
SD_5	identical	identical	SC-Bus serial data stream 5
SD_4	identical	identical	SC-Bus serial data stream 4
SD_3	identical	identical	SC-Bus serial data stream 3
SD_2	identical	identical	SC-Bus serial data stream 2
SD_1	identical	identical	SC-Bus serial data stream 1
SD_0	identical	identical	SC-Bus serial data stream 0
GND	identical	identical	Ground
CLKFAIL	identical	identical	SC-Bus System Clock Fail signal
SREF_8K	SREF8k	identical	SC-Bus 8 kHz Reference
n.c.	identical	identical	Not Connected
SL_0L	SL_0		SC-Bus ID SC4000
SL_1L	SL_1		SC-Bus ID SC4000
SL_2L	SL_2		SC-Bus ID SC4000
SL_3L	SL_3		SC-Bus ID SC4000
SL_4L	SL_4		SC-Bus ID SC4000
RXi+,RXi-			Framer Line Interface differential input
TXi+,TXi-			Framer Line Interface differential output
V24_TX			Coldfire CPU console interface RS232
V24_RX			Coldfire CPU console interface RS232
LED1-4a			Led driver for Bi-Color LED
LED1-4b			Led driver for Bi-Color LED

For more details please refer to the *SC4000 User's Manual* and the *VITA Extensions to ANSI/VITA 6 - 1994 SCSA*.



6.1.5 SC-Bus IDs

In any SCSA system each of the SCSA devices needs to have a unique ID.

The NPMC-4E1/T1 supports the setting of SC IDs by jumpers or switches on the VMEbus backplane. The value of the switch settings can be read out from SCSC_ID register.

6.1.6 NPMC-4E1/T1 P14 Specials

The PMC I/O (P14) is available on the VMEbus P2 connector according to the VITA specification in case this is supported by the carrier board.

According to the PMC specification the PMC module on slot A of the carrier board can occupy 64 pins on the P2, the PMC module on slot B only 32 pins.

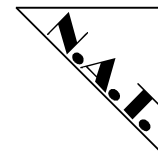
The SC-Bus specific signals on the P14 of the NMC-4E1 are available on pins 1 to 32.

6.2 The JN5 Connector

The following table specifies the pin assignment of the JN5 connector of the NPMC-4E1/T1, and how JN5 is related to the PMC I/O connector P14.

Table 10: Description JN5 Signals

Signal	Pin on P14	Pin on JN5	Description
SCLK	24	1,5,9, 21,25,29, 2,6,10, 22,26,30	Clock for DSP A Clock for DSP B Clock for DSP C Clock for DSP D
FSYNC	22	15,17 35,37 16,18 36,38	Frame Sync for DSP A Frame Sync for DSP B Frame Sync for DSP C Frame Sync for DSP D
SD0	20	11	RX Data DSP A
SD1	18	13	TX Data DSP A
SD2	17	31	RX Data DSP B
SD3	16	33	TX Data DSP B
SD4	15	12	RX Data DSP C
SD5	14	14	TX Data DSP C
SD6	13	32	RX Data DSP D
SD7	11	34	TX Data DSP D

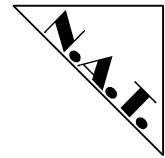


7 PCI Bridge

The PCI to Local Bus Bridge on the NPMC-4E1/T1 is implemented by an Altera FPGA device EP1K10-2.

The PCI bridge of the NPMC-4E1 has a Type 00h Configuration Space header. The following table details the values after reset:

Field	Value	Comment
Vendor ID:	0x2014	
Device ID:	0x040a	
Command / Status:	0x02000002	Medium Devsel – Memory Space supported
Class Code:	0xff8000	
Revision ID:	0x23	0x24 on V2.4 Layout version
BIST:	0x00	
Header type:	0x00	
Latency timer:	0x00	
Cache line Size:	0x00	
Base address Register 0:	0x00000000	
Base address Register 1:	0x00000000	- not supported -
Base address Register 2:	0x00000000	- not supported -
Base address Register 3:	0x00000000	- not supported -
Base address Register 4:	0x00000000	- not supported -
Base address Register 5:	0x00000000	- not supported -
CardBus CIS:	0x00000000	- not supported -
Subsystem Id:	0x0000	
Subsystem Vendor Id:	0x0040	
Expansion rom addr:	0x00000000	- not supported -
reserved:	0x00000000	
reserved:	0x00000000	
Maximim latency:	0x00	
Minimum Grant:	0x00	
Interrupt pin:	0x01	Interrupt on INTA
Interrupt line:	0x00	



8 Reference Documentation

8.1 *PCI Interface Chip*

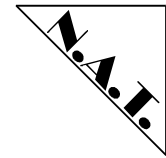
Company: Altera
101 Innovation Drive
San Jose, CA 95134
Phone 408-544-7000
<http://www.altera.com>
Title: ACEX 1K
Programmable Logic Device Family

8.2 *E1 or T1 line interface*

Company: PMC-Sierra, Inc.
8501 Commerce Court, Burnaby, BC V5A 4N3 Canada
Phone 604-668-7300
<http://www.pmc-sierra.com>
Title: PM6341 E1XC
E1 Framer / Transceiver (issue 7 or later)
or
PM4341 E1XC
T1 Framer / Transceiver (issue 6 or later)

8.3 *SCSA-Bus-Interface*

Company: VLSI Technology, Inc.
1109 McCay Drive, San Jose, CA 95131
Phone 408-434-3000
<http://www.vlsi.com>
Title: SC4000
Universal timeslot Interchange



9 APPENDIX A -- Document's History

Revision	Date	Description	Name
0.1	1999	initial revision	ga
1.0	1999	reworked for Rev. 2.0 of the NPMC-4E1/T1 board	hl
	13.12.1999	updated diagrams	as
	28.02.2000	added the IRQ_Reg assignment register	as
	13.03.2000	manual structure reworked	hl
	16.03.2000	updated table 2: NPMC-4E1/T1 Nomenclature	mz
	16.03.2000	updated table 3: NPMC-4E1/T1 Scope of Delivery	
	20.03.2000	reworked chapter 5	hl
	21.03.2000	added LED bi-colour informations to 6.3.3	mz
1.1		reworked for Rev. 2.3 of the NPMC-4E1/T1 board	hl
1.2	28.08.2003	reworked for Rev. 2.4 of the NPMC-4E1/T1 board, added JN5 connector and description of Altera FPGA	ga