NPCIe-PMC
PCIe Carrier for PMC Modules
Technical Reference Manual V1.0
HW Revision 1.0

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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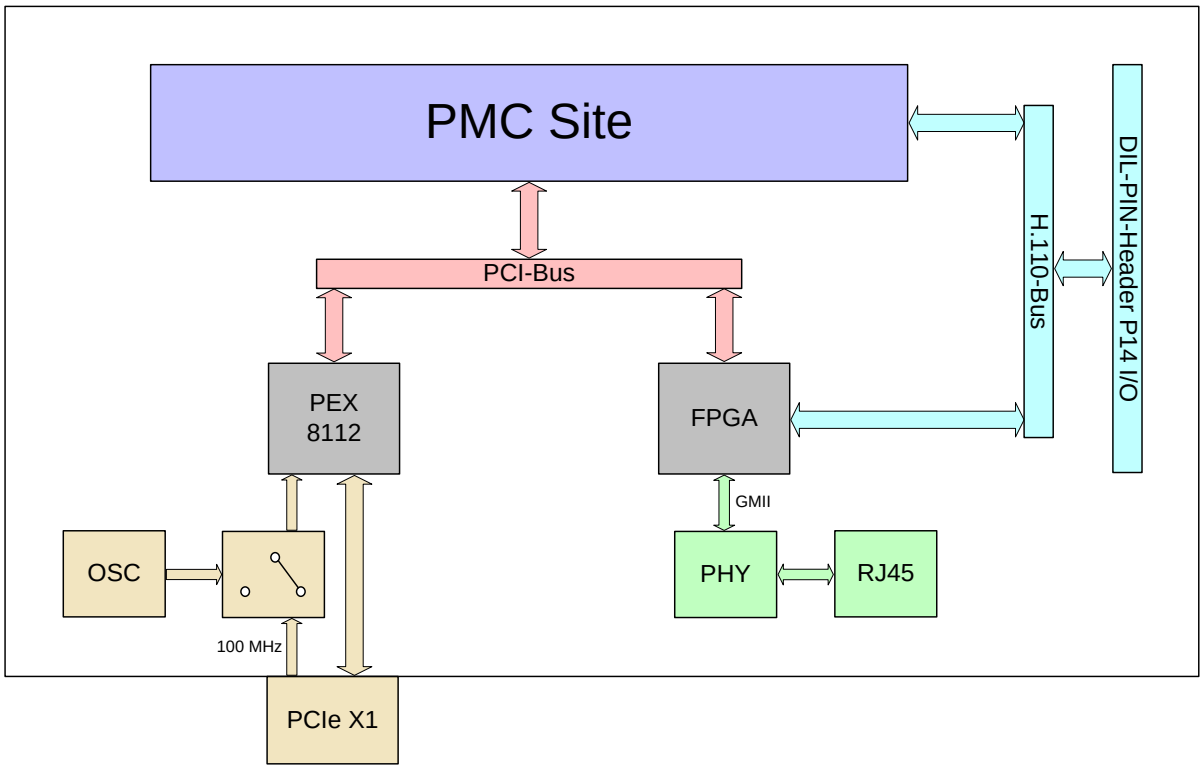
1 Introduction

The **NPCIe-PMC** is a PCIe carrier board intended for use with a PMC module. It allows the use of standard PMC modules in a standard PC with PCIe extension slots.
Functionality of the carrier it determined both by the content of an onboard FPGA device as well as selecting between different assembly options.
The standard variant of this board offers a PCIe to PCI conversion along with the capability to access the PMC module's TDM bus via a pin header intended for ribbon cable connection.

Figure 1: Block Diagram of the NPCIe-PMC



1.1 Board Features

- **Interfaces**

  PCI/PCIe: The **NPCIE-PMC** includes a 1 – lane (x1) PCI Express interface. This is implemented in a PEX8112 PCIe to PCI bridge (PLX). The PCI Express interface is connected directly to the PCI Express connector. While the PCI interface is connected to the FPGA and to the PMC connector.

  Ethernet: The **NPCIE-PMC** implements a Gigabit Ethernet interface (1000Base-T) at the backside that is connected to the onboard FPGA. It can be used for optional data path implementations.

  iTDM: The **NPCIE-PMC** implements a serial iTDM interface, that is based on Ethernet. The iTDM interface is implemented in FPGA logic and conforms to the SFP.0 and SFP.1 specifications. Please note that the TDM to ITDM conversion feature is optional as the default path for the PMC module's TDM data is the CT Bus mentioned below.

  CT Bus: The **NPCIE-PMC** implements a CT-Bus (H.110) that connects to the PMC connector and to a pin header. Via the pin header a TDM bus connection based on ribbon cable (H.100) can be established.

- **FPGA**

  The FPGA operating on the NPCIe-PMC is a Lattice ECP2M device that offers around 50.000 Logic Elements and 4Mbit of internal memory. As it is the connection point between the internal PCI bus, the TDM (H.110) bus and the Ethernet interface it can be used to implement interworking functionality between these three interfaces.

1.2 Board Specification

Table 1: NPCIe-PMC Specification

PCI Express Module	Standard height, half length PCI Express x1 add-in card	
	(111.15mm x 168.00mm)	
Front-I/O	PMC Faceplate	
Power consumption (depending on PCM)	12V 2.0A max.	
Environmental conditions	Temperature (operating):	0°C to +65°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PCI Express Base Specification Rev. 1.1	
	PCI Express CEM Specification Rev. 1.1	

2 Installation

2.1 Bus Interface

- PCIe x1 interface

2.2 Power Supply

The NPCIe-PMC draws very little power from the supplies for its internal circuitry. The PMC +5V are generated from the PCIe +12V line. Primary power consumption depends on the PMC module used.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

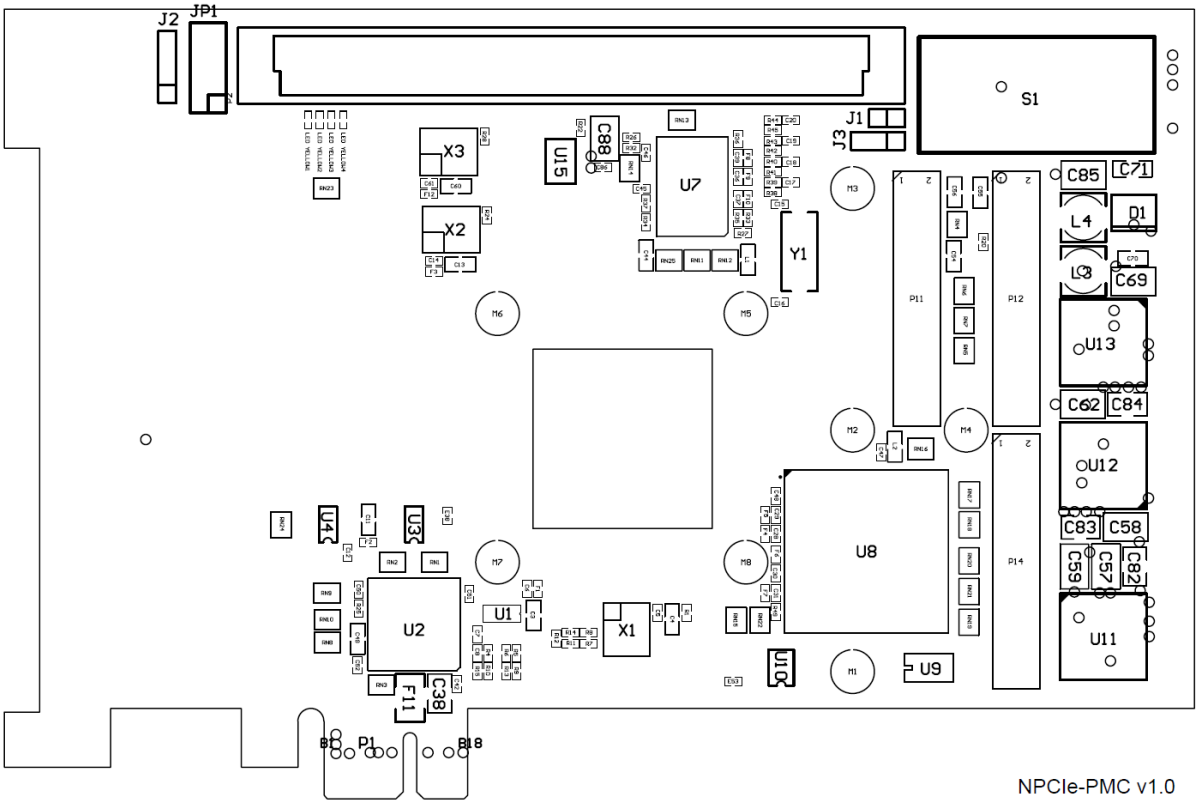
2.3.4 Product Safety

The board complies to EN60950 and UL1950.

3 Hardware Description

This chapter contains a brief description of the functional blocks of the NPCIe-PMC extender board.

Figure 2: Location Diagram of the NPCIe-PMC



3.1 Hardware Overview

The **NPCIe-PMC** is a PCIe extension card that allows the operation of PCI based PMC modules in a PCIe based PC environment. It connects the PCI interface of a PMC module into the PCIe structure of a standard PC. Furthermore it offers beside the standard TDM operation via the pin header and ribbon cable multiple paths of interworking regarding the TDM interface of a PMC module.

3.2 PCIe Bus Connectivity

The PCIe to PCI bridge PEX8112 is the connecting element between the PC's PCIe system and the local PCI bus consisting of the PEX8112 itself, the FPGA and the PMC module. Both the FPGA and the PMC module can trigger interrupts towards the PCIe root complex using the regular PCI interrupt lines. In addition, both the FPGA and the PMC module can perform bus master cycles either targeting the local PCI bus or a device in the PCIe system.

3.3 TDM Connectivity

The TDM bus coming from a PMC module can be connected to various data paths. One option is to use the pin header and a ribbon cable to establish a H.100 TDM bus towards an further TDM device operating in the PC. This is the standard option for the NPCIe-PMC.
Next option is to use the FPGA and its attached Ethernet interface to realize a TDM to ITDM conversion. Here TDM traffic travels via Ethernet packets to some destination either inside or outside the PC operating in.
Finally it is possible to realize a TDM to PCI interworking inside the FPGA, that offers the PC to transmit and receive TDM data via its PCI(e) infrastructure.
Please note that both the Ethernet and the PCI based TDM transport paths are customer specific implementations and that the standard option for the TDM path is usage of the pin header along with ribbon cable (H.100).

3.4 Ethernet Connectivity

Due to lack of space at the PCIe card face plate a RJ45 jacket is assembled at the inner side of the NPCIe-PMC carrier. It connects via a GMII interface attached PHY to the FPGA and is primary intended to carry ITDM traffic resulting from a TDM to ITDM conversion within the FPGA. The ITDM core within the FPGA is capable of converting the full capacity of the H.110 bus in ITDM and vice versa. In numbers this means the ITDM core supports 4096 full duplex channels either transported in 125µs of 1m ITDM data mode or a mixture of both.

3.5 Power Supply

Power is taken from the PCIe bus with the PMC +5V being generated by DC/DC converter U13 from the PCIe bus +12V. The PMC +3,3V is taken directly from the PCIe connector +3,3V.

4 Connectors

4.1 PMC Connectors

Table 2: PMC Connectors P11 and P12

P11				P12			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	TCK	-12V	2	1	+12V	TRST#	2
3	Ground	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	Ground	6
7	NC	+5V	8	7	Ground	PMC-RSVD	8
9	INTD#	PMC-RSVD	10	9	PMC-RSVD	PMC-RSVD	10
11	Ground	NC	12	11	NC	+3.3V	12
13	CLK	Ground	14	13	RST#	NC	14
15	Ground	GNT#	16	15	3.3V	NC	16
17	REQ#	+5V	18	17	PME#	Ground	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38
39	Ground	LOCK#	40	39	PERR#	Ground	40
41	PCI-RSVD	PMC-RSVD	42	41	+3.3V	SERR#	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64

4.2 I/O Connector P14

PMC I/O connector P14 is wired to a VG64 – type connector (rows A – C).

Table 3: PMC I/O Connector P14

P14			
Pin	**Signal**	**Signal**	**Pin**
A1	PMC I/O2	PMC I/O1	C1
A2	PMC I/O4	PMC I/O3	C2
A3	PMC I/O6	PMC I/O5	C3
A4	PMC I/O8	PMC I/O7	C4
A5	PMC I/O10	PMC I/O9	C5
A6	PMC I/O12	PMC I/O11	C6
A7	PMC I/O14	PMC I/O13	C7
A8	PMC I/O16	PMC I/O15	C8
A9	PMC I/O18	PMC I/O17	C9
A10	PMC I/O20	PMC I/O19	C10
A11	PMC I/O22	PMC I/O21	C11
A12	PMC I/O24	PMC I/O23	C12
A13	PMC I/O26	PMC I/O25	C13
A14	PMC I/O28	PMC I/O27	C14
A15	PMC I/O30	PMC I/O29	C15
A16	PMC I/O32	PMC I/O31	C16
A17	PMC I/O34	PMC I/O33	C17
A18	PMC I/O36	PMC I/O35	C18
A19	PMC I/O38	PMC I/O37	C19
A20	PMC I/O40	PMC I/O39	C20
A21	PMC I/O42	PMC I/O41	C21
A22	PMC I/O44	PMC I/O43	C22
A23	PMC I/O46	PMC I/O45	C23
A24	PMC I/O48	PMC I/O47	C24
A25	PMC I/O50	PMC I/O49	C25
A26	PMC I/O52	PMC I/O51	C26
A27	PMC I/O54	PMC I/O53	C27
A28	PMC I/O56	PMC I/O55	C28
A29	PMC I/O58	PMC I/O57	C29
A30	PMC I/O60	PMC I/O59	C30
A31	PMC I/O62	PMC I/O61	C31
A32	PMC I/O64	PMC I/O63	C32

4.3 PCIe Connector P1

P1 is a standard PCIe x1 connector.

Table 4: PCIe Connector P1

P1			
Pin	**Signal**	**Signal**	**Pin**
A1	PRSNT1#	+12V	B1
A2	+12V	+12V	B2
A3	+12V	+12V	B3
A4	GND	GND	B4
A5	TCK	SMCLK	B5
A6	TDI	SMDAT	B6
A7	TDO	GND	B7
A8	TMS	+3.3V	B8
A9	+3.3V	TRST#	B9
A10	+3.3V	+3.3Vaux	B10
A11	/PERST	WAKE#	B11
A12	GND	NC	B12
A13	REFCLK+	GND	B13
A14	REFCLK	PETp0	B14
A15	GND	PETn0	B15
A16	PERp0	GND	B16
A17	PERn0	PRSNT2#	B17
A18	GND	GND	B18

5 Known Bugs / Restrictions

none

6 Document's History

Version	Date	Description	Author
1.0	8.06.2011	initial version	se/te