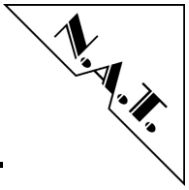

NPCIe-8560-8E1/T1/J1
Telecom PCIe Module
Technical Reference Manual V1.2
HW Revision 1.0

The NPCIe-8560-8E1/T1/J1 has been designed by:

N.A.T. GmbH
Konrad-Zuse-Platz 9
D-53227 Bonn

Phone: +49 / 228 / 965 864 - 0
Fax: +49 /228 / 965 864 - 10

Internet: http://www.nateurope.com

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	Byte
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Dual Data Rate
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
FLASH	Reprogrammable ROM
FPGA	Field Programmable Gate Array
iTDM	internal TDM
J1	1,544 Mbit G.703 Interface (Japan)
LIU	Line Interface Unit
MPC8560	Embedded Processor from Freescale
PCIe	PCI Express
PCI-X	Extended PCI
PowerQUICC III	MPC8560
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCC	Serial Communication Controller of the MPC8560
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC8560
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner

1 Introduction

The **NPCIe-8560-8E1/T1/J1** is a high performance standard height, full length PCI Express x1 add-in card. The **NPCIe-8560-8E1/T1/J1** is providing access to E1/T1/J1 interfaces combined with the functionality of a PMC carrier board. It is intended to be used with standard PMC or PTMC modules in a standard PC with PCI Express extension slots.

2 Overview

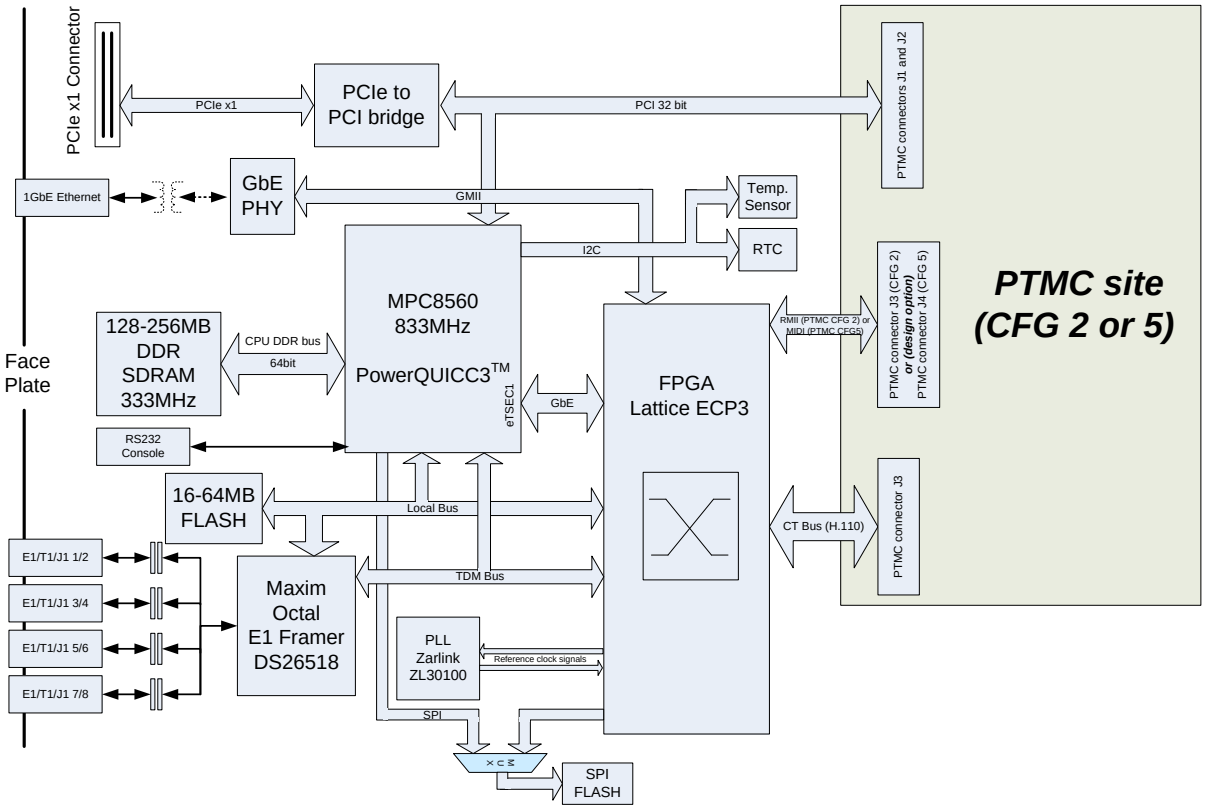
2.1 Major Features

- PowerQUICC III MPC8560 based Embedded PowerPC Architecture
- 128 MB main Memory (DDR SDRAM)
- 16 – 64 MB FLASH (default: 32MB)
- x1 PCI Express Interface Rev. 1.1
- 8x E1 / T1 / J1 Primary Rate Line Interface
- 1000BaseT Ethernet channel on Front Panel
- iTDM Interface
- PTMC Interface for configuration 2/3:
  - 32 bit PCI bus
  - CT bus
  - Ethernet
- RS232 serial I/O

2.2 Block Diagram

The following figure shows a block diagram of the **NPCIe-8560-8E1/T1/J1**.

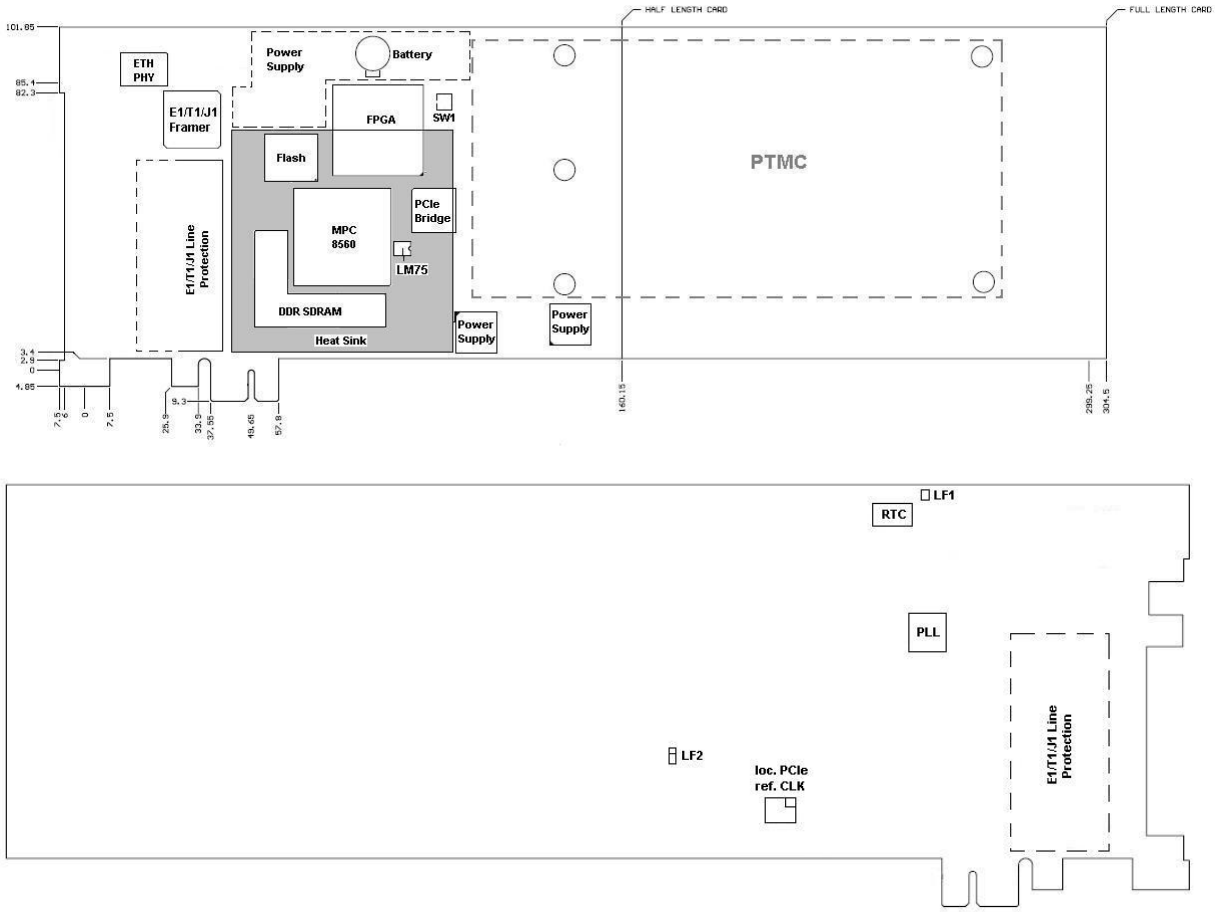
Figure 1: NPCIe-8560-8E1/T1/J1– Block Diagram - Overview



2.3 Location Overview

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 2: NPCIe-8560-8E1/T1/J1 – Location diagram – Overview



3 Board Features

The **NPCIe-8560-8E1/T1/J1** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 CPU

3.1.1 Processor Core

The MPC8560 PowerQUICC III™ is a versatile communications processor that integrates on one chip a high-performance PowerPC™ RISC microprocessor running at 833MHz, a very flexible system integration unit and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PowerPC e500™ core with 32 Kbytes of instruction cache and 32 Kbytes of data cache. To this primary cache adds 256 Kbytes of Level 2 cache. The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system and many other peripherals making this device a complete system on a chip.

3.1.2 Processor – Integrated I/O

The MPC8560 PowerQUICC III™ integrates a switch fabric and 2 10/100/1000 MB MACs, which support various standard protocols.

The communications processor module (CPM) includes four serial communications controllers (SCCs), with the addition of three high-performance communication channels that support new emerging protocols (for example, 155 Mbps ATM and Fast Ethernet). The CPM frequency may be set up to 333 MHz.

The MPC8560 features dedicated hardware that can handle up to 256 full-duplex, time-division-multiplexed logical channels, as well as DMA functionality executing memory to memory and memory to I/O transfers.

Furthermore the MPC8560 integrates a 64 bit PCI / PCI-X interface, and a 4-channel DMA controller.

3.2 Memory

3.2.1 DDR SDRAM

The onboard DDR SDRAM memory is 64 bit wide; its size is 128MB. The interface to the DDR SDRAM is implemented in the MPC8560. By programming several registers the DDR RAM controller can be adapted to different RAM architectures.

3.2.2 FLASH

The **NPCIe-8560-8E1/T1/J1** provides a 16 bit wide FLASH PROM with a capacity of 16 - 64MB (assembly option, default: 32MB). This memory is connected to the demultiplexed upper 16 data bits D0 – 15 and to the latched address lines. Demultiplexing of the local address/data bus of the CPU, as well as address latching, is performed by an FPGA. The FLASH PROM can be programmed either by the CPU (by appropriate software or through the BDM port) or by a PCI bus master.

3.3 PCI Express Interface

The **NPCIe-8560-8E1/T1/J1** includes a x1 PCI Express interface which is implemented in a PEX8111 PCI-X to PCIe bridge (PLX). The *PCI Express interface* is connected directly to the PCI Express connector whereas the *PCI interface* is connected to the MPC8560 CPU and the PMC connector.
The PCIe bridge may receive its reference clock either from the PCIe connector or from a local 100 MHz oscillator circuitry; the clock source is programmable.

3.4 E1/T1/J1 Line Interfaces

The **NPCIe-8560-8E1/T1/J1** carries a Maxim DS26518 framer, which implements eight E1/T1/J1 interfaces. These interfaces connect the framer to the front panel RJ45 connector S3. Timing and interface characteristics can be set up by software within the DS26518. The line interfaces conform to EN60950 and G.703 / G.823 (Jitter Attenuation). The front panel RJ45 connector S3 consists of 4 RJ45 jacks with integrated LEDs. In order to support 8 E1/T1/J1 interfaces each RJ45 jack carries 2 E1/T1/J1 interfaces. The LEDs are bi-colored and programmable through registers which reside within the FPGA.

3.5 Ethernet

The **NPCIe-8560-8E1/T1/J1** implements a Gigabit Ethernet interface (1000Base-T) at the front panel that is connected to the onboard FPGA. All other onboard devices are connected to the same FPGA, which implements a HUB functionality that allows all devices to access the front interface. The connected devices are the TSEC Ethernet MAC of the MPC8560 CPU as well as the PMC/PTMC (connected to the FPGA via RMII) and the iTDM block implemented in the FPGA. (The PMC is only connected via a 100MBit interface.)

The Broadcom BCM5461 Ethernet PHY is connected to the FPGA via GMII interface. It connects to the front panel connector S1.

3.6 PTMC Interface

The **NPCIe-8560-8E1/T1/J1** implements a CT-Bus (H.110) that connects to the PMC connector.

3.7 iTDM

The **NPCIe-8560-8E1/T1/J1** implements a serial iTDM interface based on Ethernet. The iTDM Block (implemented in the FPGA) has also access to the Ethernet Hub block. Therefore the iTDM Block can transfer data through the same physical ports that connects to the front panel interface or the PTMC.
The iTDM interface conforms to the SFP.0 and SFP.1 specifications.

3.8 I^2C Devices

The **NPCIe-8560-8E1/T1/J1** features an I²C link which is connected to the MPC8560 I^2C interface and to a couple of local devices.
The following devices are connected:

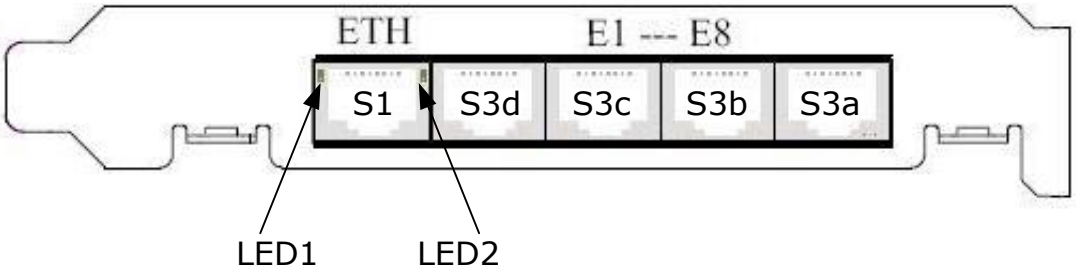
- An EEPROM for storage of board-specific information (24C08)
- A temperature sensor (LM75) which is located near the MPC8560 CPU to sense the processor temperature
- A real time clock device (DS1339C)

4 Hardware

4.1 Front Panel and LEDs

The following figures shows the LEDs placed on the front panel of the **NPCIe-8560-8E1/T1/J1**.

Figure 3: NPCIe-8560-8E1/T1/J1 – Front Panel View

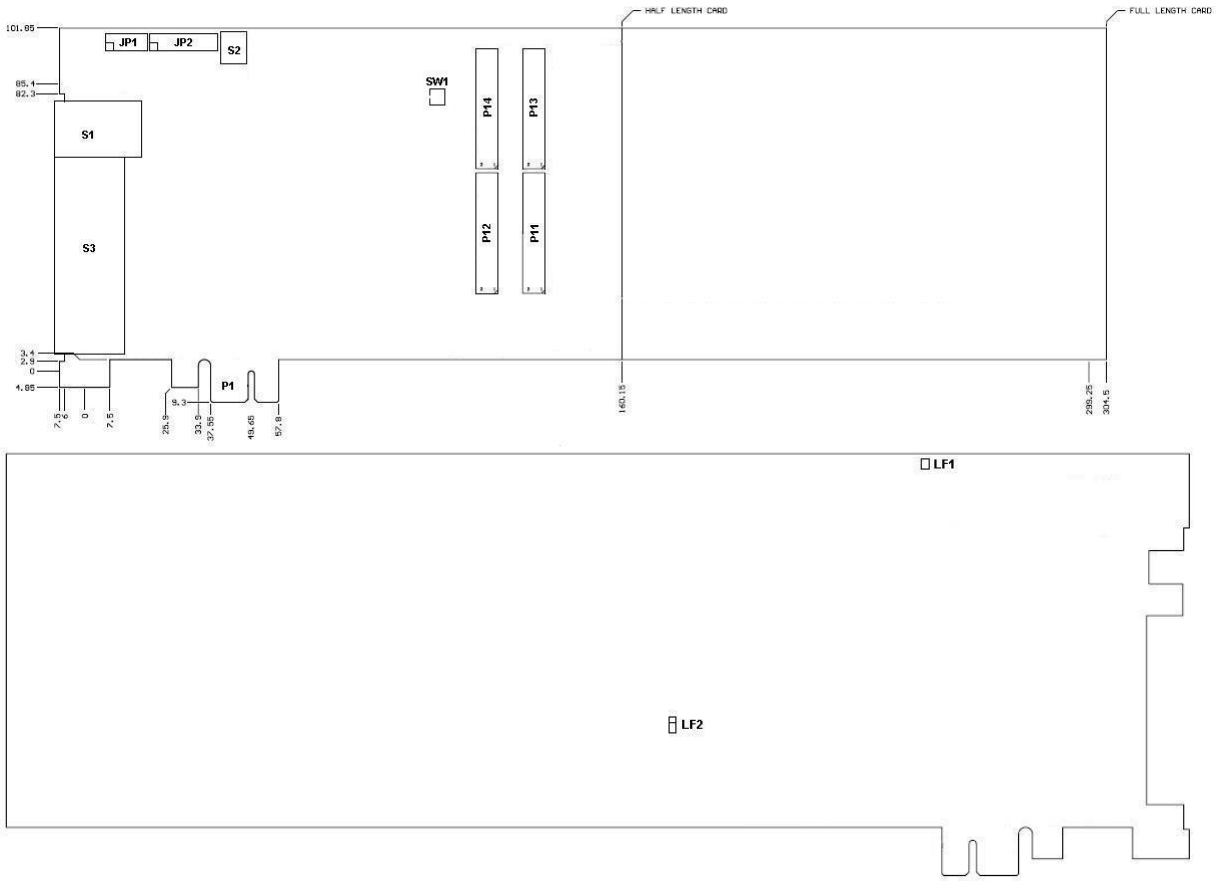


The **NPCIe-8560-8E1/T1/J1** module is equipped with 2 LEDs, which are controlled by the Ethernet PHY. They are integrated in the RJ45 Ethernet interface jack. LED1 is showing the link status and LED2 shows the activity.

Please refer to Chapter 4.2 for detailed information about the front panel connectors.

4.2 Connectors and Switches

Figure 4: NPCIe-8560-8E1/T1/J1 – Connector and Switch location – Overview



Please refer to the following sub-chapters to look up the connector pin assignment of the **NPCIe-8560-8E1/T1/J1.**

4.2.1 P1: PCI Express Connector

P1 is a standard PCIe x1 connector.

Table 2: P1: PCIe Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
A1	PRSNT1#	+12V	B1
A2	+12V	+12V	B2
A3	+12V	+12V	B3
A4	GND	GND	B4
A5	TCK	SMCLK	B5
A6	TDI	SMDAT	B6
A7	TDO	GND	B7
A8	TMS	+3.3V	B8
A9	+3.3V	TRST#	B9
A10	+3.3V	+3.3Vaux	B10
A11	/PERST	WAKE#	B11
A12	GND	NC	B12
A13	REFCLK+	GND	B13
A14	REFCLK-	PETp0	B14
A15	GND	PETn0	B15
A16	PERp0	GND	B16
A17	PERn0	PRSNT2#	B17
A18	GND	GND	B18

4.2.2 S1: Ethernet Connector

The following table shows the pin assignment of RJ45-connector S1. This connector carries the 1000BaseT signals of the Ethernet interface.

Table 3: S1: Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MX0+	MX0-	2
3	MX1+	MX2+	4
5	MX2-	MX1-	6
7	MX3+	MX3-	8

4.2.3 S3: ISDN Connector

The ISDN front panel connectors are 8-pin RJ45 connectors. The 8 E1/T1/J1 line interfaces are available on the pins of the front panel connectors S3a – S3d; each connector carries two interfaces. The following tables show the pin assignments.

Table 4: S3a: ISDN Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX7+	RX7-	2
3	RX8+	TX7+	4
5	TX7-	RX8-	6
7	TX8+	TX8-	8

Table 5: S3b: ISDN Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX5+	RX5-	2
3	RX6+	TX5+	4
5	TX5-	RX6-	6
7	TX6+	TX6-	8

Table 6: S3c: ISDN Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX3+	RX3-	2
3	RX4+	TX3+	4
5	TX3-	RX4-	6
7	TX4+	TX4-	8

Table 7: S3d: ISDN Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RX1+	RX1-	2
3	RX2+	TX1+	4
5	TX1-	RX2-	6
7	TX2+	TX2-	8

4.2.4 JP1: Lattice Programming Port

Connector JP1 connects the JTAG- or programming port of the Lattice FPGA devices.

Table 8: JP1: Lattice Programming Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	3.3V	TDO	2
3	TDI	/PROGRAMN	4
5	NC	TMS	6
7	GND	TCK	8
9	DONE	INITN	10

4.2.5 JP2: BDM and JTAG Connector

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 9: JP2: BDM and JTAG Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	TDO	nc	2
3	TDI	/TRST	4
5	10K PU to +3.3V	2K PU to+3.3V	6
7	TCK	/CKSTP_IN	8
9	TMS	nc	10
11	/SRESET	nc	12
13	/HRESET	nc	14
15	/CKSTP_OUT	GND	16

4.2.6 P11/P12: PMC Connectors

Table 10: P11/P12: PMC Connectors – Pin Assignment

P11				P12			
Pin #	**Signal**	**Signal**	**Pin #**	**Pin #**	**Signal**	**Signal**	**Pin #**
1	TCK	-12V	2	1	+12V	TRST#	2
3	GND	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	GND	6
7	NC	+5V	8	7	GND	PMC-RSVD	8
9	INTD#	PMC-RSVD	10	9	PMC-RSVD	PMC-RSVD	10
11	GND	NC	12	11	NC	+3.3V	12
13	CLK	GND	14	13	RST#	NC	14
15	GND	GNT#	16	15	3.3V	NC	16
17	REQ#	+5V	18	17	PME#	GND	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	GND	AD[26]	22
23	AD[25]	GND	24	23	AD[24]	+3.3V	24
25	GND	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	GND	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	GND	34	33	GND	PMC-RSVD	34
35	GND	IRDY#	36	35	TRDY#	+3.3V	36
37	DEVSEL#	+5V	38	37	GND	STOP#	38
39	GND	LOCK#	40	39	PERR#	GND	40
41	PCI-RSVD	PMC-RSVD	42	41	+3.3V	SERR#	42
43	PAR	GND	44	43	C/BE[1]#	GND	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	GND	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54
55	AD[04]	GND	56	55	PMC-RSVD	GND	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	GND	PMC-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62
63	GND	REQ64#	64	63	GND	PMC-RSVD	64

4.2.7 P13: PMC Connector

Table 11: P13: PMC Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MDIO	GND	2
3	GND	STX	4
5	MDC	SRX	6
7	RXER	GND	8
9	PTID2	TXD0	10
11	PTGNDZ	TXD1	12
13	REFCLK	GND	14
15	GND	RXD0	16
17	CT_FA	RXD1	18
19	CT_FB	GND	20
21	PTID0	TXEN	22
23	PTGNDZ	CAS_DV	24
25	CT_C8A	GND	26
27	GND	CT_D19	28
29	CT_D18	CT_D17	30
31	CT_D16	GND	32
33	GND	NETREF2	34
35	CT_D14	USER1Z	36
37	CT_D12	GND	38
39	PTENB#	USER2Z	40
41	PTGNDZ	NETREF1	42
43	CT_C8B	GND	44
45	GND	CT_D15	46
47	CT_D10	CT_D13	48
49	CT_D8	CT_D11	50
51	GND	CT_D9	52
53	CT_D6	CT_D7	54
55	CT_D4	GND	56
57	PTID1	CT_D5	58
59	CT_D2	CT_D3	60
61	CT_D0	GND	62
63	GND	CT_D1	64

4.2.8 P14: PMC Connector – Configuration 2/3

Table 12: P14: PMC Connector – Configuration 2/3 – Pin Assignment

P14 (Configuration 2)				P14 (Configuration 3)			
Pin #	**Signal**	**Signal**	**Pin #**	**Pin #**	**Signal**	**Signal**	**Pin #**
1	USER	USER	2	1	TxSOC	GND	2
3	USER	USER	4	3	GND	RXADR4	4
5	USER	USER	6	5	TXCLAV	TXADR4	6
7	USER	USER	8	7	RXADR3	GND	8
9	USER	USER	10	9	USER	GND	10
11	USER	USER	12	11	GND	RXREF	12
13	USER	USER	14	13	TXREF	GND	14
15	USER	USER	16	15	GND	RXENB#	16
17	USER	USER	18	17	TXADR3	RXCLAV	18
19	USER	USER	20	19	TXADR2	GND	20
21	USER	USER	22	21	USER	TXENB#	22
23	USER	USER	24	23	GND	RXADR2	24
25	USER	USER	26	25	TXCLK	GND	26
27	USER	USER	28	27	GND	TXADR1	28
29	USER	USER	30	29	TXADR0	RXADR1	30
31	USER	USER	32	31	TXPRTY	GND	32
33	USER	USER	34	33	GND	RXADR0	34
35	USER	USER	36	35	TXD7	RXPRTY	36
37	USER	USER	38	37	TXD6	GND	38
39	USER	USER	40	39	USER	RXD7	40
41	USER	USER	42	41	GND	RXD6	42
43	USER	USER	44	43	RXCLK	GND	44
45	USER	USER	46	45	GND	RXD5	46
47	USER	USER	48	47	TXD5	RXD6	48
49	USER	USER	50	49	TXD4	GND	50
51	USER	USER	52	51	GND	RXD3	52
53	USER	USER	54	53	+TXD3	RXD2	54
55	USER	USER	56	55	TXD2	GND	56
57	USER	USER	58	57	USER	RXD1	58
59	USER	USER	60	59	TXD1	RXD0	60
61	USER	USER	62	61	TXD0	GND	62
63	USER	USER	64	63	GND	RxSOC	64

For configuration 2 the PTMC Specification does not define a fixed usage for the PINS marked with USER. These pins are connected to the FPGA on the **NPCIe-8560-8E1/T1/J1**. Please contact NAT if a user defined usage of those pins is needed!

4.2.9 S2: RS232 Connector

The following table shows the pin assignment of the RS232 interface.

Table 13: S2: RS232 Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	NC	RxD_SCC1	2
3	TxD_SCC1	NC	4
5	GND		

Connector S2 is connected to SCC1 of the MPC8560 CPM.

4.2.10DIP SW1: Flash Half Select / PCIe Bridge Direction

The table below gives an overview of the operating parameters configurable via DIP SW1. Details are given in the following subchapters.

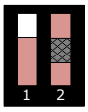
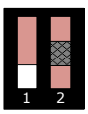
Table 14: DIP SW1: Pin Assignment - Overview

Switch #	Function
1	FLASH half select
2	PCIe Bridge Direction

4.2.10.1 DIP SW1: Switch 1 – Boot FLASH Select Switch

By operating Switch 1 of DIP SW1 to ON, the upper half of the Boot FLASH is selected for booting. If Switch 1 of DIP SW1 is turned to OFF, the lower half of the Boot FLASH is selected for booting.

Table 15: DIP SW1: Switch 1 – Boot Flash Select – Pin Assignment

DIP SW1 – Switch 1	Function
	Upper FLASH Half
	Lower FLASH Half

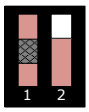
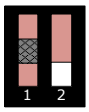
Default:

Switch 1 of DIP SW1 is toggled to OFF, lower half of the Boot FLASH is selected for booting.

4.2.10.2 DIP SW1: Switch 2 – PCIe Bridge Direction Switch

This switch is used to select the source of the PCIe reference clock. If Switch 2 of DIP SW1 is turned to ON a local 100MHz reference is chosen. Additionally the PCI reset from the PEX8112 has no longer impact on the rest of the board. This mode is intended to be selected when the board is used in a standalone application.
If Switch 2 of DIP SW1 is turned to OFF the external reference clock from the PCIe connector is taken.

Table 16: DIP SW1: Switch 2 – PCIe Bridge Direction – Pin Assignment

DIP SW1 – Switch 2	Function
	Local 100MHz Clock
	External Clock from PCIe Connector

Default:
Switch 2 of DIP SW1 is switched to OFF, external clock from PCIe connector selected

4.2.11LF1: Write-Protect-Pin – Solder Field

If the solder field LF1 is closed the Write-Protect-Pin (WP-Pin) of the FLASH is asserted.

Default:
Solder field LF1 is open, FLASH write protection is disabled.

4.2.12LF2: Voltage Source – Solder Field

Solder field LF2 selects the source of the PMC +3.3V_{AUX}. If the solder field is closed towards the mark on the PCB "3.3V AUX", the +3.3V_{AUX} of the PMC is directly connected to the +3.3V_{AUX} of the PCIe connector. If the solder field is closed to the other side the +3.3V_{AUX} of the PMC is sourced by the local generated +3.3V.

Default:
Solder field LF2 is closed towards the mark "3.3V AUX", the PMC +3.3V_{AUX} is sourced by the local generated +3.3V.

5 NPCIe-8560-8E1/T1/J1 Programming Notes

TBD

Note:

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further assistance on programming.

6 Board Specification

Table 17: NPCIe-8560-8E1/T1/J1 – Features

Processor	PowerQUICC III MPC8560 (833MHz) based Embedded PowerPC Architecture
PCI Express Module	Standard height, full length PCI Express x1 add-in card (111.15mm x 312.00mm)
Front-I/O	5x RJ45 connectors
Main Memory	128MB DDR SDRAM
FLASH PROM	16 – 64MB FLASH PROM – on board programmable
Firmware	OK1, LINUX BSP (on request)
Power Consumption (MPC8560 / 833MHz)	12V 2.0A max.
Operating Temperature	0°C – +65°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PCI Express Base Specification Rev. 1.1 PCI Express CEM Specification Rev. 1.1 PICMG 2.15 Rev. 1.0 ITU-T G.703 (for E1/T1 Standard) ITU-T G.823 (Jitter Attenuation)

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NPCIe-8560-8E1/T1/J1** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NPCIe-8560-8E1/T1/J1** read this installation section
- Before installing or uninstalling the **NPCIe-8560-8E1/T1/J1**, read the Installation Guide and the User's Manual of the PC/Server main board used, or of the PCIe system the board will be plugged into.
- Before installing or uninstalling the **NPCIe-8560-8E1/T1/J1** switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPCIe-8560-8E1/T1/J1** is connected to the main board or to the PCIe backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires only

- an PCIe main board or a PCIe backplane for connecting the **NPCIe-8560-8E1/T1/J1**

7.2.2 Power supply

The power supply for the **NPCIe-8560-8E1/T1/J1** must meet the following specifications:

- Required for the **NPCIe-8560-8E1/T1/J1**:
  - +12V / 1.1A typ.
  - +3.3V / 0.9A typ.
- Required for the PMC Module
  - +3.3Vaux / can be connected to 3.3aux of the PMC via LF2 or it can be connected to the local generated +3.3V for the PMC.
  - All other PMC Power supplies (+12V, +5V, +3.3V, -12V) are locally generated out of the +12V from the PCIe connector. That means the complete power that is needed by the PMC will be added to the +12V line of the PCIe connector!

7.2.3 Automatic Power Up

In the following situations the **NPCIe-8560-8E1/T1/J1** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The main board / backplane signals a PCIe Reset.

7.2.4 Thermal Considerations

The **NPCIe-8560-8E1/T1/J1** can be operated in a temperature range of 0°C to +65°C if the air velocity does not fall below 1 m/s. This minimum velocity is required in the region of the CPU's heat sink, the residual area should be passed by air with a minimum velocity of 0.5 m/s.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Freescale, MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual, 7/2004, Rev. 1
[3] Samsung, DDR SDRAM 512 MB C-die, Rev. 1.1, 6/2005
[7] PLX Technology, PEX8112AA, PCI Express to PCI Bridge, Data Book, 11/2007, Rev. 1.1
[8] Zarlink, ZL30100 T1/E1 System Synchronizer, Data Sheet, 11/2005
[10] Maxim, DS26518, 8-Port T1/E1/J1 Transceiver , Rev.: 103008
[11] Spansion, S29GL-N MirrorBit Flash Family Data Sheet, Rev. B, Am. 3, 10/2006
[12] N.A.T., FPGA-TSI Technical Reference Manual, March 2005, Ver. 1.0
[13] N.A.T., iTDM-FPGA Technical Reference Manual, October 2006, Ver. 1.0

Appendix B: Document's History

Revision	Date	Description	Author
1.0	07.07.2010	initial revision	ks
1.1	12.08.2010	Changed Memory size, added LED description, updated connector location diagram.	ks
1.2	20.05.2013	Contact data updated, typo correction	Fh
	04.07.2013 15 .10.2013	Adapted to new layout, reworked Document renamed	Se