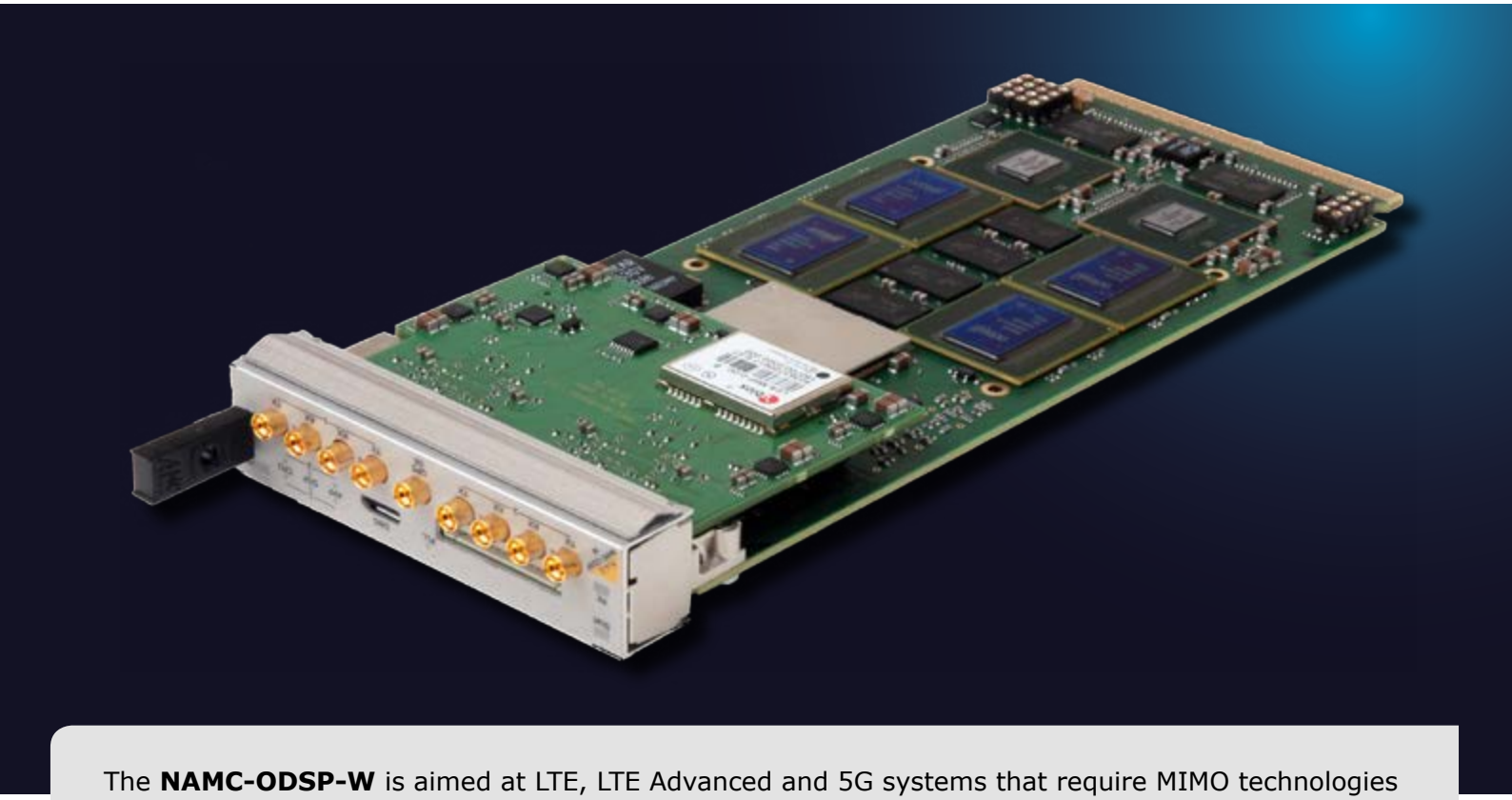
NAMC-ODSP-W

Small Cell & Wireless Processing for ATCA & MTCA



The **NAMC-ODSP-W** is aimed at LTE, LTE Advanced and 5G systems that require MIMO technologies and enables complete RF to Layer 3 wireless basestation functionality to be implemented on a compact, single-wide AdvancedMC module. Combining four RF channels with DSP, FPGA and quad-core ARM based processing, this module includes a comprehensive range of software including a Linux operating system, L2/L3 stack, virtualized core network software and software defined radio PHY firmware. A GPS antenna input on the front panel connects to on-board GPS receiver circuitry for high precision clock synchronization. A variant of the NAMC-ODSP-W offers a dual SFP connector to the front panel to enable a CPRI link to external RF, allowing the module to be used in conjunction with third party remote radio head (RRH) solutions.

Key features

- Four OCT2224W DSPs
- Xilinx Kintex-7 XC7K160T FPGA
- Two NXP LS1043A CPUs
- Broadcom BCM5396
- On-board GPS receiver circuitry
- Control connector to external power amplifier
- Supports up to:
  - 20 km range for all cellular standards
  - 130/50 Mbps LTE throughput
  - 64 3G users

Applications

- LTE
- LTE Advanced
- 5G Network Testing
- MIMO and Massive MIMO Applications

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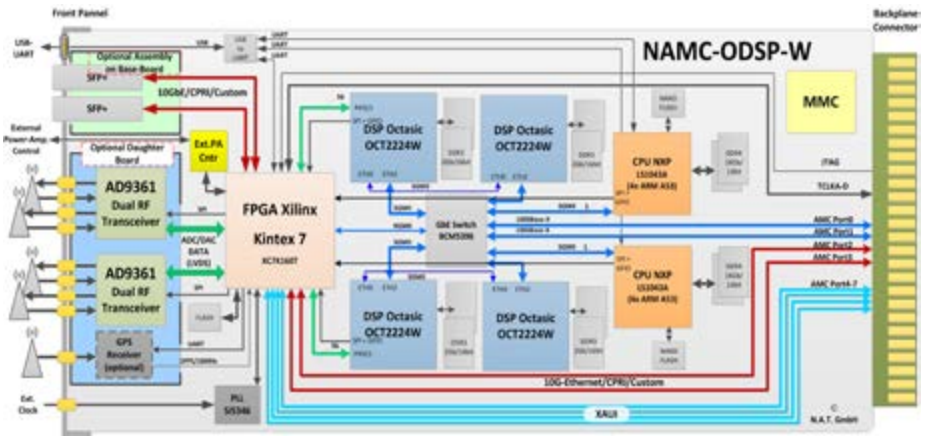
Technical Data

NAMC-ODSP-W



Overview

The **NAMC-ODSP-W** from N.A.T. combines a powerful FPGA with an array of DSPs, two quad-core ARM processors, four RF interfaces and advanced wireless software in a single-width, mid-size AMC module package.

RF Interface

Two Analog Devices AD9361 RF-SoCs offer four Rx and Tx antennas operating between 70Mhz and 6Ghz with up to 56Mhz analog bandwidth.

The RF interface is implemented on a mezzanine module, so it can be easily adapted to new technologies or different RF front ends.

Alternative RF Interface

Dual SFP connector on front panel for CPRI links to external RF.

Subsystem Processor

The on-board Xilinx Kintex-7 FPGA provides pre-DSP data manipulation while also giving you headroom for further extension and customization. This includes efficient linearization, i.e. using a single digital pre-distortion (DPD) per user instead of each power amplifier, and other data pre-processing capabilities.

PHY Processing Array

Four Octasic OCT2224W DSPs, each with 24 DSP cores, provide the specialized power needed for PHY processing. Each DSP is equipped with its own private external 512MB DDR3 memory.

L2/L3 and Core Processing

Two NXP QorIQ® LS1043A processors for L2/L3 and core processing. These quad-core 64-bit ARM-based processors are each supported by 4GB DDR4 memory and feature a data path acceleration architecture.

Switching

A Broadcom BCM5396 device establishes a full-non-blocking interconnect between the DSPs, CPUs, FPGA and backplane and provides an individual data and control path access to these devices.

Clock Interfaces

A GPS antenna input on the front panel connects to on-board GPS receiver circuitry. The module also features an additional external reference clock input on the front panel, a TCLKA-D interface (receive or transmit) on the backplane connector and an on-board Stratum-3 oscillator.

Software

DSPs: Octasic FlexiPHY Firmware

- Four Software Defined Radio (SDR) PHY products
  - GSM, GPRS, EDGE PHY
  - UMTS/WCDMA/HSPA
  - LTE-FDD/LTE-TDD
  - CDMA 2000
- Up to 64 3G users
- Up to 130 / 50 Mbps LTE throughput
- Up to 20 Km range for all cellular standards
- Radio Utility System (RUS)

CPUs:

- Linux operating system
- Radisys L2/L3 stack software
- Existing adaptation of Quortus core network software

Application Optimization

N.A.T. can adapt the NAMC-ODSP-W to suit your application-specific needs with for example, fewer DSPs or a larger FPGA. Please contact us to discuss your requirements.

Key Features

Subsystem Processor

- Xilinx Kintex-7 XC7K160T, FBG676 (160k LE, 12Mbit internal SRAM, 8SerDes, 400 I/0)

PHY Processing Array & Memory

- Four 24-core Octasic OCT2224M DSPs. Each DSP connects to two 16-bit wide DDR3 memory slots. Using 2Gb devices this results in 512MB DRAM per DSP.
- Each DSP has two serial GbE connections to on-board Ethernet switch
- 3W typical power consumption

Backplane Connectivity

- Full AMC TCLKA-D connectivity
- XAUI 10GbE (or custom SerDes protocol) connectivity to Fat-Pipe-Region ports #4-7
- Dual 1GbE connectivity to ports #0 and #1
- CPRI or custom SerDes protocol to ports #2 and #3

Front Panel

- Bi-colour status LEDs, one for each DSP, one for each CPU, two for application status
- PLL lock status LED
- 4x SMP Rx, 4x SMP Tx RF connectors
- GPS antenna RF connector (SMP)
- Control connector to external power amplifier

Operating System Support

- Embedded Linux operating system

Environmental Conditions

Temperature (operating):

- 0ºC to +60ºC with forced air cooling

Temperature (storage):

- -40ºC to +85ºC

Relative Humidity:

- 10% to 90% at +55ºC (non-condensing)

Power Consumption

- 45W typical (TBD)

Standard Compliance

- AMC.0 R2.0, AMC.2, IMPI V1.5 & V2.0, HPM.1
- CE, RoHS, EN61000, EN5022, EN55024