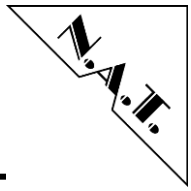
NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.2
Hub Module XAUI HW Revision 1.0



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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SRIO	Serial Rapid IO
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)
XAUI	10 Gigabit Attachment Unit Interface

1 Introduction

The **NAT-MCH** consists of a **BASE-Module**, which can be expanded with additional PCBs. The **BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and up to four power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB-Modules** are available. With the **CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

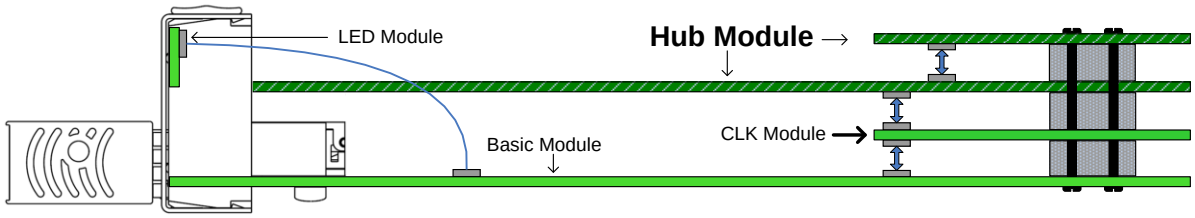
Through the extension of the **NAT-MCH** with a **HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet (XAUI)

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in the following figure.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **Hub-Module XAUI**. In addition to the **CLK-Module** it can be mounted on the **NAT-MCH BASE-Module**. The **HUB-Module XAUI** is in a 6 Slot ("**x24**") and in a 12 slot ("**x48**") option available. With the **HUB-Module XAUI** the 3rd tongue of the **NAT-MCH** connector to the MicroTCA backplane is always installed. With the **x48** option, additional the 4th tongue is installed. The **NAT-MCH HUB-Module XAUI** implements the following major features:

- support of Ethernet switching in configurable speeds (1/2.5/10 Gbit/s) for fabrics D to G of up to 6 AMCs (**HUB-Module XAUI x24)**

- support of Ethernet switching in configurable speeds (1/2.5/10 Gbit/s) for fabrics D to G of up to 12 AMCs (**HUB-Module XAUI x48)**
- support of a 10 Gbit Ethernet update connection to second MCH
- support of 10 Gbit Ethernet switching for two faceplate ports (additional module needed)

The main component of the **HUB-Module XAUI** is a 20 port 10 Gbit Ethernet switch. This switch connects up to 12 AMCs (x48 version), a second MCH and optional two ports at the face plate.

2 Overview

2.1 Major Features

- Ethernet switching in configurable speeds: 1 Gbit/s, 2.5 Gbit/s or 10 Gbit/s for up to 6 AMCs (**HUB-Module XAUI x24**) / 12 AMCs (**HUB-Module XAUI x48**)
- Altera Cyclone II FPGA
- Atmel ATmega16
- Backplane update fabric to second MCH
- 2x 10 Gbit Ethernet uplink ports on faceplate via copper or optical medium (optional)

2.2 Technical Features

Interface features

- Link Aggregation (802.3ad)
- Multi-point link-Ag extensions
- PAUSE flow control (802.3x)

Bridge features

- 16K entry MAC address table
- Spanning Tree (802.1D, s, w)
- VLAN, priority (802.1Q, P)
- 4K VLAN table
- Link Aggregation (802.3ad)
- Duplex Flow Control (802.3x)
- All IEEE protocol traps
- User-defined monitoring and filtering rules
- RMON, and Fulcrum statistics

Security

- Mac address security
- Port access control (802.1x)

Chip performance

- 240 Gbps bandwidth
- Low-latency cut-through switching: 200 ns @ 10G, 650 ns @ 1G.
- Store and Forward mode
- 2x internal switch fabric over speed
- Full speed multicast

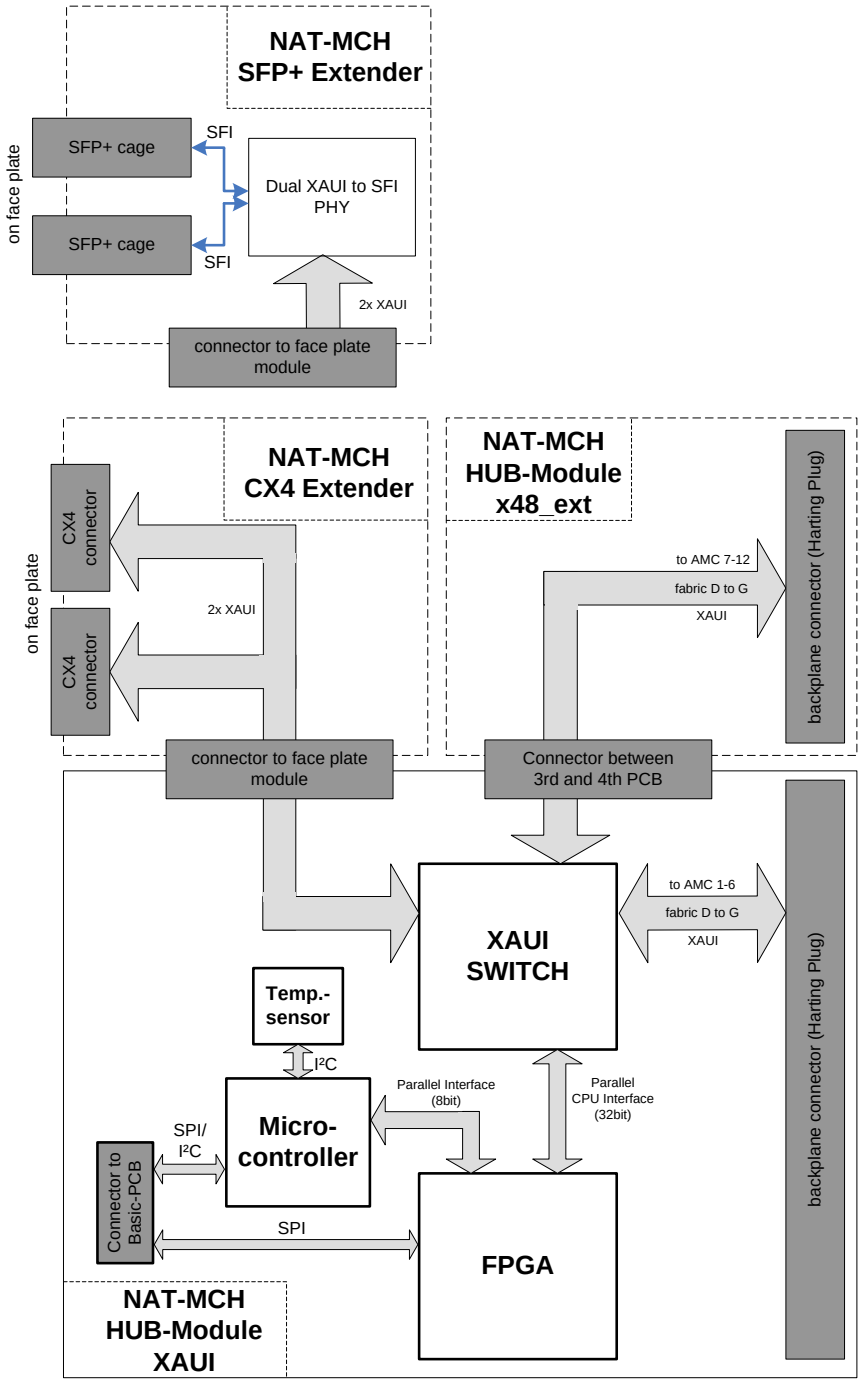
Board Features

- configuration interface via on board microcontroller / FPGA
- 2 onboard temperature sensors

2.3 Block Diagram

The following figure shows a block diagram of the **NAT-MCH HUB-Module XAUI** and optional available extension modules.

Figure 2: NAT-MCH HUB-Module XAUI – Block Diagram



* The HUB-PCB x48_ext is only assembled in the x48 version.
* The CX4 and the SFP+ Extender are only optional. Please note: only one face plate module can be chosen either the CX4 or the SFP+ extender.

2.4 Location Diagram

The following figure shows the position of important components of the **NAT-MCH HUB-Module XAUI**.

Figure 3: NAT-MCH HUB-Module XAUI – Location diagram (top)

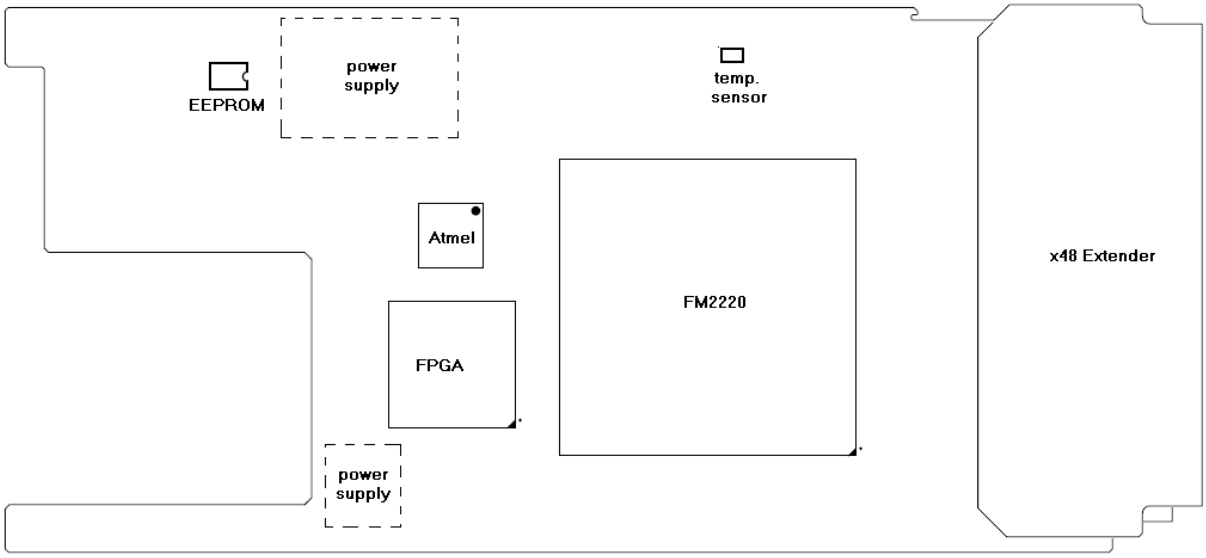
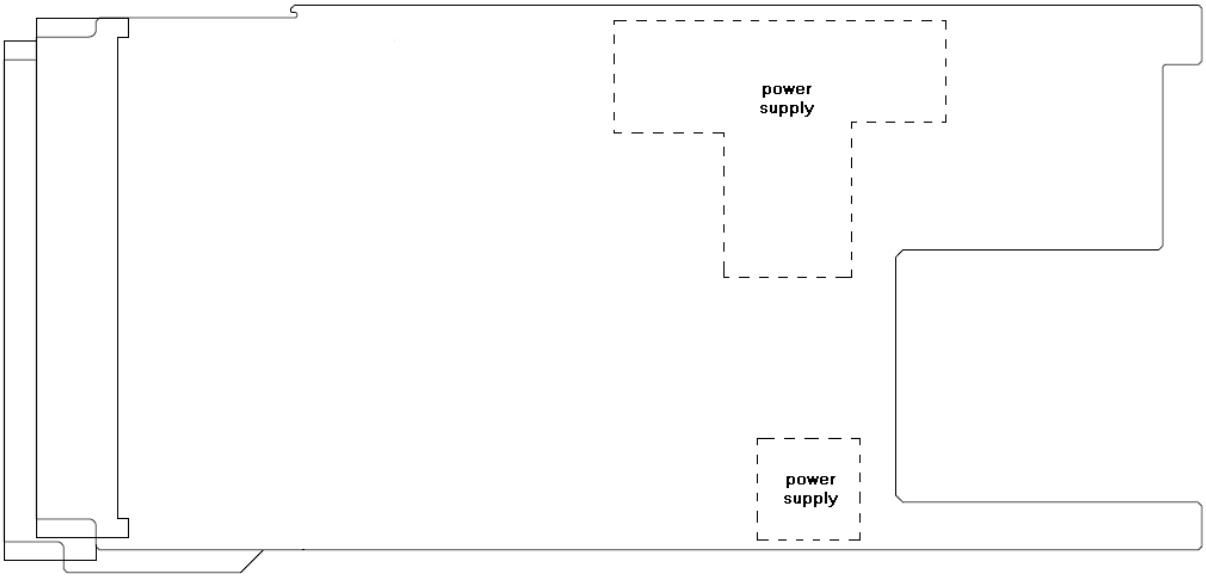


Figure 4: NAT-MCH HUB-Module XAUI – Location diagram (bottom)



3 Functional Blocks

The **NAT-MCH HUB-Module XAUI** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 XAUI Switch

The **NAT-MCH HUB-Module XAUI** is equipped with a Fulcrum Microchip FM2220 switch, which provides high performance, low latency and robust Ethernet packet switching. The FM2220 offers per port configurable speed of 1GbE (one lane), 2.5GbE (one lane), and 10GbE (four lanes/ XAUI). It supports 15 ports in order to connect 12 AMCs, a second MCH and two optional face plate interfaces.

The FM2220 can be configured by an EEPROM, or by accessing the FM2220 register interface via a parallel CPU interface. The CPU on the **NAT-MCH BASE-Module** has access to that interface via the SPI bus. A standard configuration is done by the EEPROM after a reset. The CPU interface has to be used if changes have to be done at the running system.

The following table shows the AMC slot to switch port assignment.

Table 2: AMC Slot to Switch Port assignment

# AMC Slot Fabric D-G	#Port FM2220
AMC1	11
AMC2	13
AMC3	19
AMC4	20
AMC5	14
AMC6	12
AMC7	1
AMC8	21
AMC9	23
AMC10	24
AMC11	22
AMC12	2
2nd MCH	7
front interface 1	Tbd
front interface 2	Tbd

3.2 FPGA

An Altera Cyclone II FPGA is used as "glue logic" to translate between the SPI interface on the **NAT-MCH BASE-Module** and the parallel CPU interface of the FM2220 switch.

3.3 Microcontroller

An 8-bit Atmel ATmega16 microcontroller resides on the **NAT-MCH HUB-Module XAUI**, which can be updated by the CPU on the **BASE-Module** via a SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages over the I²C interface.

The reset signals of the switches can be controlled through programming registers in the microcontroller.

Two temperature sensors are connected to a **HUB-Module XAUI** internal I²C bus. The microcontroller makes these sensors accessible to the CPU on the **BASE-Module** via IPMI.

3.4 Interfaces

The **NAT-MCH HUB-Module XAUI** implements interfaces to connect fabrics D to G of up to 12 AMCs and a second MCH.
With the extension of a face plate module additional two 10GbE interfaces are accessible at the face plate. The physical medium depends on the chosen face plate module. Options are:

- CX4 Extender: 10GBase-CX4 (XAUI)
- SFP+ Extender: this extender provides only two SFP+ cages. The physical medium depends on the chosen SFP+ Transceiver, but it is normally any optical medium.

3.5 Uplink Option

With the uplink option it is possible to connect to the XAUI fabric up to two face plate connectors. This is an assembly option and therefore need to be chosen when ordered.

The speed is set to 10 GbE by default.

4 Hardware

4.1 Connectors

4.1.1 Connector Overview

Figure 5: NAT-MCH HUB-Module XAUI – Connectors (top)

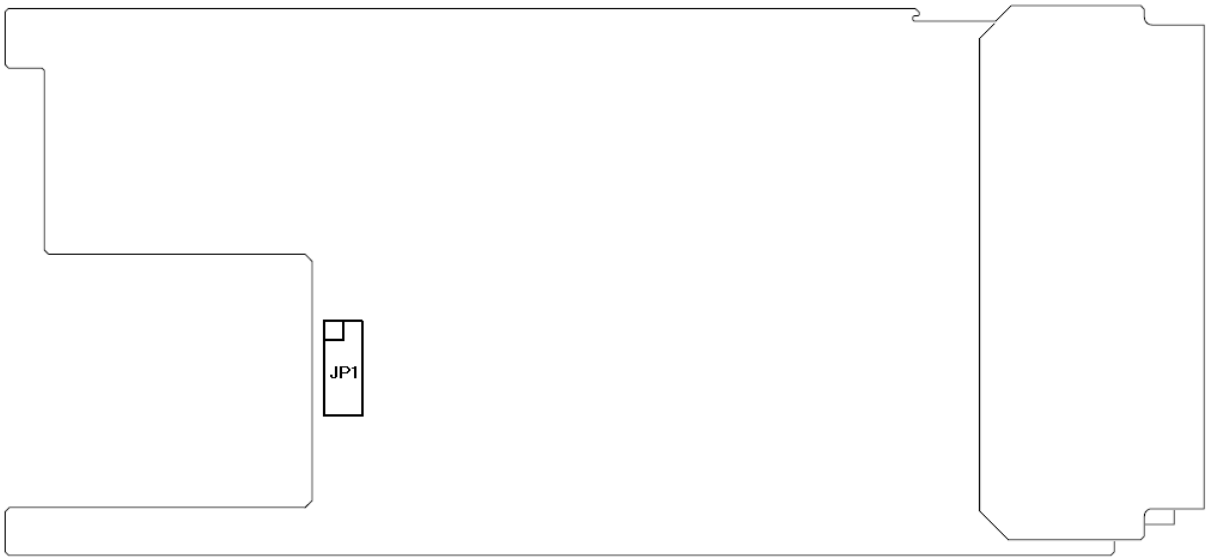
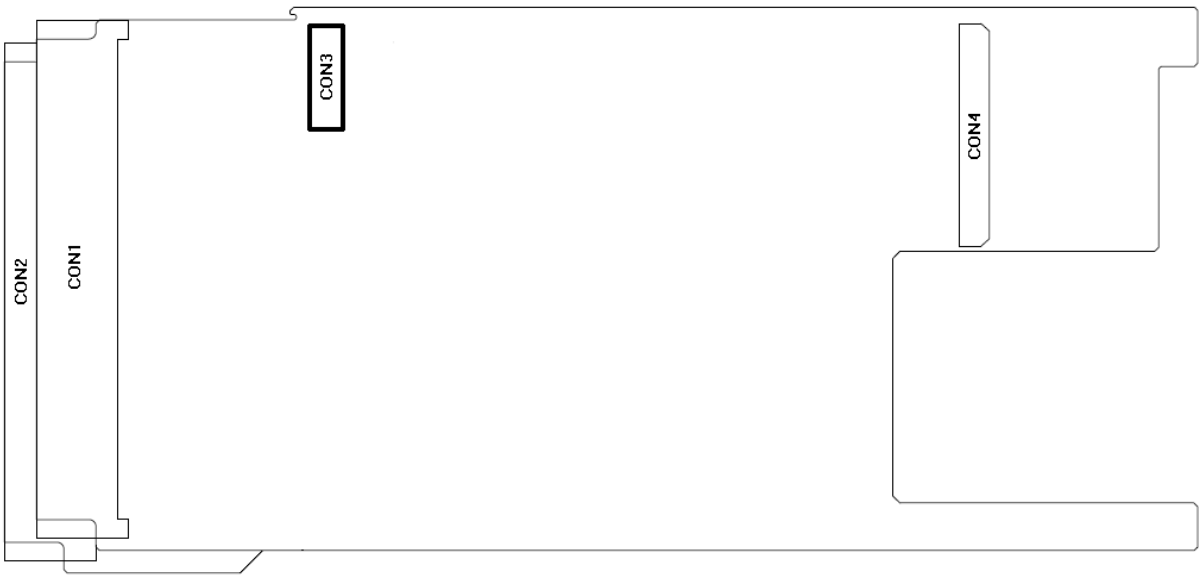


Figure 6: NAT-MCH HUB-Module XAUI – Connectors (bottom)



Please refer to the following tables to look up the pin assignment of the **NAT-MCH HUB-Module XAUI**.

4.1.2 CON1: HUB-Module XAUI Backplane Connector

Table 3: CON1: HUB-Module XAUI Backplane Connector – Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUD+	RxFUD+	163
9	TxFUD-	RxFUD-	162
10	GND	GND	161
11	TxFUE+	RxFUE+	160
12	TxFUE-	RxFUE-	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

4.1.3 CON2: HUB-Module x48 Extender Connector

Table 4: CON2: HUB-Module x48 Extender Backplane Connector – Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUF+	RxFUD+	163
9	TxFUF-	RxFUD-	162
10	GND	GND	161
11	TxFUG+	RxFUE+	160
12	TxFUG-	RxFUE-	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

4.1.4 CON3: CLK-Module Connector

Table 5: CON3: CLK-Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	+12V	+12V	2
3	+12V	+12V	4
5	N.C.	+3.3V_MP	6
7	N.C.	SPICLK	8
9	GND	expansion3	10
11	MOSI	MISO	12
13	GND	/SPISEL_HUBPCB	14
15	SCL	N.C.	16
17	SDA	nRESET_HUB_PCB	18
19	GND	GND	20

This connector connects to the **CLK-Module**. On the **CLK-Module** the signals of this connector are routed through to a connector that connects to the **BASE-Module**.

4.1.5 CON4: Uplink-Module Connector

Table 6: CON4: Uplink-Module Connector – Pin Assignment

Pin No#	Signal	Signal	Pin #
1	GND	GND	2
3	+1.2V	+1.2V	4
5	+1.2V	+1.2V	6
7	GND	GND	8
9	FP_CON_5	FP_CON_1	10
11	FP_CON_6	FP_CON_2	12
13	GND	GND	14
15	FP_CON_7	FP_CON_3	16
17	FP_CON_8	FP_CON_4	18
19	GND	GND	20
21	FP_CON9	FP_CON11	22
23	FP_CON10	FP_CON12	24
25	GND	GND	26
27	UP_LINK1_TD_N	UP_LINK1_RA_P	28
29	UP_LINK1_TD_P	UP_LINK1_RA_N	30
31	GND	GND	32
33	UP_LINK1_TC_N	UP_LINK1_RB_P	34
35	UP_LINK1_TC_P	UP_LINK1_RB_N	36
37	GND	GND	38
39	UP_LINK1_TB_N	UP_LINK1_RC_P	40
41	UP_LINK1_TB_P	UP_LINK1_RC_N	42
43	GND	GND	44
45	UP_LINK1_TA_N	UP_LINK1_RD_P	46
47	UP_LINK1_TA_P	UP_LINK1_RD_N	48
49	GND	GND	50
51	UP_LINK2_TD_N	UP_LINK2_RA_P	52
53	UP_LINK2_TD_P	UP_LINK2_RA_N	54
55	GND	GND	56
57	UP_LINK2_TC_N	UP_LINK2_RB_P	58
59	UP_LINK2_TC_P	UP_LINK2_RB_N	60
61	GND	GND	62
63	UP_LINK2_TB_N	UP_LINK2_RC_P	64
65	UP_LINK2_TB_P	UP_LINK2_RC_N	66
67	GND	GND	68
69	UP_LINK2_TA_N	UP_LINK2_RD_P	70
71	UP_LINK2_TA_P	UP_LINK2_RD_N	72
73	GND	GND	74
75	+3.3V	+3.3V	76
77	+3.3V	+3.3V	78
79	GND	GND	80

4.1.6 JP1: FPGA Programming Interface

Table 7: JP1: FPGA Programming Interface – Pin Assignment

Pin No#	Signal	Signal	Pin #
1	DCLK	GND	2
3	CONF_DONE	+3,3V	4
5	/CONFIG	/CECONF	6
7	DATAO	nCSO	8
9	ASDI	GND	10

5 Programming Notes

The Hub-Module XAUI is connected to the MCH Base-Module by two different interfaces:

- SPI
- I²C

The main purpose of the SPI interface is to provide access to the register set of the FM2220. Additional the SPI interface is connected to the microcontroller; this connection is only used for maintenance purposes, e.g. updating the microcontroller firmware.

The onboard Atmel microcontroller provides a set of registers which can be accessed by proprietary IPMI messages via the I²C Interface. The following chapters are describing the registers and their functions in more detail.

5.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH HUB-Module XAUI**.

Table 8: Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xbb								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**BOARD_ID**							

5.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH HUB-Module XAUI**.

Table 9: PCB_REV Register

PCB Revision – Address 0x01								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**PCB_REV**							

Bit 7 to 4 contains the major revision and bit 3 to 0 contains the minor revision. That means if the PCB revision is e.g. v1.3 the PCB Revision register contains the value 0x13.

5.3 Firmware Version

The Firmware Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH HUB-Module XAUI**.

Table 10: FW_VERSION Register

Firmware Version – Address 0x02								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	Atmel_vers							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the Firmware running on the Atmel is v1.3 the Firmware Version register contains the value 0x13.

5.4 Hub Module XAUI Type

The Hub-Module XAUI Type Register contains the information if the **HUB-Module XAUI** is a type x24 or x48.

Table 11: XAUI_TYP Register

Hub Module XAUI Type - Address 0x03								
Default value 0x24/48								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	XAUI_Mod_Typ							

5.5 FPGA Revision Register

The FPGA Revision Register contains the revision code of the Altera FPGA.

Table 12: FPGA Revision Register

FPGA Revision - Address 0x04								
Default value # of running FPGA revision								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FPGA_REV							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the FPGA is running with the image v1.3 the FPGA Version register contains the value 0x13.

5.6 Switch Control Register

With the Switch Control Register various strapping and reset pins of the FM2220 can be controlled.

Table 13: SW_CTL Register

Switch Control - Address 0x5								
Default value 0x03								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	CONT_EN	SW_EEP-ROM_EN	SW_AUTO-BOOT	SW_CPU _RST_n	SW_CHIP_ RST_n

Table 14: SW_CTL - Register Bits

Bit	Name	Function
0	SW_CHIP_RST_n	This bit controls the active low CHIP_RESET (the hardware reset)of the FM2220.
1	SW_CPU_RST_n	This bit controls the active low CPU_RST_n pin of the FM2220. This pin is used to reset the CPU interface of the switch.
2	SW_AUTOBOOT	This bit controls the AUTOBOOT pin of the FM2220. When the bit is set to '1', the BOOT FSM starts automatically. After RESET it is de-asserted, the chip is initialized according to the content of the fuse box; control is returned to the CPU Interface after the initialization is completed. When the bit is set to '0' booting is down via processor.
3	SW_EEPROM_EN	This bit controls the EEPROM_EN pin of the FM2220. Set to '0' to bypass the EEPROM and boot via processor.
4	SW_CONT_EN	This bit controls the CONT_EN pin of the FM2220. Enables the SerDes continuity test; for debug purpose only.
[7..5]	-	Reserved Write as '0' and ignore when read.

5.7 Reserved

This register is reserved.

Table 15: RSVD Register

Reserved - Address 0x6								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	

5.8 SPI Multiplexer Control

This register controls a SPI multiplexer.

Table 16: SPI_MUX_CTL Register

SPI Multiplexer Control - Address 0x7								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-		SPI_MUX_CTL

Table 17: SPI_MUX_CTL - Register Bits

Bit	Name	Function
0	SPI_MUX_CTL	This bit controls the SPI multiplexer '0' =EEPROM and switch are connected; SPI from **BASE-Module** and SPI to parallel interface are connected (CPU interface of FM2220) '1' = SPI from BASE**-Module** and EEPROM are connected.
[7..1]	-	Reserved Write as '0' and ignore when read.

6 Board Specification

Table 18: NAT-MCH HUB-Module XAUI – Features

Power Consumption	29W max. (only **NAT-MCH HUB-Module XAUI x48**)
Voltage Range	8V – 14V
Operating Temperature	-5°C – +55°C with forced cooling
Storage Temperature	-40°C - +70°C
Humidity	5% – 95% rh non-condensing
Standards compliance	PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.2 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification v2.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH HUB-Module XAUI** during its usual life-time take refer to the safety note section of the **NAT-MCH BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements

7.2.1 Requirements

The installation requires a **NAT-MCH BASE-Module** and a **CLK-Module** where the **HUB-Module XAUI** can be mechanically fixed on to. The **HUB-Module XAUI** must be completely connected and joint to the complete PCB stack (**BASE-Module** and **CLK-Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH HUB-Module XAUI** must meet the following specifications:

- The power supply must be able to supply 29W (only **HUB-Module XAUI x48**, in addition to other PCBs of the **NAT-MCH**), in a voltage range from 8V to 14V.

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

- With the Hardware Version v1.0 it is not possible to use any face plate module.

Appendix A: Reference Documentation

[1] Fulcrum Microchip, FM2224 "Focal Point" FM2224, Datasheet, FM2224-DS-2.3, 06.2008
[2] Fulcrum Microchip, FM2220 "Focal Point" FM2220, Datasheet Addendum, FM2220-DSA-1.3, 09.2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	15.08.2008	initial revision	ks
1.1	19.05.2013	Address, phone and fax updated, words updated	fh
1.2	14.11.2013	Adaption to new layout, typo correction	Se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	se