NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.5
HUB-Module SRIO HW Revision 2.2

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SRIO	Serial Rapid IO
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Introduction

The **NAT-MCH** consists of a **BASE-Module**, which can be expanded with additional PCBs. The **BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB Modules** are available. With the **CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

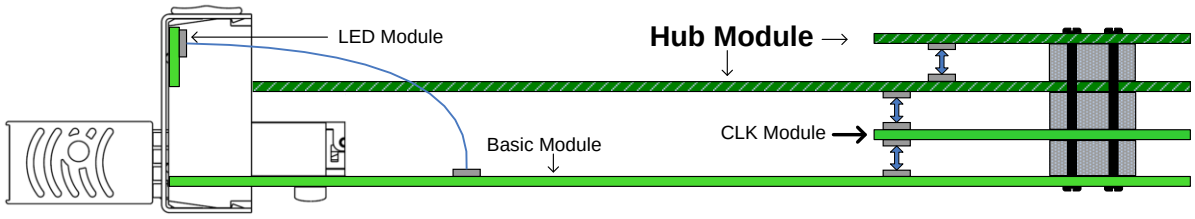
Through the extension of the **NAT-MCH** with a **HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in the following figure.

Figure 1: **Arrangement of different NAT-MCH Modules**



This Technical Reference Manual describes the **NAT-MCH HUB-Module SRIO**. In addition to the **CLK-Module** it can be mounted on the **NAT-MCH BASE-Module**. The **HUB-Module SRIO** is in a 6 Slot ("**x24**") and in a 12 slot ("**x48**") option available. With the **HUB-Module SRIO** the 3rd tongue of the **NAT-MCH** connector to the MicroTCA backplane is always installed. With the **x48** option, additional the 4th tongue is installed. The **NAT-MCH HUB-Module SRIO** implements the following major features:

- support of SRIO x4 switching function for fabrics D to G of up to 6 AMCs (**HUB-Module SRIO x24)**
- support of SRIO x4 switching function for fabrics D to G of up to 12 AMCs (**HUB-Module SRIO x48)**

- support of up to two SRIO x4 face plate uplinks and/or a SRIO x4 fabric update to the second MCH (**Uplink Option**)

The **HUB-Module SRIO** contains out of two IDT CPS-1848 SRIO switches. The first SRIO switch connects to AMC 1-6. This switch is subsequent referred as 1st switch or 1st CPS-1848. The second SRIO switch connects to AMC 7-12. This switch is subsequent referred as 2nd switch or 2nd CPS-1848.

2 Overview

2.1 Major Features

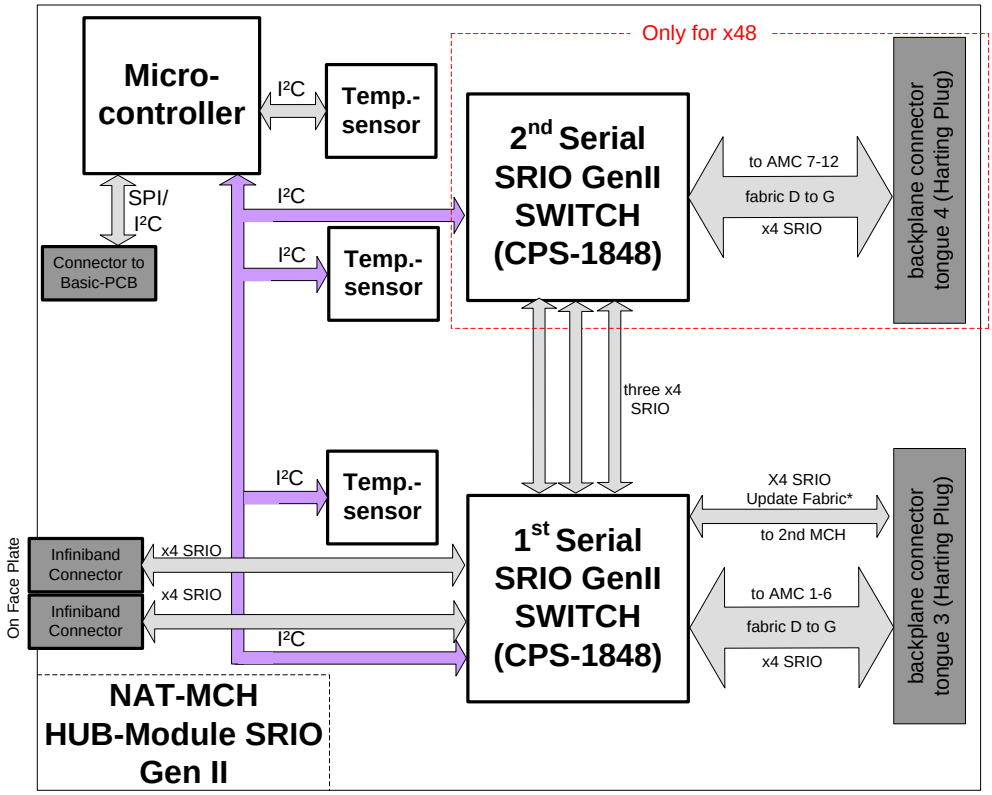
- Configurable x1 or x4 SRIO interfaces to 12 AMC modules
- backplane update fabric to second MCH
- operation baud rate per data lane 1.25 Gbit/s, 2.5 Gbit/s, 3.125 Gbit/s, 5Gbit/s or 6.25Gbit/s1*
- two optional face plate uplinks
- transport layer error management
- low latency packet transport
- configuration interface via onboard microcontroller
- 3 onboard temperature sensors

[1] Because of a chip bug 6.25Gbaud is not supported. Please refer to chapter "known bugs and restrictions" for a more detailed description

2.2 Block Diagram

The following figure shows a block diagram of the **NAT-MCH HUB-Module SRIO** and optional available extension modules.

Figure 2: **NAT-MCH HUB-Module SRIO – Block Diagram**



** Only the Update Fabrics for fabric D and E are connected via the tongue 3 backplane connector. The Update Fabrics for fabric F and G are connected via the tongue 4 backplane connector. To simplify the diagram this is not shown.*

2.3 Location Diagram

The following figures show the position of important components of the **NAT-MCH HUB-Module SRIO.**

Figure 3: **NAT-MCH HUB-Module SRIO – Location diagram (top)**

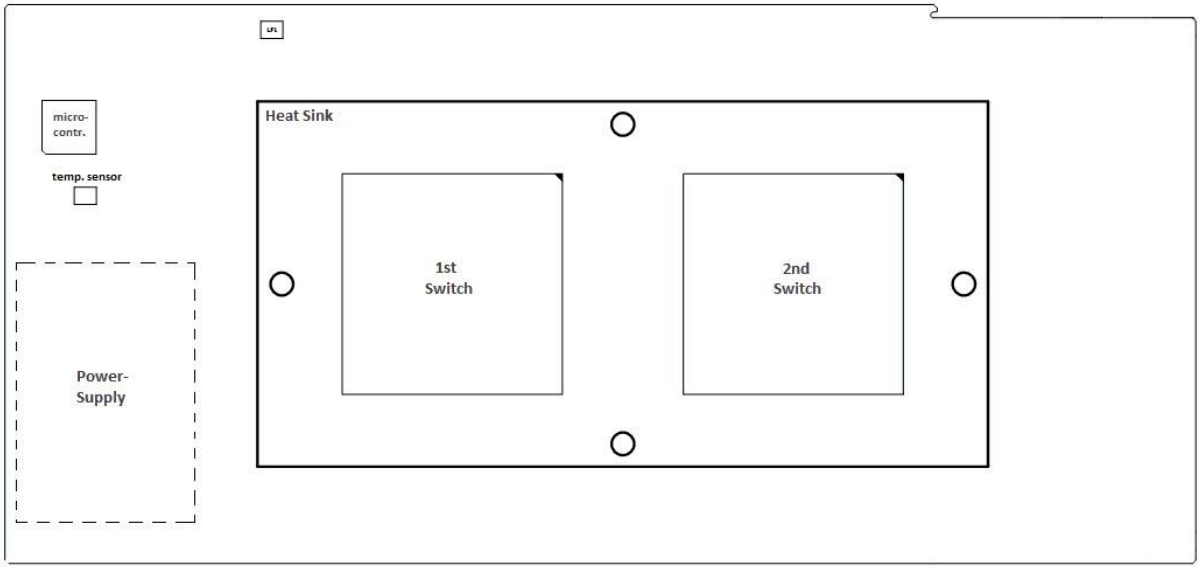
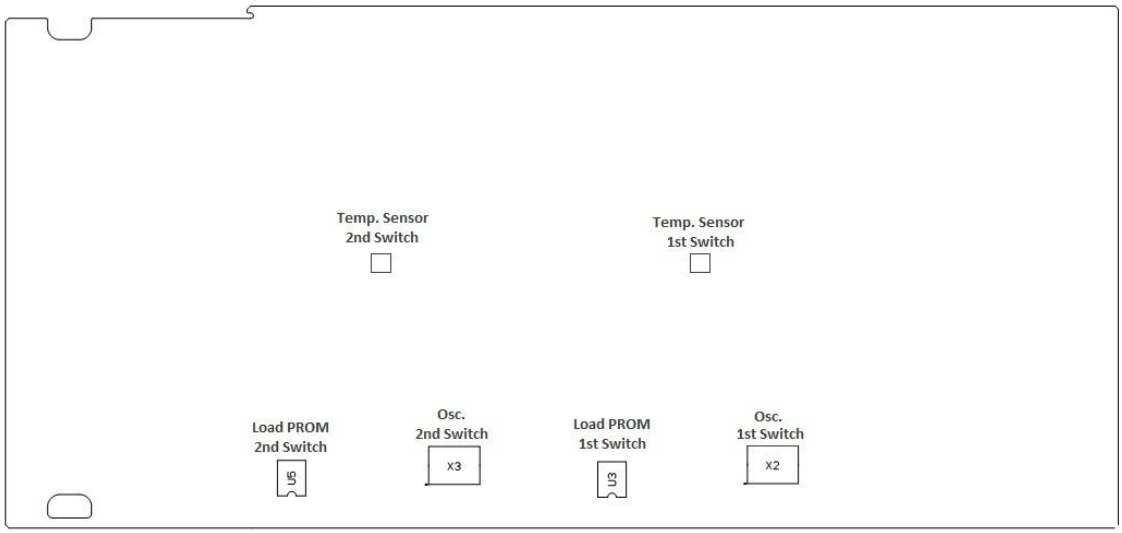


Figure 4: **NAT-MCH HUB-Module SRIO – Location diagram (bottom)**



3 Functional Blocks

The **NAT-MCH HUB-Module SRIO** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 SRIO Switches

The board is equipped with two IDT CPS-1848 Serial Rapid IO switches, which provide non-blocking high performance data switching functionality. Data integrity and health checks are performed by hardware. The CPS-1848 offers 12.5 Gbit/s bandwidth per port (x4) combined with a low latency packet transport. Additional a flexible port width (x1 or x4) and different operating baud rates (1.25Gbit/s, 2.5Gbit/s and 3.125Gbit/s) can be selected.

Each of the twoCPS-1848 SRIO Switches supports 6 ports, each with 4 lanes (SRIO x4), in order to connect 6 AMCs. Three ports with 4 lanes are used to connect the two Switches. The first switch supports also a 4-lane port to connect to a second MCH via the backplane update fabrics D-G. Furthermore two four lane ports of the first switch are used to supports the optional face plate uplinks.

Both CPS-1848 can be configured by strapping pins, by loading an EEPROM, or by accessing the TSI register interface via I²C from the microcontroller. A standard configuration is done by the microprocessor and resistors, by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.
These standard settings can be changed by reading the EEPROM after a reset, or by changing the values of the TSI register interface with the help of the microcontroller (via I²C interface).
The intended way of standard configuration is that the microcontroller performs the basic setup via strapping. By default the EEPROM contains basic settings that need to be done to configure the device regarding the board and system requirements. The MCH firmware is then able to initialize (or terminate) each port to the needed speed and port width.

The first port of the switch is <u>not</u> connected to the first port of fabric D-G, and so on. To ease routing of the differential fabrics between the switches and the backplane connectors the following allocation has been selected.

Table 2: 1st Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	# Port - 1st CPS-1848
AMC1	9
AMC2	1
AMC3	4
AMC4	11
AMC5	3
AMC6	6
MCH Update (backplane connection to 2nd MCH)	5
1st switch interconnect: connection to port # 2 of the 2nd CPS-1848	0
2nd switch interconnection: connection to port # 10 of the 2nd CPS-1848	7
3rd switch interconnection: connection to port # 5 of the 2nd CPS-1848	8
Face plate uplink 1	2
Face plate uplink 2	10

Table 3: 2nd Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	#Port - 2nd CPS-1848
AMC7	1
AMC8	8
AMC9	0
AMC10	7
AMC11	11
AMC12	6
1st switch interconnect: connection to port # 0 of the 1st CPS-1848	2
2nd switch interconnection: connection to port # 7 of the 1st CPS-1848	10
3rd switch interconnection: connection to port # 8 of the 1st CPS-1848	5

Under some conditions it might be more useful to have the ports mapping sorted by the switch ports. Therefore the following table shows again the switch port mapping sorted by the switch ports.

Table 4: Switch Port Mapping

Port #	Assignment – Switch 1	Assignment – Switch 2
0	1st switch interconnect	AMC9
1	AMC2	AMC7
2	Uplink1	1st switch interconnect
3	AMC5	-
4	AMC3	-
5	MCH update	3rd switch interconnect
6	AMC6	AMC12
7	2nd switch interconnect	AMC10
8	3rd switch interconnect	AMC8
9	AMC1	-
10	Uplink2	2nd switch interconnect
11	AMC4	AMC11

All previous ports mapping are considering a 1-to-1 connecting backplane. In case a NATIVE-R5 or NATIVE-C5 chassis is used the following port mapping have to be considered due to the backplane topology of these chassis.

Table 5: Switch Port Mapping NATIVE-R5 or NATIVE-C5

	# AMC Slot Fabric D-G	
SRIO ports	**1-To-1 Connecting Backplane**	**NATIVE-C5 NATIVE-R5**
# Port - 1st CPS-1848		
9	AMC1	AMC2
1	AMC2	AMC3
4	AMC3	AMC4
11	AMC4	AMC5
3	AMC5	AMC6
6	AMC6	AMC7
#Port - 2nd CPS-1848		
1	AMC7	AMC1
8	AMC8	n/a
0	AMC9	n/a
7	AMC10	n/a
11	AMC11	n/a
6	AMC12	n/a

3.2 Microcontroller

An 8-bit Atmel microcontroller resides on the **NAT-MCH HUB-Module SRIO**. The microcontroller can be updated by the CPU on the **BASE-Module** via the SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages via the I²C interface.

The strapping options and the reset signal of the switches can be controlled through programming registers in the microcontroller.
Furthermore each switch is connected to a separate I²C bus. Via these buses the microcontroller has access to the register interface of the switches.

Also three temperature sensors are connected to the I²C bus that connects the 1st Switch. The microcontroller makes these sensors and the register interfaces of the switches accessible to the CPU on the **BASE-Module** via IPMI.

3.3 Interfaces

The **NAT-MCH HUB-Module SRIO** implements interfaces to connect fabrics D to G of up to 12 AMCs. It also supports the Update Fabric D to G to the second MCH.
As an additional option the **NAT-MCH Hub Module SRIO** supports up to two x4 SRIO uplinks on the face plate (see chapter 3.4 for details).

3.4 Uplink Option

With the uplink option it is possible to connect to the SRIO fabric up to two face plate connectors. This is an assembly option and therefore need to be chosen when ordered.
If the uplink option is assembled the baud rate of each uplink connection can be configured. The following options are available:

- 1.25Gbit/s
- 2.5 Gbit/s
- 3.125 Gbit/s
- 5 Gbit/s
- 6.25 Gbit/s[2]
- disabled (default setting)

The individual modes can configured within the **NAT-MCH** configuration settings (SRIO setting). For a more detailed description of the MCH configuration please refer to the **NAT-MCH User's manual**.

[2] Because of a chip bug 6.25Gbaud is not supported. Please refer to chapter "known bugs and restrictions" for a more detailed description

4 Hardware

4.1 Connectors

Figure 5: **NAT-MCH HUB-Module SRIO – Connectors (top)**

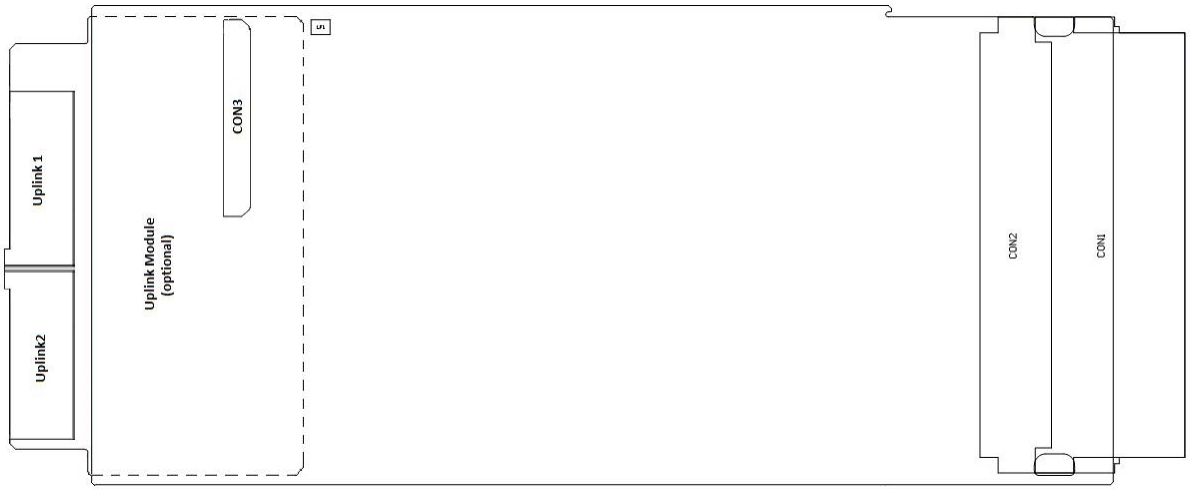
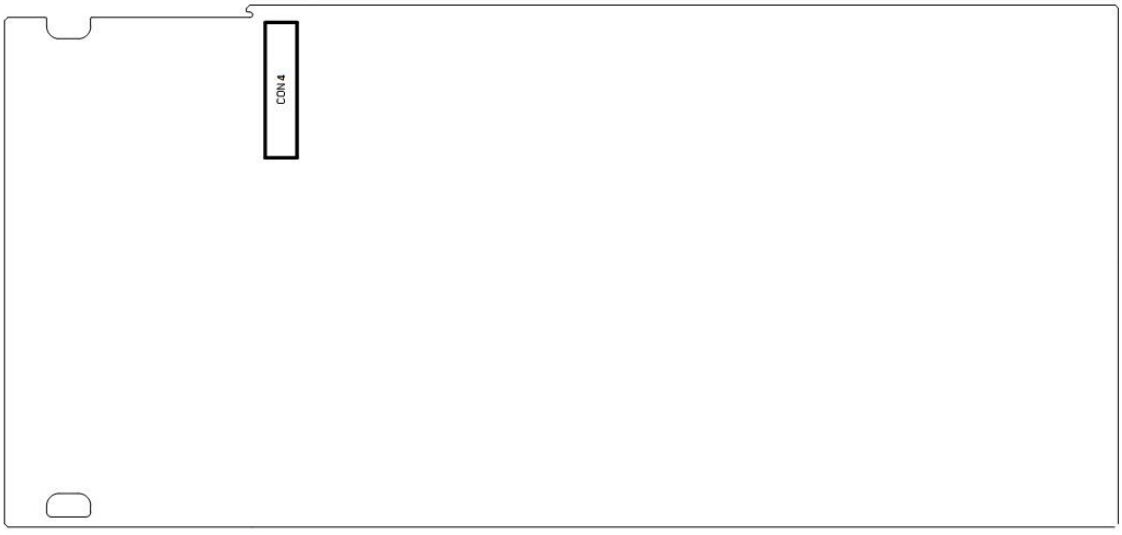


Figure 6: **NAT-MCH HUB-Module SRIO – Connectors of the (bottom)**



Please refer to the following tables to look up the pin assignment of the **NAT-MCH HUB-Module SRIO**.

4.1.1 CON1: HUB-Module SRIO Backplane Connector

Table 6: CON1: HUB-Module SRIO Backplane Connector - Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUD+	RxFUD+	163
9	TxFUD-	RxFUD-	162
10	GND	GND	161
11	TxFUE+	RxFUE+	160
12	TxFUE-	RxFUE-	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

4.1.2 CON2: HUB-Module x48 Extender Connector

Table 7: CON2: HUB-Module x48 Extender Backplane Connector – Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUF+	RxFUD+	163
9	TxFUF-	RxFUD-	162
10	GND	GND	161
11	TxFUG+	RxFUE+	160
12	TxFUG-	RxFUE-	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

4.1.3 CON3: CLK-Module Connector

Table 8: CON3: CLK-Module Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	INT1	INT2	2
3	GND	GND	4
5	N.C.	N.C.	6
7	N.C.	N.C.	8
9	+12V	+12V	10
11	+12V	+12V	12
13	N.C.	+3.3V_MP	14
15	N.C.	SPICLK	16
17	GND	N.C.	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	N.C.	24
25	SDA	nRESET_HUB_PCB	26
27	GND	GND	28

This connector connects to the **CLK-Module**. On the **CLK-Module** the signals of this connector are passed through to a connector that connects to the **BASE-Module**.

4.1.4 CON4: Uplink-Module Connector

Table 9: CON4: Uplink-Module Connector – Pin Assignment

Pin No#	Signal	Signal	Pin #
1	GND	GND	2
3	+1.2V	+1.2V	4
5	+1.2V	+1.2V	6
7	GND	GND	8
9	FP_CON5	UP_LNK_SCL	10
11	FP_CON6	UP_LNK_SDA	12
13	GND	GND	14
15	FP_CON 7	FP_CON3	16
17	FP_CON8	FP_CON 4	18
19	GND	GND	20
21	FP_CON9	FP_CON11	22
23	FP_CON10	FP_CON12	24
25	GND	GND	26
27	UP_LINK1_TD_N	UP_LINK1_RA_P	28
29	UP_LINK1_TD_P	UP_LINK1_RA_N	30
31	GND	GND	32
33	UP_LINK1_TC_N	UP_LINK1_RB_P	34
35	UP_LINK1_TC_P	UP_LINK1_RB_N	36
37	GND	GND	38
39	UP_LINK1_TB_N	UP_LINK1_RC_P	40
41	UP_LINK1_TB_P	UP_LINK1_RC_N	42
43	GND	GND	44
45	UP_LINK1_TA_N	UP_LINK1_RD_P	46
47	UP_LINK1_TA_P	UP_LINK1_RD_N	48
49	GND	GND	50
51	UP_LINK2_TD_N	UP_LINK2_RA_P	52
53	UP_LINK2_TD_P	UP_LINK2_RA_N	54
55	GND	GND	56
57	UP_LINK2_TC_N	UP_LINK2_RB_P	58
59	UP_LINK2_TC_P	UP_LINK2_RB_N	60
61	GND	GND	62
63	UP_LINK2_TB_N	UP_LINK2_RC_P	64
65	UP_LINK2_TB_P	UP_LINK2_RC_N	66
67	GND	GND	68
69	UP_LINK2_TA_N	UP_LINK2_RD_P	70
71	UP_LINK2_TA_P	UP_LINK2_RD_N	72
73	GND	GND	74
75	+3.3V	+3.3V	76
77	+3.3V	+3.3V	78
79	GND	GND	80

4.1.5 Uplink1: 1st Face Plate Interface

Table 10: Uplink1: 1st Face Plate Interface – Pin Assignment

Pin #	Signal	Signal	Pin #
1	UP_LINK1_RA_P	UP_LINK1_TA_P	16
2	UP_LINK1_RA_N	UP_LINK1_TA_N	15
3	UP_LINK1_RA_P	UP_LINK1_TA_P	14
4	UP_LINK1_RA_N	UP_LINK1_TA_N	13
5	UP_LINK1_RA_P	UP_LINK1_TA_P	12
6	UP_LINK1_RA_N	UP_LINK1_TA_N	11
7	UP_LINK1_RA_P	UP_LINK1_TA_P	10
8	UP_LINK1_RA_N	UP_LINK1_TA_N	9
G1	GND	GND	G5
G2	GND	GND	G6
G3	GND	GND	G7
G4	GND	GND	G8

4.1.6 Uplink2: 2nd Face Plate Interface

Table 11: Uplink2: 2nd Face Plate Interface – Pin Assignment

Pin #	Signal	Signal	Pin #
1	UP_LINK2_RA_P	UP_LINK2_TA_P	16
2	UP_LINK2_RA_N	UP_LINK2_TA_N	15
3	UP_LINK2_RA_P	UP_LINK2_TA_P	14
4	UP_LINK2_RA_N	UP_LINK2_TA_N	13
5	UP_LINK2_RA_P	UP_LINK2_TA_P	12
6	UP_LINK2_RA_N	UP_LINK2_TA_N	11
7	UP_LINK2_RA_P	UP_LINK2_TA_P	10
8	UP_LINK2_RA_N	UP_LINK2_TA_N	9
G1	GND	GND	G5
G2	GND	GND	G6
G3	GND	GND	G7
G4	GND	GND	G8

5 Programming Notes

5.1 SPI Interface

The SPI interface on the **HUB-Module SRIO** is only used for maintenance purposes, e.g. updating the microcontroller firmware.

5.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **NAT-MCH BASE-Module**. All communication is based on IPMI Messages.

5.3 Register

A register interface is implemented in the Atmel microcontroller. With the help of this interface different functions can be controlled and various identification values can be read.

5.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH HUB-Module SRIO**.

Table 12: Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xb8								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	BOARD_ID							

5.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH HUB-Module SRIO**.

Table 13: PCB_REV Register

PCB Revision - Address 0x01								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB_REV							

Bit 7 to 4 contain the major revision and bit 3 to 0 contain the minor revision. That means if the PCB revision is e.g. v2.0 the PCB Revision register contains the value 0x20.

5.3.3 Firmware Version

The Firmware Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH HUB-Module SRIO**.

Table 14: FW_VERSION Register

Firmware Version – Address 0x02								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	Atmel_vers							

Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the Firmware running on the Atmel is v1.3 the Firmware Version register contains the value 0x13.

5.3.4 Hub Module SRIO Type

The Hub Module SRIO Type Register contains the information if the **HUB-Module SRIO** is a type x24 or x48.

Table 15: SRIO_TYPE Register

Hub Module SRIO Type - Address 0x03								
Default value 0x24/48								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	SRIO_Mod_Typ							

5.3.5 Miscellaneous Control Register

The miscellaneous control Register contains the value of the various strapping and reset pins of both CPS-1848 switches.

Table 16: MISC_CTL Register

Miscellaneous Control - Address 0x10								
Default value 0xA3								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Func	**SW2_ MCAST**	**SW1_ MCAST**	**SW_SPD[0..2]**			**SW_IRQ_N**	**SW2_RST_N**	**SW1_RST_N**

Table 17: MISC_CTL - Register Bits

Bit	Name	Function
0	SW1_RST_N	This bit controls the RST_N pin of the first CPS-1848. Writing a "0" into this bit resets the whole CPS-1848.
1	SW2_RST_N	This bit controls the RST_N pin of the second CPS-1848. Writing a "0" into this bit resets the whole CPS-1848.
2	SW_IRQ_N	This bit shows the OR'ed state of the IRQ_N pin of both CPS-1848 switches.
[5..3]	SW_SPD[0..2]	These bits control the SPD pins of both CPS-1848 switches. They select the default serial port frequency of all ports of both CPS-1848 switches. 000 = 1.25 Gbit/s 100 = 2.5 Gbit/s 101 = 3.125 Gbit/s x10 = 5.0 Gbit/s x11 = 6.25 Gbit/s[3] 001 = Reserved
6	SW1_MCAST	This bit controls the MCAST pin of the first CPS-1848.
6	SW2_MCAST	This bit controls the MCAST pin of the first CPS-1848.

[3] Because of a chip bug 6.25Gbaud is not supported. Please refer to chapter "known bugs and restrictions" for a more detailed description

6 Board Specification

Table 18: NAT-MCH HUB-Module SRIO Features

Power Consumption	12V / 1.5A max. (only **NAT-MCH HUB-Module SRIO x48**)
Operating Temperature	0°C – +50°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	Rapid IO Interconnect Specification Rev. 1.3 PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.4 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification v2.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH HUB-Module SRIO** during its usual life-time take refer to the safety note section of the **NAT-MCH BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements

7.2.1 Requirements

The installation requires a **NAT-MCH BASE-Module** and a **CLK-Module** where the **HUB-Module SRIO** can be mechanically fixed on to. The **HUB-Module SRIO** must be completely connected and joint to the complete PCB stack (**BASE-Module** and **CLK-Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH HUB-Module SRIO** must meet the following specifications:

- +12 V / 1.5 A max. (only **HUB-Module SRIO x48**, in addition to other PCBs of the **NAT-MCH**).

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

- The lanes of port 0,7 and 8 (AMC8, 9 and 10) are swapped. Automatic lane swapping is part of the SRIO spec. 2.1. Boards with SRIO "GenII" devices will perform automatic lane swapping. Boards that are only compliant to older SRIO specifications will not perform automatic lane swapping! **This restriction applies only to hardware version 2.0 boards!**
- Uplink ports are only working reliable with a speed of up to 3.125Gbaud/s.
- The used SRIO switch (VPS/CPS1848) has a bug that may show up when ports are configured to 6.25Gbaud. If that bug shows up the related port will result in an unreliable Link establishment. Because of that bug it is not recommended to run any port with 6.25Gbaud. Therefore the latest MCH firmware will no longer support that speed. 6.25Gbaud/s can be used for Lab testing. Please contact N.A.T. for a description how to enable that 6.25Gbaud.

Appendix A: Reference Documentation

[1] IDT, CPS-1848 User Manual, 02.2011
[2] IDT, CPS-1848 Datasheet, 02.2011

Appendix B: Document's History

Revision	Date	Description	Author
1.0	07.04.2011	initial revision	Ks
1.1	03.05.2011 29.09.2011	Corrected table "2nd Switch to Fabric Port Mapping" on page 18. Added restriction that 6.25Gbaud cannot be used, whole document	Ks Ks
1.2	19.05.2013	Address, phone and fax updated, words updated	fh
1.3	24.09.2013 14.11.2013	Adaption to new layout Typo correction Update pin assignment connector 4	Se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	se
1.4	23.04.2015	Update document to latest WEEE directive	ks
1.5	08.1.2016	Update chapter 3.1SRIO Switches with Table 5: Switch Port Mapping NATIVE-R5 or NATIVE-C5	hn