NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.2
Hub Module SRIO HW Revision 1.3/1.4

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SRIO	Serial Rapid IO
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Board Specification

NAT-MCH Hub Module SRIO Features

Power Consumption	12V / 1.2A max. (only Hub Module SRIO x48)	
Environmental Conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards Compliance	Rapid IO Interconnect Specification Rev. 1.3	
	PICMG µTCA.0 Rev. 1.0	
	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.4 Rev. 1.0	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	IPMI Specification v2.0 Rev. 1.0	
Product Safety	The board complies with EN60950 and UL1950	

NAT-MCH Hub Module SRIO Technical Features

- configurable x1 or x4 SRIO interfaces to 12 AMC modules
- operation baud rate per data lane 1.25 Gbit/s, 2.5 Gbit/s or 3.125 Gbit/s
- Optional face plate uplinks or backplane update fabric
- Transport layer error management
- low latency packet transport
- configuration interface via on board microcontroller
- 3 onboard temperature sensors

2 Statement on Environmental Protection

2.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

3 Installation

3.1 Safety Note

To ensure proper functioning of the **NAT-MCH Hub Module SRIO** during its usual lifetime take refer to the safety note section of the **NAT-MCH BASIC-Module** Technical Reference Manual before handling the board.

3.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up check this section for installation prerequisites and requirements

3.2.1 Requirements

The installation requires a **NAT-MCH Basic-Module** and a **CLK Module** where the **Hub Module SRIO** can be mechanically fixed on to. The **Hub Module SRIO** must be completely connected and joint to the complete PCB stack (**Basic-Module** and **CLK Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASIC-Module** Technical Reference Manual.

3.2.2 Power supply

The power supply for the **NAT-MCH Hub Module SRIO** must meet the following specifications:

+12 V / 1.2 A max. (only **Hub Module SRIO x48**, in addition to other PCBs of the **NAT-MCH**).

3.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH Basic-Module**

In the following situations the **NAT-MCH Basic-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

4 Introduction

The **NAT-MCH** consists of a **Basic-Module**, which can be expanded with additional PCBs. The **Basic-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **Basic-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB Modules** are available. With the **Clock-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

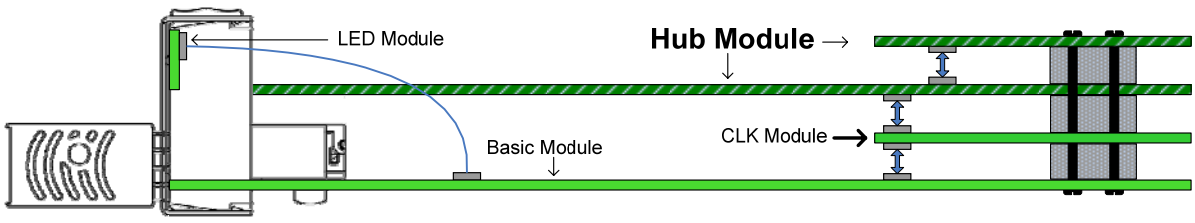
Through the extension of the **NAT-MCH** with a **HUB Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in *Figure 1*.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **Hub Module SRIO**.

5 Hub Module SRIO Basics

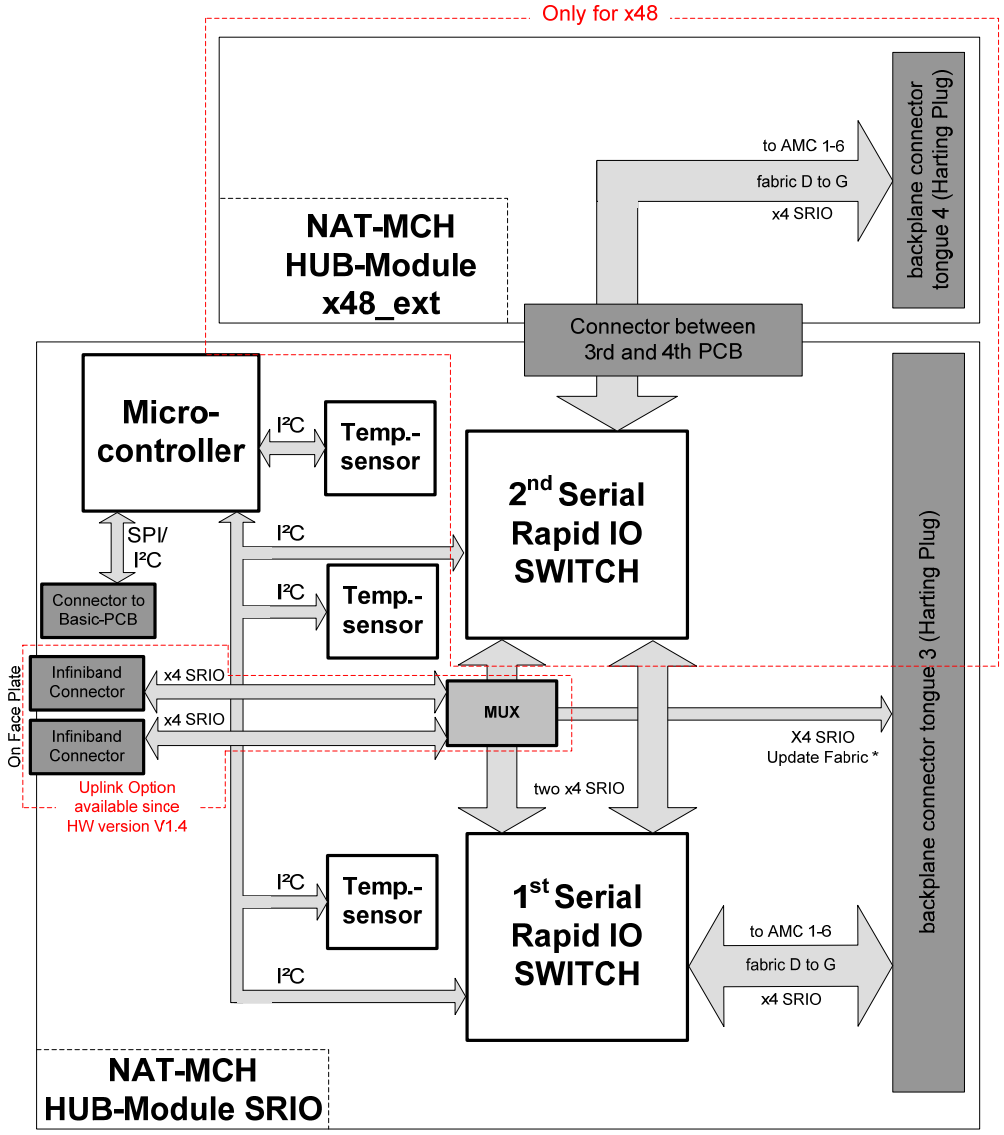
The **Hub Module SRIO** is an expansion Module of the **NAT-MCH**. In addition to the **CLK Module** it can be mounted on the **NAT-MCH Basic-Module**. The **Hub Module SRIO** is in a 6 Slot ("**x24**") and in a 12 slot ("**x48**") option available. With the **Hub Module SRIO** the 3rd tongue of the **NAT-MCH** connector to the MicroTCA backplane is always installed. With the **x48** option, additional the 4th tongue is installed. The **NAT-MCH Hub Module SRIO** implements the following major features:

- support of SRIO x4 switching function for fabrics D to G of up to 6 AMCs (**Hub Module SRIO x24)**
- support of SRIO x4 switching function for fabrics D to G of up to 12 AMCs (**Hub Module SRIO x48)**
- support of up to two SRIO x4 face plate uplinks and/or a SRIO x4 fabric update to the second MCH (**Uplink Option**)

The **Hub Module SRIO** contains out of two Tundra TSI578 SRIO switches. The first SRIO switch connects to AMC 1-6. This switch is subsequent referred as 1st switch or 1st TSI578. The second SRIO switch connects to AMC 7-12. This switch is subsequent referred as 2nd switch or 2nd TSI578.

6 Hub Module SRIO Block Diagram

Figure 2: Block Diagram of the NAT-MCH Hub Module SRIO



** Only the Update Fabrics for fabric D and E are connected via the tongue 3 backplane connector. The Update Fabrics for fabric F and G are connected via the tongue 4 backplane connector. To simplify the diagram this is not shown.*

- The HUB-PCB x48_ext and the 2nd SRIO switch are only assembled in the x48 version.
- MUX1 and MUX2 with the optional faceplate Uplinks or Update Fabrics are first implemented in hardware version v1.4.
- refer to chapter 9.2 for a more detailed description of the MUX function

7 BOARD FEATURES

- **SRIO Switch**

  The board is equipped with two Tundra TSI578 Serial Rapid IO switches, which provide non-blocking high performance data switching functionality. Data integrity and health checks are performed by hardware. The TSI578 offers 12.5 Gbit/s bandwidth per port (x4) combined with a low latency packet transport. Additional a flexible port width (x1 or x4) and different operating baud rates (1.25Gbit/s, 2.5Gbit/s and 3.125Gbit/s) can be selected.

- **Microprocessor**

  To configure the two switches the board is equipped with an Atmel 8-bit microcontroller.

- **Interfaces**

  - The **NAT-MCH Hub Module SRIO** implements interfaces to connect fabrics D to G of up to 12 AMCs.
  - As an additional option the **NAT-MCH Hub Module SRIO** supports up to two x4 SRIO uplinks on the face plate. Or it supports an Update Fabric to the second MCH and only one front plate uplinks. (*first available since HW v1.4*)

- **Interface to other NAT-MCH PCBs**

  Basic-Module: - The Microcontroller on the **Hub Module SRIO** can be updated by the CPU on the **Basic-Module** via a SPI interface. Normal communication between the Microprocessor and the CPU is done by IPMI messages via the I²C interface.

8 Location Overview

Figure 3 and Figure 4 are showing the position of important components of the **NAT-MCH Hub Module SRIO** hardware version v1.3.

Figure 3: Location diagram of the NAT-MCH Hub Module SRIO v1.3 (top-view)

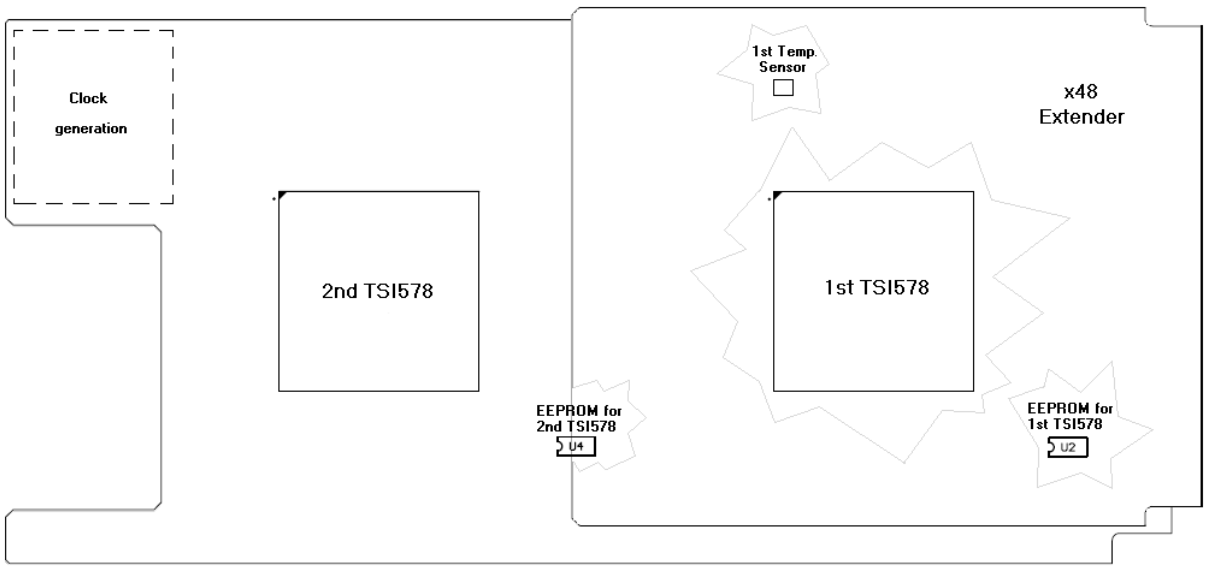


Figure 4: Location diagram of the NAT-MCH Hub Module SRIO v1.3 (bottom-view)

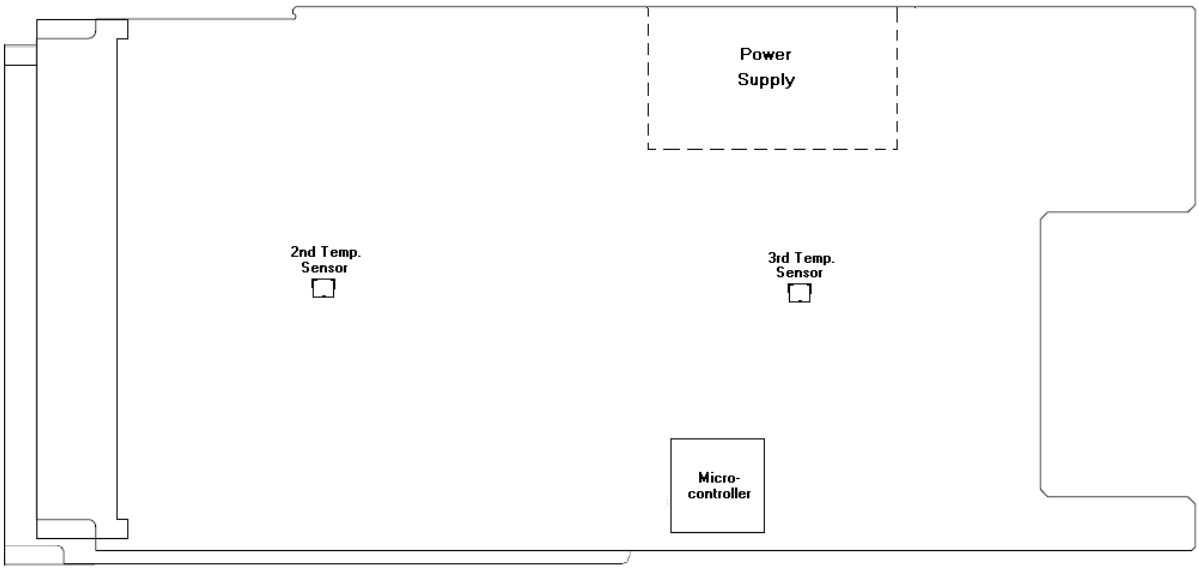


Figure 5 and Figure 6 are showing the position of important components of the **NAT-MCH Hub Module SRIO** hardware version v1.4.

Figure 5: Location diagram of the NAT-MCH Hub Module SRIO v1.4 (top-view)

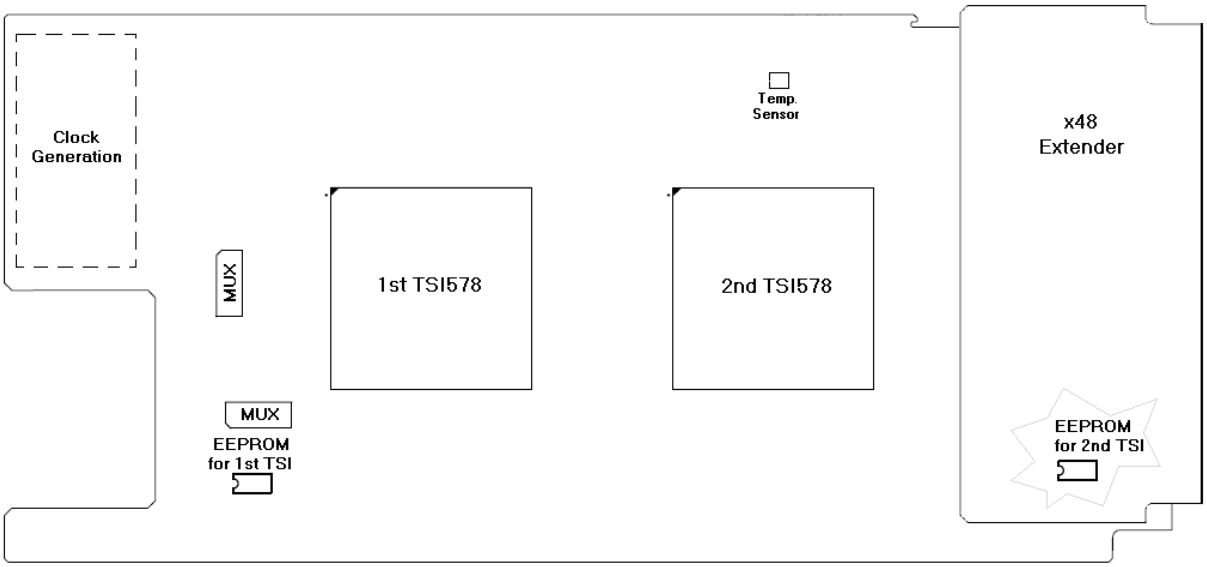
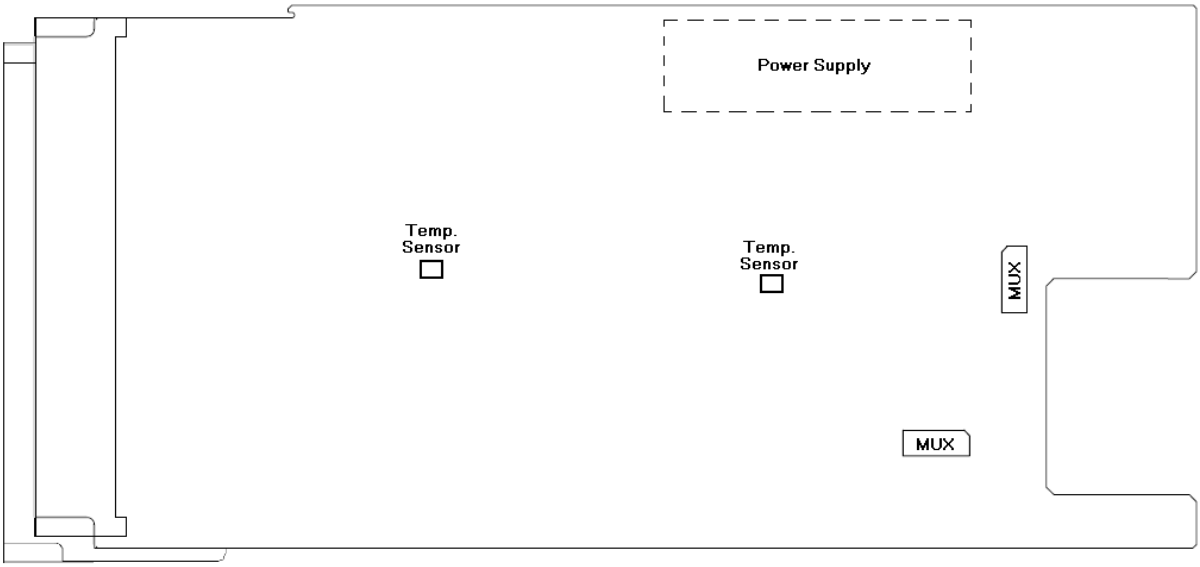


Figure 6: Location diagram of the NAT-MCH Hub Module SRIO v1.4 (bottom-view)



9 Functional Blocks

The **NAT-MCH Hub Module SRIO** is divided into a number of functional blocks, which are described in the following paragraphs.

9.1 SRIO Switches

Each of the twoTSI578 SRIO Switches supports 6 ports, each with 4 lanes (SRIO x4), in order to connect 6 AMCs. Two ports with 4 lanes are used to connect the two Switches. One of these two connections can optionally be used to connect to different Uplink options (refer to …)

Both TSI578 can be configured by strapping pins, by loading an EEPROM, or by accessing the TSI register interface via I²C from the microcontroller.

A standard configuration is done by the microprocessor and resistors, by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.

These standard settings can be changed by reading the EEPROM after a reset, or by changing the values of the TSI register interface with the help of the microcontroller (via I²C interface).

By default the EEPROM contains no information.

The first port of the switch is <u>not</u> connected to the first port of fabric D-G, and so on. To ease routing of the differential fabrics between the switches and the backplane connectors the following allocation has been selected:

1st Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	**#Port 1st TSI578**
AMC1	14
AMC2	6
AMC3	12
AMC4	4
AMC5	10
AMC6	2
connection to port # 0 of the 2nd TSI578	0
connection to port # 8 of the 2nd TSI578 or to FP Uplink1 or to Fabric Update, depending on Uplink Option	8

2nd Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	#Port 2nd TSI578
AMC7	14
AMC8	6
AMC9	12
AMC10	4
AMC11	10
AMC12	2
connection to port # 0 of the 1st PEX8532	0
connection to port # 8 of the 1st PEX8532 or to FP Uplink2, depending on Uplink Option	8

9.2 Uplink Option

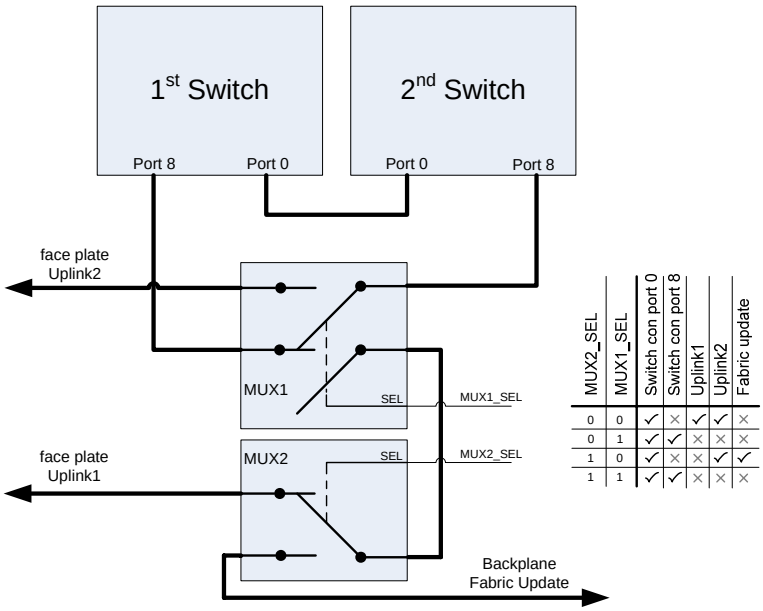
With the uplink option it is possible to connect to the SRIO fabric via up to two face plate connectors or through a fabric update channel that connects to a second MCH.

The Uplink option can be configured in various modes of operation:

Mode 0:	No uplink channels used, the preserved X4 link is used as additional interconnect between the two SRIO chips (default setting). This mode is compatible with previous releases of the SRIO hub module (V1.3 and V1.2).
Mode 1:	Dual Uplink mode – one X4 link of each SRIO chip is routed to the faceplate connectors.
Mode 2:	Mixed Uplink / Backplane Update function. One X4 link is routed to one face plate connector, the other X4 link is routed to the fat pipe update channel in the backplane.

The individual modes can configured within the MCH configuration settings (SRIO setting) and are realized by additional multiplexers. Figure 7 gives a detailed overview, how the uplink option is realized and how the multiplexers are connected.

Figure 7: Detailed Block Diagram of Uplink Option



9.3 Microcontroller

An 8-bit Atmel microcontroller resides on the **Hub Module SRIO**. The microcontroller can be updated by the CPU on the **Base-Module** via the SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages over the I²C interface.

The strapping options and the reset signal of the switches can be controlled through programming registers in the microcontroller.

Furthermore each switch is connected to a separate I²C bus. Via these busses the microcontroller has access to the register interface of the switches.

Also three temperature sensors are connected to the I²C bus that connects the 1st Switch.

The microcontroller makes these sensors and the register interfaces of the switches accessible to the CPU on the **Base-Module** via IPMI.

10 NAT-MCH Hub Module SRIO Programming Notes

10.1 SPI Interface

The SPI interface on the **Hub Module SRIO** is only used for maintenance purposes, e.g. updating the microcontroller firmware.

10.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the Basic-Module. All communication is based on IPMI Messages.

10.3 Register

A register interface is implemented in the Atmel microcontroller. With the help of this interface different functions can be controlled and various identification values can be red.

10.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH Hub Module SRIO**.

Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xb8								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	BOARD_ID							

10.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH Hub Module SRIO**.

PCB_REV Register

PCB Revision - Address 0x01								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB_REV							

Bit 7 to 4 contains the major revision and bit 3 to 0 contains the minor revision. That means if the PCB revision is e.g. v1.3 the PCB Revision register contains the value 0x13.

10.3.3 Firmware Version

The Firmware Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH Hub Module SRIO**.

FW_VERSION Register

Firmware Version – Address 0x02								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	Atmel_vers							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the Firmware running on the Atmel is v1.3 the Firmware Version register contains the value 0x13.

10.3.4 Hub Module SRIO Type

The Hub Module SRIO Type Register contains the information if the **Hub Module SRIO** is a type x24 or x48.

SRIO_TYPE Register

Hub Module SRIO Type - Address 0x03								
Default value 0x24/48								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	SRIO_Mod_Typ							

10.3.5 SRIO Uplink Option

The SRIO Uplink Option Register controls which Uplink Option the **Hub Module SRIO** supports.

SRIO_UPLINK_OPT Register

SRIO Uplink Option - Address 0x04								
Default value 0x03								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-						**MUX2_SEL**	**MUX1_SEL**

SRIO_UPLINK_OPT - Register Bits

Bit	Name	Function
0	MUX1_SEL	This bit controls the switch position of the first Multiplexer. This bit controls together with the MUX1_SEL bit which Uplink Option is supported.
1	MUX2_SEL	This bit controls the switch position of the second Multiplexer. This bit controls together with the MUX1_SEL bit which Uplink Option is supported.
[7..2]	-]	**no function** write as 0 and ignore when read

MUX2_SEL	MUX1_SEL	Switch con port 0	Switch con port 8	Uplink1	Uplink2	Fabric update
0	0	✓	×	✓	✓	×
0	1	✓	✓	×	×	×
1	0	✓	×	×	✓	✓
1	1	✓	✓	×	×	×

10.3.6 Miscellaneous Control Register

The miscellaneous control Register the value of the various strapping and reset pins of the both TSI578.

MISC_CTL Register

Miscellaneous Control - Address 0x10								
Default value 0xA3								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**TSI2_IO_SPEED[1..0]**		**TSI1_IO_SPEED[1..0]**		**TCSI2_I2C_ DISABLE**	**TCSI1_I2C_ DISABLE**	**TSI2_HARD_ RST**	**TSI1_HARD_ RST**

MISC_CTL - Register Bits

Bit	Name	Function
0	TSI1_HARD_ RST	This bit controls the HARD_RST_b pin of the first TSI578 Writing a “0” into this bit resets the whole TSI578
1	TSI2_HARD_ RST	This bit controls the HARD_RST_b pin of the second TSI578 Writing a “0” into this bit resets the whole TSI578
2	TSI1_I2C_ DISABLE	This bit controls the I2C_DISABLE pin of the first TSI78 When this bit is set the TSI578 will not attempt register values from the I2C Bus.
3	TSI2_I2C_ DISABLE	This bit controls the I2C_DISABLE pin of the second TSI578 Refer to “TSI1_I2C_DISABLE” for functional description.
[5..4]	TSI1_IO_ SPEED[1..0]	These bits control the SP_IO_SPEED pins of the first TSI578 These bits select the default serial port frequency of all ports of the dedicated TSI578. 00 = 1.25 Gbit/s 01 = 2.5 Gbit/s 10 = 3.125 Gbit/s 11 = illegal
[7..6]	TSI2_IO_ SPEED[1..0]	These bits control the SP_IO_SPEED pins of the first TSI578 Refer to “TSI1_IO_SPEED” for functional description.

10.3.7 TSI1 Mode Select Register

The TSI1 Mode Select Register controls the MODESEL pins of the first TSI578.

TSI1_MODESEL Register

TSI1 Mode Select - Address 0x11								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**TSI1_SP14_ MODESEL**	**TSI1_SP12_ MODESEL**	**TSI1_SP10_ MODESEL**	**TSI1_SP8_ MODESEL**	**TSI1_SP6_ MODESEL**	**TSI1_SP4_ MODESEL**	**TSI1_SP2_ MODESEL**	**TSI1_SP0_ MODESEL**

TSI1_MODESEL - Register Bits

Bit	Name	Function
0	TSI1_SP0 MODESEL	This bit controls the SP0_MODESEL pin of the first TSI578 This bit selects the serial port operating mode. 0 = Port n operates in x4 mode (port n + 1 is not available). 1 = Port n and n + 1 are operating in x1 mode.
1	TSI1_SP2 MODESEL	This bit controls the SP2_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
2	TSI1_SP4 MODESEL	This bit controls the SP4_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
3	TSI1_SP6 MODESEL	This bit controls the SP6_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
4	TSI1_SP8 MODESEL	This bit controls the SP8_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
5	TSI1_SP10 MODESEL	This bit controls the SP10_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
6	TSI1_SP12 MODESEL	This bit controls the SP12_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.
7	TSI1_SP14 MODESEL	This bit controls the SP14_MODESEL pin of the first TSI578 Refer to “TSI1_SP0_MODESEL” for functional description.

10.3.8 TSI2 Mode Select Register

The TSI2 Mode Select Register controls the MODESEL pins of the second TSI578.

TSI2_MODESEL Register

TSI2 Mode Select - Address 0x12								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**TSI2_SP14_ MODESEL**	**TSI2_SP12_ MODESEL**	**TSI2_SP10_ MODESEL**	**TSI2_SP8_ MODESEL**	**TSI2_SP6_ MODESEL**	**TSI2_SP4_ MODESEL**	**TSI2_SP2_ MODESEL**	**TSI2_SP0_ MODESEL**

TSI2_MODESEL - Register Bits

Bit	Name	Function
0	TSI2_SP0 MODESEL	This bit controls the SP0_MODESEL pin of the first TSI578 This bit selects the serial port operating mode. 0 = Port n operates in x4 mode (port n + 1 is not available). 1 = Port n and n + 1 are operating in x1 mode.
1	TSI2_SP2 MODESEL	This bit controls the SP2_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
2	TSI2_SP4 MODESEL	This bit controls the SP4_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
3	TSI2_SP6 MODESEL	This bit controls the SP6_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
4	TSI2_SP8 MODESEL	This bit controls the SP8_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
5	TSI2_SP10 MODESEL	This bit controls the SP10_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
6	TSI2_SP12 MODESEL	This bit controls the SP12_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.
7	TSI2_SP14 MODESEL	This bit controls the SP14_MODESEL pin of the first TSI578 Refer to “TSI2_SP0_MODESEL” for functional description.

10.3.9 PLL Control Register

The PLL Control Register controls the PLL that generates the reference clock for both TSI578.

PLL_CTL Register

PLL Control - Address 0x13								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	**PLL_RST**

TSI2_MODESEL - Register Bits

Bit	Name	Function
0	PLL_RST	Setting this bit holds the PLL in reset.
[7..1]	-	**no function** write as 0 and ignore when read

11 Connectors

11.1 Connector Overview

Figure 1: Connectors of the NAT-MCH Hub Module SRIO (top view)

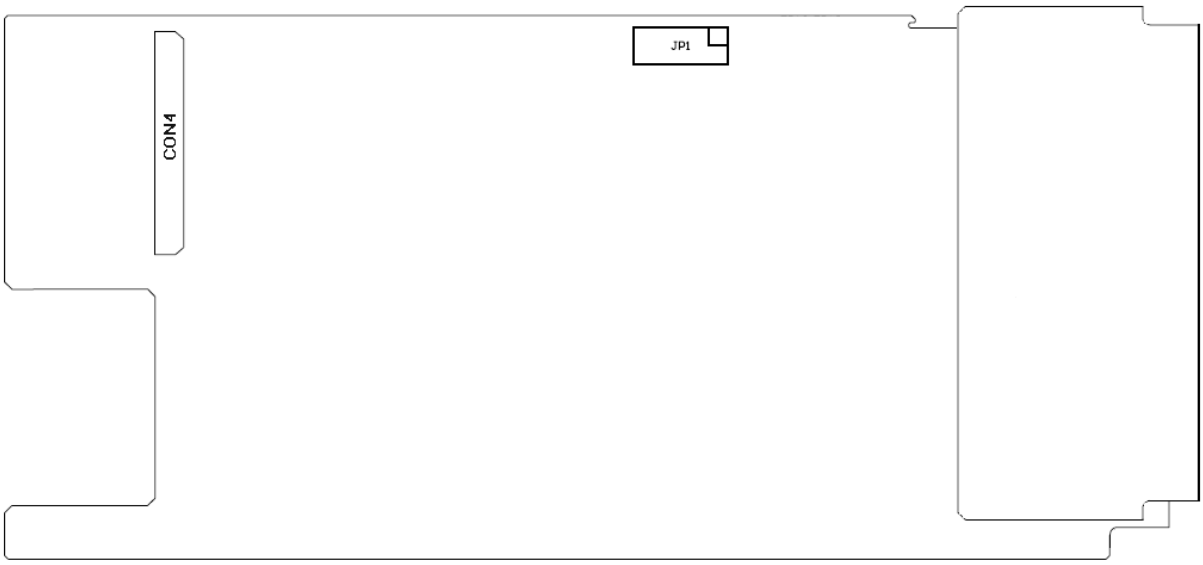
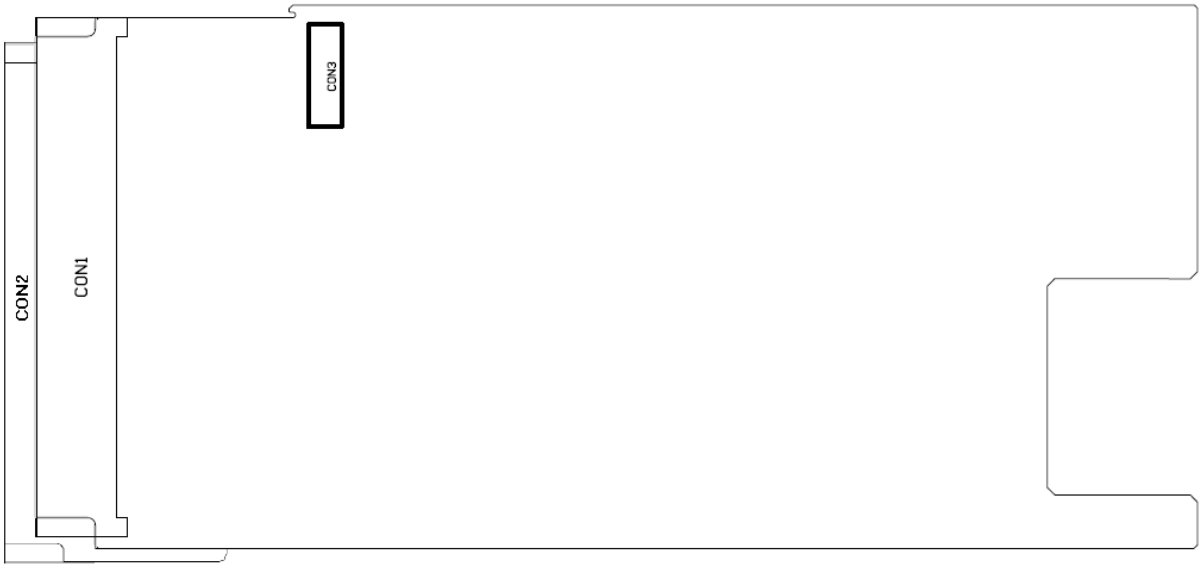


Figure 2: Connectors of the NAT-MCH Hub Module SRIO (bottom view)



Please refer to the following tables to look up the pin assignment of the **NAT-MCH Hub Module SRIO**.

11.2 NAT-MCH Hub Module SRIO Connector CON1

Hub Module SRIO backplane connector CON1

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUD+	RxFUD+	163
9	TxFUD-	RxFUD-	162
10	GND	GND	161
11	TxFUE+	RxFUE+	160
12	TxFUE-	RxFUE-	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

11.3 NAT-MCH Hub Module x48 Extender Connector CON2

Hub Module x48 Extender backplane connector CON2

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUF+	RxFUD+	163
9	TxFUF-	RxFUD-	162
10	GND	GND	161
11	TxFUG+	RxFUE+	160
12	TxFUG-	RxFUE-	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140

Pin No.	MCH-Signal	MCH-Signal	Pin No.
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92

Pin No.	MCH-Signal	MCH-Signal	Pin No.
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

11.4 Connector CON3: Interface to CLK-Module

Connector to CLK-Module CON3

Pin No.	Signal	Signal	Pin No.
1	+12V	+12V	2
3	+12V	+12V	4
5	SRIOCLK_P	+3.3V_MP	6
7	SRIOCLK_N	SPICLK	8
9	GND	expansion3	10
11	MOSI	MISO	12
13	GND	/SPISEL_HUBPCB	14
15	SCL	N.C.	16
17	SDA	nRESET_HUB_PCB	18
19	GND	GND	20

This connector connects to the **CLK-Module**. On the **CLK-Module** the signals of this connector are routed to a connector that connects to the **Basic-Module**.

11.5 Connector CON4: Interface to Uplink Module

Connector to Uplink Module CON4

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	2
3	+1.2V	+1.2V	4
5	+1.2V	+1.2V	6
7	GND	GND	8
9	FP_CON5	FP_CON1	10
11	FP_CON6	FP_CON2	12
13	GND	GND	14

Pin No.	MCH-Signal	MCH-Signal	Pin No.
15	FP_CON 7	FP_CON3	16
17	FP_CON8	FP_CON 4	18
19	GND	GND	20
21	FP_CON9	FP_CON11	22
23	FP_CON10	FP_CON12	24
25	GND	GND	26
27	UP_LINK1_TD_N	UP_LINK1_RD_P	28
29	UP_LINK1_TD_P	UP_LINK1_RD_N	30
31	GND	GND	32
33	UP_LINK1_TC_N	UP_LINK1_RC_P	34
35	UP_LINK1_TC_P	UP_LINK1_RC_N	36
37	GND	GND	38
39	UP_LINK1_TB_N	UP_LINK1_RB_P	40
41	UP_LINK1_TB_P	UP_LINK1_RB_N	42
43	GND	GND	44
45	UP_LINK1_TA_N	UP_LINK1_RA_P	46
47	UP_LINK1_TA_P	UP_LINK1_RA_N	48
49	GND	GND	50
51	UP_LINK2_TD_N	UP_LINK2_RD_P	52
53	UP_LINK2_TD_P	UP_LINK2_RD_N	54
55	GND	GND	56
57	UP_LINK2_TC_N	UP_LINK2_RC_P	58
59	UP_LINK2_TC_P	UP_LINK2_RC_N	60
61	GND	GND	62
63	UP_LINK2_TB_N	UP_LINK2_RB_P	64
65	UP_LINK2_TB_P	UP_LINK2_RB_N	66
67	GND	GND	68
69	UP_LINK2_TA_N	UP_LINK2_RA_P	70
71	UP_LINK2_TA_P	UP_LINK2_RA_N	72
73	GND	GND	74
75	+3.3V	+3.3V	76
77	+3.3V	+3.3V	78
79	GND	GND	80

* This connector does not exist in hardware v1.3 or earlier versions.

11.6 Connector JP1: JTAG interface to the TSI578 Chips

JTAG Connector JP1

Pin No.	Signal	Signal	Pin No.
1	+3.3V	GND	2
3	TCK	TMS	4
5	TDI	TDO	6
7	BCE	nTSI1_TRST	8
9	N.C.	nTSI2_TRST	10

12 Known Bugs / Restrictions

Appendix A: Reference Documentation

[1] Tundra, TSI578 Serial Rapid IO Switch, Hardware Manual, 80B80A_MA002_07, 09.2007

[2] Tundra, TSI578 Serial Rapid IO Switch, User Manual, 80B80A_MA001_06, 09.2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	13.03.2008	initial revision	Ks
1.1	17.03.2008	Changes for hardware revision v1.3 - Figure 2 and 3 (location diagram) - Tables showing switch to fabric port mapping - Figure 4 and 5 showing connectors - deleted known bugs	Ks
1.2	22.01.2009	Added description for hardware revision 1.4 and description of Uplink option	Ks