NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.0
Hub Module PCIe HW Revision 1.4

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

Table of Contents

List of Figures

List of Tables

Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Board Specification

Table 2: NAT-MCH Hub Module PCIe Features

Power Consumption	12V / 1.6A max. (only Hub Module PCIe x48)	
Environmental Conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards Compliance	PCI Express Base Specification Rev. 1.1	
	PICMG µTCA.0 Rev. 1.0	
	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 1.0	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	IPMI Specification v2.0 Rev. 1.0	
Product Safety	The board complies with EN60950 and UL1950	

Table 3: NAT-MCH Hub Module PCIe Technical Key Features

- support for 6 (option ”x24”) or 12 (option “x48”)
- non-blocking switch fabric
- built of two PLX5832 PCIe switches
- high performance x8 interconnect between chips to prevent performance bottleneck
- upstream port (and NT-upstream port) configurable to any of the 12 AMC slots
- PCIe hot plug support for each AMC slot
- clustering support, two clusters of 6 AMC modules each can be operated individually each having its on root complex
- support x1 and x4 width ports to any AMC
- PCIe compliant spread spectrum clocking

2 Statement on Environmental Protection

2.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

3 Installation

3.1 Safety Note

To ensure proper functioning of the **NAT-MCH Hub Module PCIe** during its usual lifetime take refer to the safety note section of the **NAT-MCH BASIC-Module** Technical Reference Manual before handling the board.

3.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up check this section for installation prerequisites and requirements

3.2.1 Requirements

The installation requires a **NAT-MCH Basic-Module** and a **CLK Module** where the **Hub Module PCIe** can be mechanically fixed on to. The **Hub Module PCIe** must be completely connected and joint to the complete PCB stack (**Basic-Module** and **CLK Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASIC-Module** Technical Reference Manual.

3.2.2 Power supply

The power supply for the **NAT-MCH Hub Module PCIe** must meet the following specifications:

+12 V / 1.6 A max. (only **Hub Module PCIe x48**, in addition to other PCBs of the **NAT-MCH**).

3.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH Basic-Module**

In the following situations the **NAT-MCH Basic-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

4 Introduction

The **NAT-MCH** consists of a **Basic-Module**, which can be expanded with additional PCBs. The **Basic-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **Basic-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB Modules** are available. With the **Clock-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

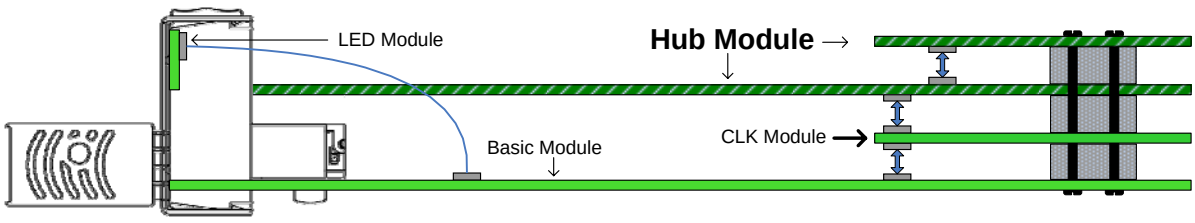
Through the extension of the **NAT-MCH** with a **HUB Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in *Figure 1*.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **Hub Module PCIe**.

5 Hub Module PCIe Basics

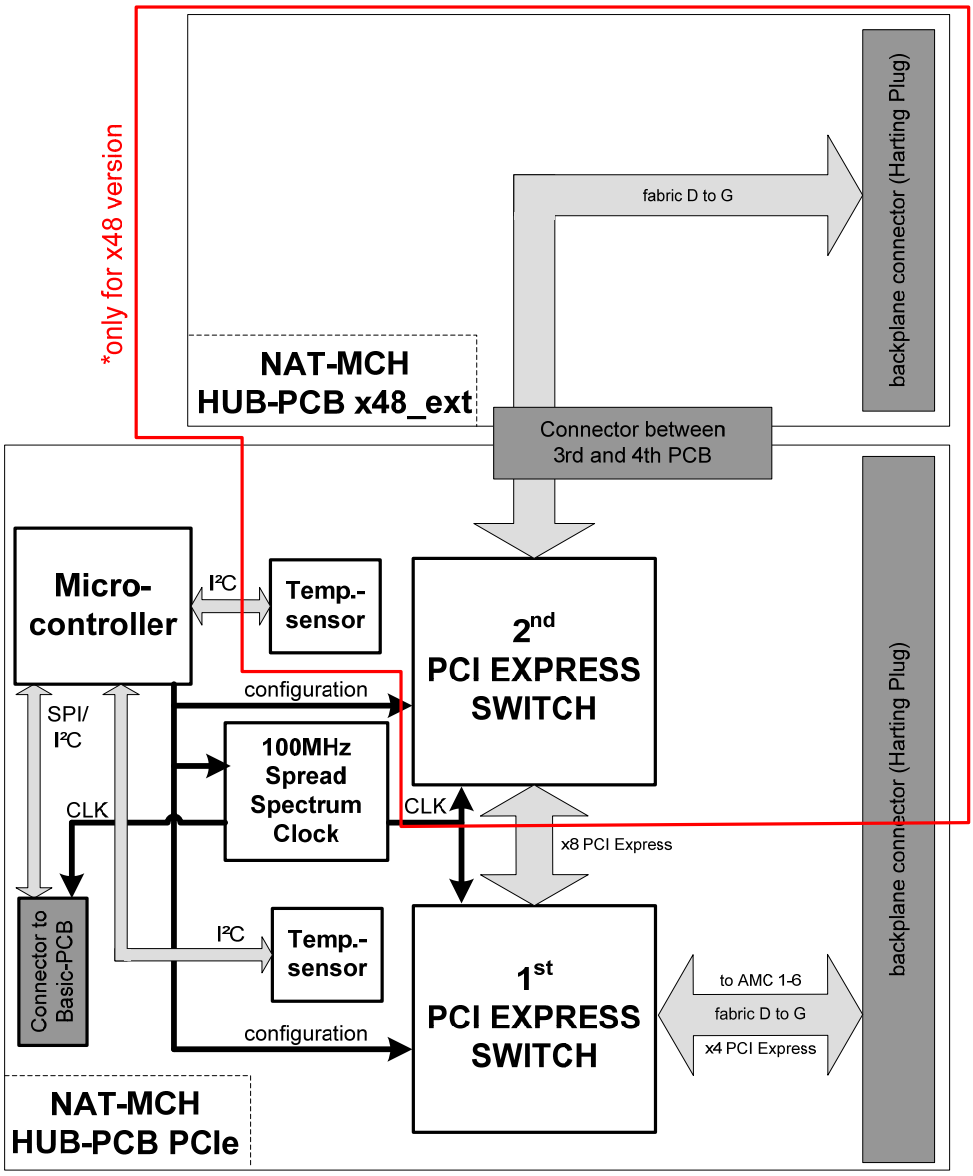
The **Hub Module PCIe** is an expansion Module of the **NAT-MCH**. In addition to the **CLK Module** it can be mounted on the **NAT-MCH Basic-Module**. The **Hub Module PCIe** is in a 6 Slot (**x24**) and in a 12 slot (**x48**) option available. With the **Hub Module PCIe** the 3rd tongue of the **NAT-MCH** connector to the MicroTCA backplane is always installed. With the **x48** option, additional the 4th tongue is installed. The **NAT-MCH Hub Module PCIe** implements the following major features:

- support of PCI Express x4 switching function for fabrics D to G of up to 6 AMCs (**Hub Module PCIe x24)**
- support of PCI Express x4 switching function for fabrics D to G of up to 12 AMCs (**Hub Module PCIe x48)**
- support of spread spectrum clocking (distribution of the SSC signal is done by the **CLK Module**)

The **Hub Module PCIe** contains out of two PLX 8532 PCIe switches. The first PCIe switch connects to AMC 1-6. This Switch is subsequent referred as 1st Switch or 1st PEX8532. The second PCIe switch connects to AMC 7-12. This switch is subsequent referred as 2nd switch or 2nd PEX8532.

6 Hub Module PCIe Block Diagram

Figure 1: Block Diagram of the NAT-MCH Hub Module PCIe



* The HUB-PCB x48_ext and the 2nd PCIe switch are only assembled in the x48 version.

7 BOARD FEATURES

- **PCI Express Switch**

  The board is equipped with PLX PEX8532 PCI Express switches, which provide non-blocking switching at full line rate. Quality of Service (QoS) is provided by the PEX8532, supporting 2 virtual cannels and 8 traffic classes per port. One of all ports can be configured as transparent upstream port, and one of all ports can be configured as non-transparent upstream port.

- **Spread Spectrum Clock**

  The board is equipped with an ICS9FG104, which generates reference clock for the two switches.

- **Microprocessor**

  To configure the two switches and the SSC the board is equipped with an Atmel 8-bit microcontroller.

- **Interfaces**

  The **NAT-MCH Hub Module PCIe** implements interfaces to connect fabrics D to G of up to 12 AMCs.

- **Interface to other NAT-MCH PCBs**

  Basic-Module:
  - The Microcontroller on the **Hub Module PCIe** can be updated by the CPU on the **Basic-Module** via a SPI interface. Normal communication between the Microprocessor and the CPU is done by IPMI messages via the I²C interface.
  - For each of the PCIe switches a configuration EEPROM resides on the **Hub Module PCIe**. These two EEPROMs can be programmed / updated by the CPU on the **Basic-Module** via the SPI interface.

  CLK-Module:
  - The **Hub Module PCIe** can provide the 100 MHz PCI Express compliant clock signal to the **CLK-Module**.

8 Location Overview

Figure 2: "Location diagram of the **NAT-MCH Hub Module PCIe**" shows the position of important components.

Figure 2: Location diagram of the NAT-MCH Hub Module PCIe (top-view)

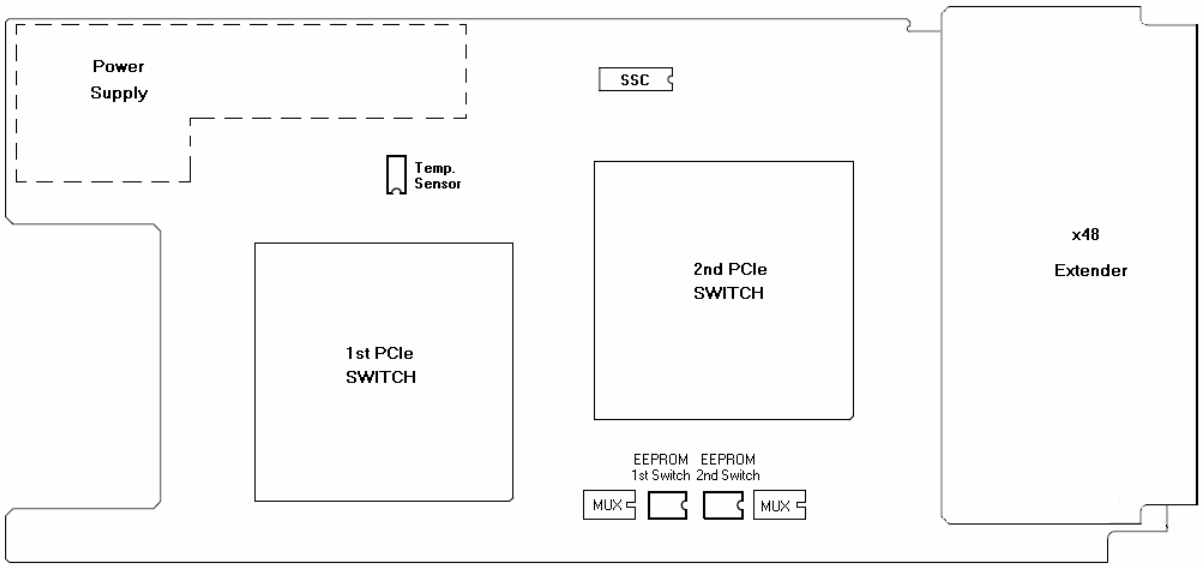
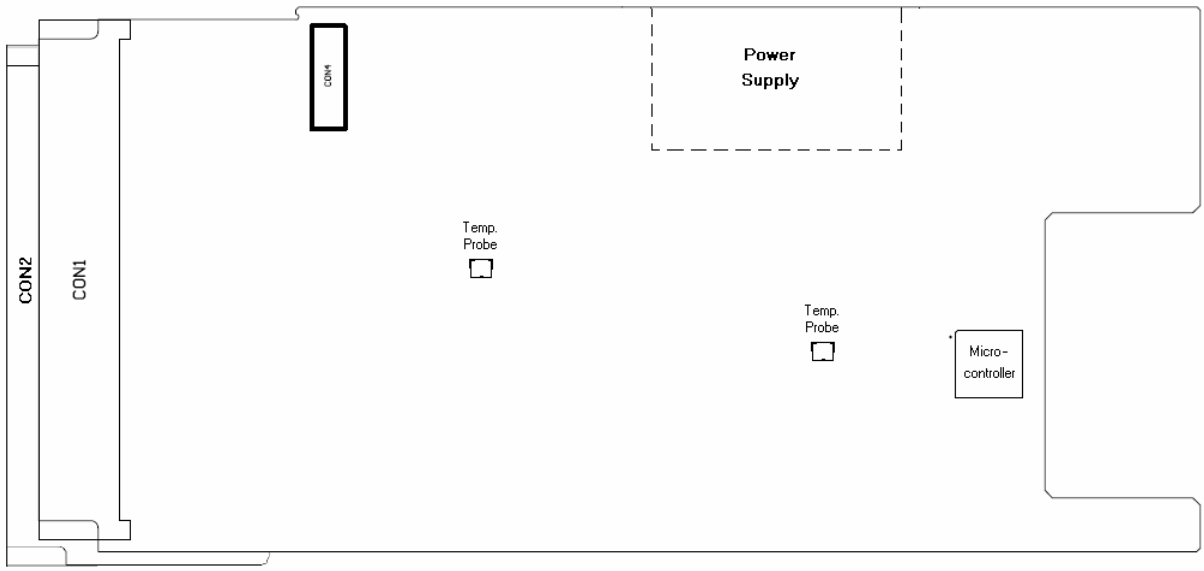


Figure 3: Location diagram of the NAT-MCH Hub Module PCIe (bottom-view)



9 Functional Blocks

The **NAT-MCH Hub Module PCIe** is divided into a number of functional blocks, which are described in the following paragraphs.

9.1 PCI Express Switches

Each of the two PEX8532 PCI Express Switches supports 6 ports, each with 4 lanes (PCIe x4), in order to connect 6 AMCs. One port with 8 lanes is used to connect the two Switches.

Both PEX8532 can be configured by strapping pins, by loading an EEPROM, or by PCI Express messages from a host. A standard configuration is done by the microprocessor and resistors by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.

These standard settings can be changed by reading the EEPROM after a reset, or by receiving PCI Express messages from a host.

The EEPROM contains basic configuration information for the PCIe switch as well as user settings, e.g. upstream port settings. The user settings can be changed by the CPU on the **Basic-Module** via the SPI interface.

The /PERST pin is also connected to the microcontroller. The value of this pin can also be controlled by programming a register in the microcontroller.

The first port of the switch is <u>not</u> connected to the first port of fabric D-G, and so on. To ease routing of the differential fabrics between the switches and the backplane connectors the following allocation has been selected: Connection to 2nd PEX8532

Table 4: 1st Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	#Port 1st PEX8532
AMC1	2
AMC2	1
AMC3	8
AMC4	9
AMC5	10
AMC6	11
connection to 2nd PEX8532	0
Not used	3

Table 5: 2nd Switch to Fabric Port Mapping

# AMC Slot Fabric D-G	#Port 2nd PEX8532
AMC7	2
AMC8	1
AMC9	8
AMC10	9
AMC11	10
AMC12	11
Connection to 1st PEX8532	0
Not used	3

9.2 Spread Spectrum Clock

An ICS9FG104 clocking device generates a PCI Express compliant clock signal with a frequency of 100 MHz fixed or spread spectrum (0.5% down spread). The ICS9FG104 feeds the PEX8532 with this clock signal. Additional the **CLK Module** can be sourced by the ICS9FG104 over CON4.

9.3 Microcontroller

An 8-bit Atmel microcontroller resides on the **Hub Module PCIe**. The microcontroller can be updated by the CPU on the **Base-Module** via the SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages over the I²C interface.

The strapping options and the reset signal of the switches can be controlled through programming registers in the microcontroller. Also the spread spectrum function of the ICF9FG104 can be controlled over these register.

Furthermore, three temperature sensors are connected to a second I²C bus of the Microcontroller. The microcontroller makes these sensors accessible to the CPU on the **Base-Module** via IPMI.

10 NAT-MCH Hub Module PCIe Programming Notes

10.1 SPI Interface

The SPI interface can be multiplexed between three devices on the **Hub Module PCIe**. Default the SPI interface is connected to the Microcontroller. In this it is only used for maintenance purposes, e.g. updating the microcontroller firmware.
Or the SPI Bus can be connected to one of the two configuration EEPROMs that reside on the Hub Module PCIe. In this case the SPI interface is used to read or write data on the EEPROM.

10.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the Basic-Module. All communication is based on IPMI Messages.

10.3 Register

A register interface is implemented in the Atmel microcontroller. With the help of this interface different functions can be controlled and various identification values can be red.

10.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH Hub Module PCIe**.

Table 6: Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xb7								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	BOARD_ID							

10.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH Hub Module PCIe**.

Table 7: PCB Revision Register

PCB Revision - Address 0x01								
Default value 0x14								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB_REV							

10.3.3 Atmel Version

The Atmel Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH Hub Module PCIe**.

Table 8: PCB Revision Register

Atmel Version - Address 0x02								
Default value 0x12								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	Atmel_vers							

10.3.4 Hub Module PCIe Typ

The Hub Module PCIe Typ Register contains the information if the **Hub Module PCIe** is a type x24 or x48.

Table 9: PCB Revision Register

Hub Module PCIe Typ - Address 0x03								
Default value 0x24/48								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCIe_Mod_Typ							

10.3.5 Hot Plug Present 1 Register

The Hot Plug Present Register 1 register controls together with the Hot Plug Present 2 Register the value of the /HP_PRSNT balls of the corresponding PEX8532.

Table 10: HP_PRSNT1 Register

Hot Plug Present1 - Address 0x12								
Default value 0xff								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	HP_PRSNT(8:1)							

Table 11: HP_PRSNT1 - Register Bits

Bit	Name	Function
[7..0]	HP_PRSNT (8:1)	These bits have to be cleared by the Coldfire if an AMC is recognized on the corresponding AMC slot. These bits have to be set if the corresponding AMC slot is empty. HP_PRSNT1 is assigned to AMC1 and HP_PRSNT8 to AMC8

10.3.6 Hot Plug Present 2 Register

The Hot Plug Present Register 2 Register controls together with the Hot Plug Present 1 Register the value of the /HP_PRSNT balls of the corresponding PEX8532.

Table 12: HP_PRSNT2 Register

Hot Plug Present 2 – Address 0x13								
Default value 0xff								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func					HP_PRSNT[12:9]			

Table 13: HP_PRSNT2 - Register Bits

Bit	Name	Function
[3..0]	HP_PRSNT (12:9)	These bits have to be cleared by the CPU on the Base Module if an AMC is recognized on the corresponding AMC slot. These bits have to be set if the corresponding AMC slot is empty. HP_PRSNT9 is assigned to AMC9 and HP_PRSNT12 to AMC12
[7..4]	-	**no function** write as 0 and ignore when read

10.3.7 Hot Plug Button 1 Register

The Hot Plug Button 1 Register controls together with the The Hot Plug Button 2 Register controls together with the Hot Plug Button 1 Register the value of the /HP_BUTTON balls of the corresponding PEX8532.
HP_BUTTON2 Register the value of the /HP_BUTTON balls of the corresponding PEX8532.

Table 14: HP_BUTTON1 Register

Hot Plug Button 1 – Address 0x14								
Default value 0xff								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	HP_BUTTON[8:1]							

Table 15: HP_BUTTON1 - Register Bits

Bit	Name	Function
[7..0]	HP_BUTTON (8:1)	These bits have to be cleared and set again, if an AMC's HP handle was attended. HP_ BUTTON 1 is assigned to AMC1 and HP_ BUTTON 8 to AMC8

10.3.8 Hot Plug Button 2 Register

The Hot Plug Button 2 Register controls together with the Hot Plug Button 1 Register the value of the /HP_BUTTON balls of the corresponding PEX8532.

Table 16: HP_BUTTON2 Register

2nd Hot Plug Button – Address 0x15								
Default value 0xff								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-				HP_BUTTON[12:9]			

Table 17: HP_BUTTON2 - Register Bits

Bit	Name	Function
[7..0]	HP_BUTTON (12:9)	hese bits have to be cleared and set again, if an AMC's HP handle was attended. HP_ BUTTON 9 is assigned to AMC9 and HP_ BUTTON 12 to AMC12

10.3.9 Hot Plug Power Enable 1 Register

The Hot Plug Power Enable Register 1 Register shows together with the Hot Plug Power Enable 2 Register the value of the /HP_PWREN balls of the corresponding PEX8532.

Table 18: HP_PWREN1 Register

Hot Plug Power Enable 1 – Address 0x18								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	HP_PWREN[8:1]							

Table 19: HP_PWREN1 - Register Bits

Bit	Name	Function
[7..0]	HP_PWREN (8:1)	These bits represent the value of the /HP_PWREN balls. If the PCIe host allows that the corresponding AMC gets power the bit is cleared (Note: this has to be done by the PCIe host software). HP_ PWREN 1 is assigned to AMC1 and HP_ PWREN 8 to AMC8

10.3.10 Hot Plug Power Enable 2 Register

The Hot Plug Power Enable Register 1 Register shows together with the Hot Plug Power Enable 1 Register the value of the /HP_PWREN balls of the corresponding PEX8532.

Table 20: HP_PWREN2 Register

Hot Plug Power Enable 2 – Address 0x19								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	-				HP_PWREN[12:9]			

Table 21: HP_PWREN2 - Register Bits

Bit	Name	Function
[3..0]	HP_PWREN (12:9)	These bits represent the value of the /HP_PWREN balls. If the PCIe host allows that the corresponding AMC gets power the bit is cleared (Note: this has to be done by the PCIe host software). HP_ PWREN 9 is assigned to AMC9 and HP_ PWREN 12 to AMC12
[7..4]	-	**no function** write as 0 and ignore when read

10.3.11 Miscellaneous Control Register

The Miscellaneous Control register manages different strapping and reset pins of the two PEX8532 and the SSC generator.

Table 22: Misc_CTRL Register

Miscellaneous Control - Address 0x16								
Default value 0x03								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-					**SPREAD**	**/PERST2**	**/PERST1**

Table 23: Misc_CTRL - Register Bits

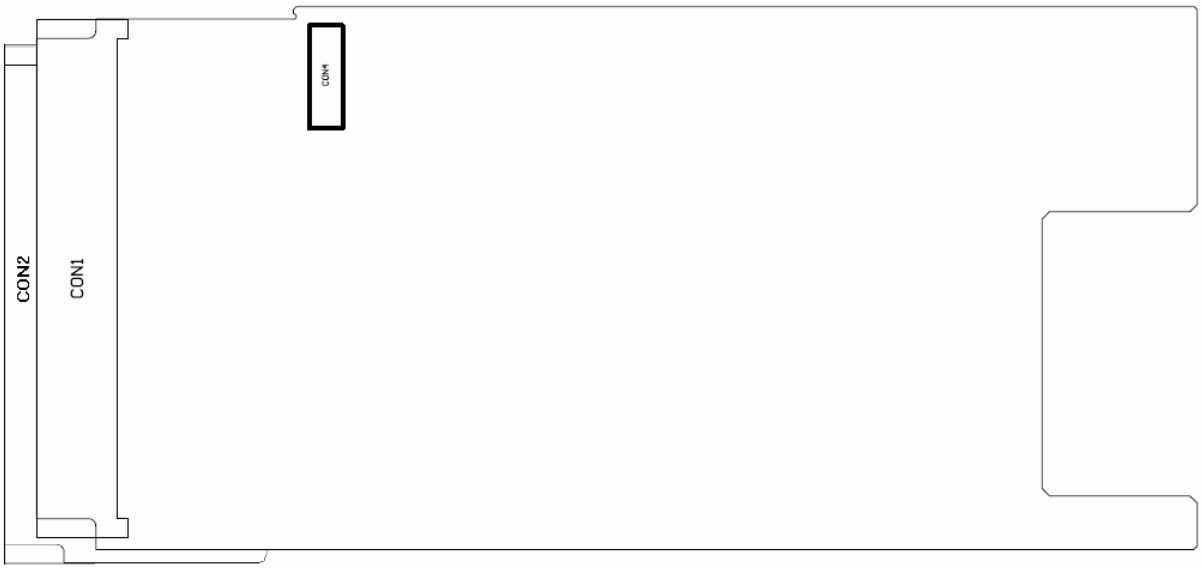
Bit	Name	Function
0	/PERST1	**This bit controls the /PERST pin of the 1st PEX8532.** A 0 in this bit causes a Fundamental reset of the 1st PEX8532.
1	/PERST2	**This bit controls the /PERST pin of the 2nd PEX8532.** A 0 in this bit causes a Fundamental reset of the 2nd PEX8532.
2	SPREAD	**The value of this bit selects if the SSC generates a spread spectrum signal or a fixed 100MHz signal.** 0 – fixed 1 – spread spectrum
[7..3]	-	**no function** write as 0 and ignore when read

11 Connectors

11.1 Connector Overview

Figure 4: Connectors of the NAT-MCH Hub Module PCIe (top view)

Figure 5: Connectors of the NAT-MCH Hub Module PCIe (bottom view)



Please refer to the following tables to look up the pin assignment of the **NAT-MCH Hub Module PCIe**.

11.2 NAT-MCH Hub Module PCIe Connector CON1

Table 24: Hub Module PCIe backplane connector CON1

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUD+	RxFUD+	163
9	TxFUD-	RxFUD-	162
10	GND	GND	161
11	TxFUE+	RxFUE+	160
12	TxFUE-	RxFUE-	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

11.3 NAT-MCH Hub Module x48 Extender Connector CON2

Table 25: Hub Module x48 Extender backplane connector CON2

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	TxFUF+	RxFUD+	163
9	TxFUF-	RxFUD-	162
10	GND	GND	161
11	TxFUG+	RxFUE+	160
12	TxFUG-	RxFUE-	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

11.4 Connector CON4: Interface to CLK-Module

Table 26: Connector to CLK-Module CON4

Pin No.	Signal	Signal	Pin No.
1	+12V	+12V	2
3	+12V	+12V	4
5	PCIeCLK_P	+3.3V_MP	6
7	PCIeCLK_N	SPICLK	8
9	GND	expansion3	10
11	MOSI	MISO	12
13	GND	/SPISEL_HUB PCB	14
15	SCL	N.C.	16
17	SDA	nRESET_HUB _PCB	18
19	GND	GND	20

This connector connects to the **CLK-Module**. On the **CLK-Module** the signals of this connector are routed to a connector that connects to the **Basic-Module**.

12 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] PLX, PEX8532AA/BA/BB/BC Express Lane Versatile PCI Express Switch, Data Book v1.7 07.2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	04.03.2008	initial revision	Ks