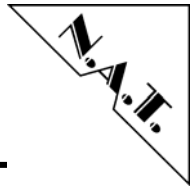

NAT-MCH
Clock-Module
Technical Reference Manual V 1.4
CLK Module HW
Revision 2.1 and Revision 2.3

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1: gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Board Specification

Table 2: NAT-MCH CLK Module Features

Power Consumption	12 V / 0.5 A max. (only **CLK Module**)	
Environmental Conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards Compliance	PICMG µTCA.0 Rev. 1.0	
	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.3 Rev. 1.0	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	IPMI Specification v2.0 Rev. 1.0	
Product Safety	The board complies with EN60950 and UL1950	
PLL Input Frequencies *(To be sourced from external Reference via Face Plate Connector, CLK1 or CLK2)*	• 2 kHz • 8 kHz • 1.544 MHz • 2.048 MHz • 8.192 MHz • 16.384 MHz • 19.44 MHz	
PLL Output Frequencies *(To be distributed via Face Plate Connector, CLK1, CLK2 orCLK3)*	• 1.544 MHz (T1) • 2.048 MHz (E1) • 3.088 MHz • 16.384 MHz • **19.44 MHz** (SDH) • 4.096 MHz or 32.768 MHz • 8.192 MHz or 65.536 MHz • 6.312 MHz (DS2) • 8.448 MHz (E2) • 44.736 MHz (DS3) • 34.368 MHz (E3) • 2 kHz and **8 kHz** (frame pulses)	

2 Statement on Environmental Protection

2.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

3 Installation

3.1 Safety Note

To ensure proper functioning of the **NAT-MCH CLK Module** during its usual lifetime take refer to the safety note section of the **NAT-MCH BASIC-Module** Technical Reference Manual before handling the board.

3.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

3.2.1 Requirements

The installation requires a **NAT-MCH Basic-PCB**, where the **CLK Module** can be mechanically fixed on to. The **CLK Module** must be completely connected and joint to the **Basic-PCB**, before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH BASIC-Module** Technical Reference Manual.

3.2.2 Power supply

The power supply for the **NAT-MCH CLK Module** must meet the following specifications:

+12 V / 0.5 A max. (only **CLK Module**, in addition to other PCBs of the **NAT-MCH**).

3.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH Basic-Module**

In the following situations the **NAT-MCH Basic-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

4 Introduction

The **NAT-MCH** consists of a **Basic-Module**, which can be expanded with additional PCBs. The **Basic-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **Basic-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB Modules** are available. With the **Clock-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs
- reception of clock signals from either of 12 AMCs or from the front panel input and redistribution

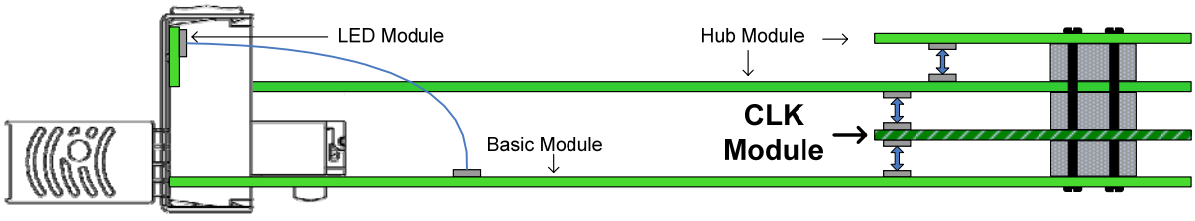
Through the extension of the **NAT-MCH** with a **HUB Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in *Figure 1*.

Figure 1: Arrangement of different NAT-MCH Modules



This Technical Reference Manual describes the **Clock-PCB**.

5 CLK Module Basics

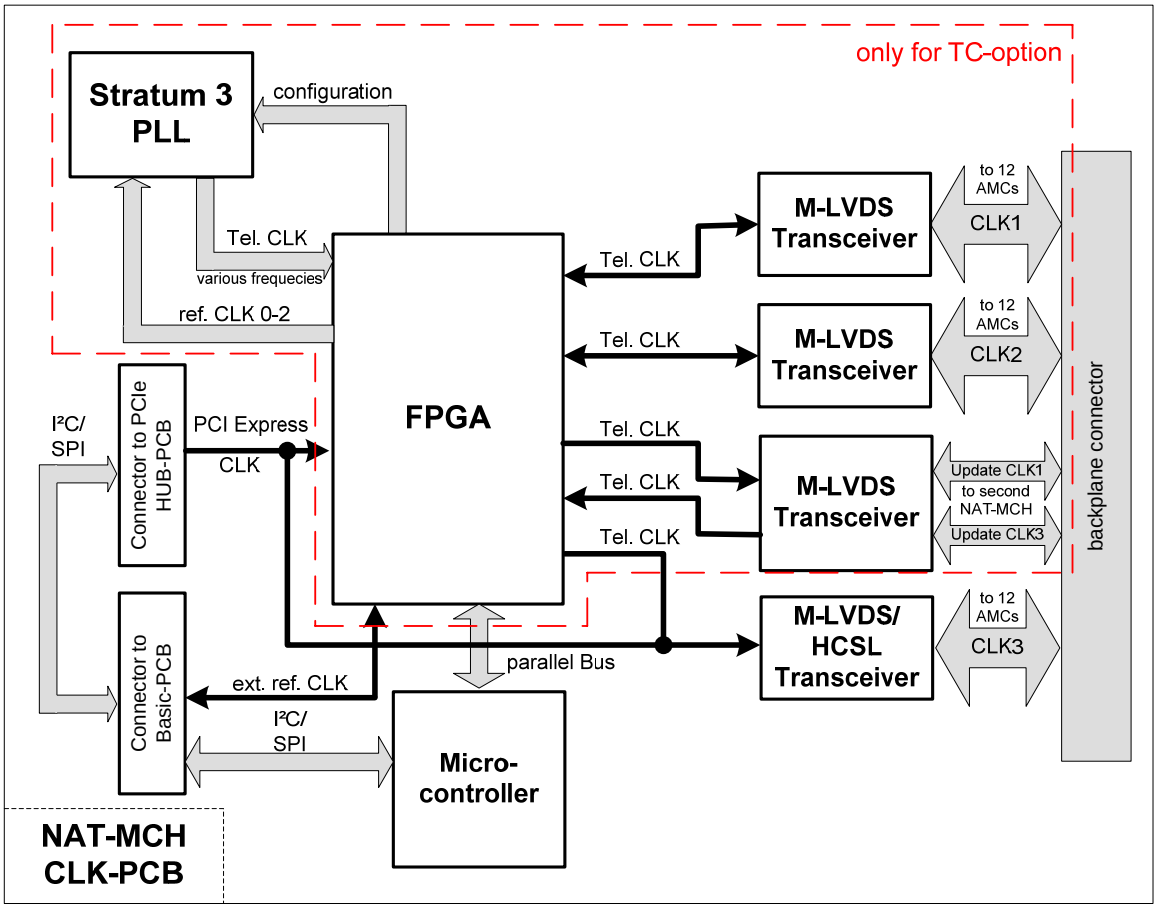
The **CLK Module** can be mounted on the **NAT-MCH Basic-PCB**. With the **CLK Module**, the 2nd tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed. The **NAT-MCH CLK Module** implements the following major features:

- support of AMC clocks CLK1, CLK2 and CLK3 for up to 12 AMCs
- support of CLK1 and CLK3 update for a second **NAT-MCH** in a redundant system
- support of the front panel reference clock In/Output
- Stratum 3 type PLL clock source for telecom applications with various output frequencies
- Telecom CLK signals can be distributed over all backplane clock connections and the front panel interface
- CLK1 and CLK2 from all 12 AMCs, the update clocks from a second **NAT-MCH**, or a signal from the front panel interface can be used as reference for the PLL
- a PCI Express compliant clock signal can be distributed via CLK3 to all 12 AMCs (only possible with a installed PCI Express **Hub-Module**)
- Support of M-LVDS **or** HCSL compliant driver and termination for CLK3

The Clock Module

6 Block Diagram of the NAT-MCH CLK Module

Figure 2: Block Diagram of the NAT-MCH CLK Module



7 BOARD FEATURES

- **PLL**

  The board is equipped with a Zarlink ZL30105 Stratum 3 PLL, which provides various typical telecom frequencies in the range from 8 kHz to 65.536 MHz. Especially to the two frequencies 8 kHz and 19.44 MHz, which are recommended for telecom applications by the MicroTCA Specification, are supported.

  The Zarlink PLL is only assembled if the “TC-Option” is chosen.

- **Microprocessor**

  To configure the **CLK Module** an Atmel 8-bit microprocessor resides on the **CLK Module**.

- **Interfaces**

CLK1: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any of the 12 AMCs.

CLK2: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any AMC.

CLK3: The **NAT-MCH CLK Module** implements clock interfaces to 12 AMCs. These interfaces can be used to send one of the telecom clock signals, or a PCI Express clock signal to the AMCs.

Update CLK: The **NAT-MCH CLK Module** implements 2 update channels (update CLK1 and CLK3). These channels are full-duplex connections to a second NAT-MCH. They can only be used to send and receive telecom clock signals (not the PCI Express clock signal).

Ext.-ref.-CLK: The **NAT-MCH CLK Module** supports an external reference clock in- or output, accessible via a face plate connector. This signal is routed to the **Base-Module**, were the face plate connector is assembled. If the external clock interface is used to receive a reference clock, this clock signal is amplified by a special input circuit on the **Base-Module**. This circuit accepts signal forms in a wide range, concerning frequency and input voltage as well as single ended or differential. For a more detailed specification of the input signal please refer to the hardware reference manual of the **Base-Module**.

- **Interface to other NAT-MCH PCBs**

  Basic PCB: - The Microprocessor on the **CLK Module** can be programmed by the ColdFire on the **Basic-Module** via a SPI interface. Normal communication between the Microprocessor and the ColdFire is done by IPMI messages via the I²C interface.

  - The external clock interface on the front panel is connected to the **CLK Module** via the interface to the **Basic-PCB** (via connector CON2).

  PCIe Hub-PCB: - The **CLK Module** can receive a PCI Express compliant clock signal from the **Hub-PCB** (only PCI Express versions).

8 Functional Blocks

The **NAT-MCH CLK Module** is divided into a number of functional blocks, which are described in the following paragraphs.

8.1 Stratum 3 PLL

The ZL30105 supports the Telcordia GR-1244-CORE Stratum 3/4E/4 specification. The ZL30105 accepts 3 different input references, and synchronizes to any combination of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz inputs. One input is connected to the external reference clock input on the face plate; the remaining two inputs are connected to the FPGA. By programming a FPGA register bit, any clock signal from any AMC (either CLK1 or CLK2) or from the other NAT-MCH (CLK1 or CLK3 update) can be connected to either of the two reference inputs of the PLL. If no reference signal is available, the ZL30105 uses a 25 MHz master clock for frequency generation in a free running mode. The 25 MHz clock is generated by an oscillator.

The ZL30105 generates the following output frequencies:

- 1.544 MHz (T1)
- 2.048 MHz (E1)
- 3.088 MHz
- 16.384 MHz
- **19.44 MHz** (SDH)
- 4.096 MHz or 32.768 MHz
- 8.192 MHz or 65.536 MHz
- 6.312 MHz (DS2)
- 8.448 MHz (E2)
- 44.736 MHz (DS3)
- 34.368 MHz (E3)
- 2 kHz and **8 kHz** (frame pulses)

The different output signals are provided through different output pins of the ZL30105[1]. These output pins are connected to the FPGA.

Also the different configuration inputs are connected to the FPGA or to the microprocessor, and thus can be configured at runtime by application software.

The Zarlink PLL is only assembled if the TC-Option is chosen.

8.2 Microprocessor

An Atmel 8-bit microprocessor resides on the **CLK Module**. With the help of this microprocessor, the ColdFire of the base board can configure all multiplexers implemented in the FPGA and enable the M-LVDS/HCSL transceivers for the connection to each AMCs. The Atmel firmware can be updated by the ColdFire on the **Base Module** over the SPI interface. The ColdFire communicates with the **CLK Module** via IPMI (using the I²C interface).

8.3 CLK-Multiplex Function

Flexible multiplexing of the various clock signals is achieved by an Altera Cyclone FPGA. Multiplexing of source clock signals to destination clock signals is performed by programming a register interface provided by the microcontroller.

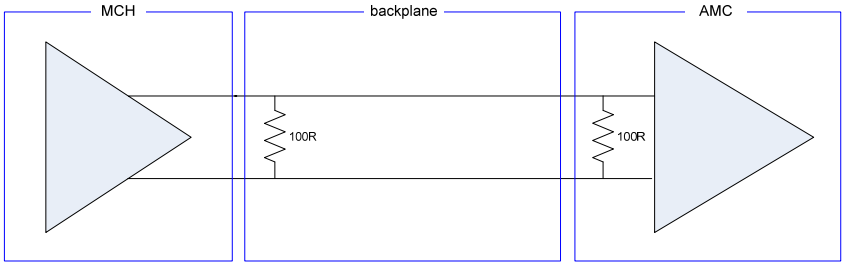
The FPGA for these multiplexers is only assembled with the TC-option

8.4 M-LVDS / HCSL Transceiver

The MicroTCA R1.0 Specification recommends that all clock interfaces are equipped with M-LVDS compliant driver/receiver and termination. Against that the AMC.0 R2.0 allows for FCLKA (formerly CLK3) also HCSL compliant driver/receiver and termination.

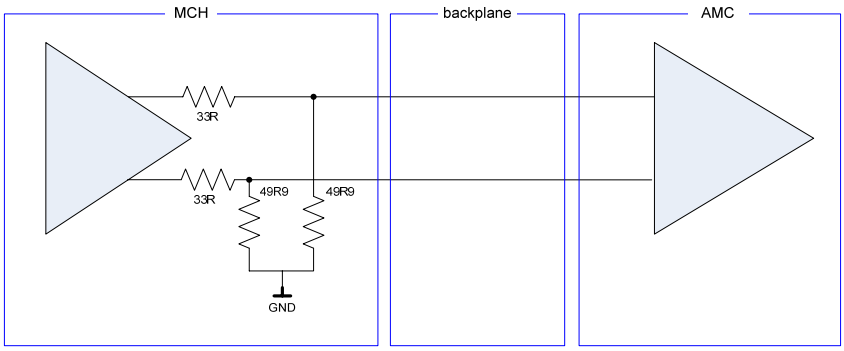
The main difference between the two signal specifications, which makes it difficult to realize both with the same hardware, is the different termination. M-LVDS uses a dual differential termination between the two complimentary clock lines at both ends of the bus. This termination is shown in Figure 3.

Figure 3: M-LVDS Termination



HCSL uses a source-only termination with two series and term-to-ground resistors. This termination is depicted in Figure 4.

Figure 4: HCSL termination



Because of this differences N.A.T. decided to offer two different assembly/ordering options SSCM (Spread Spectrum Clock M-LVDS) and SSCH (Spread Spectrum Clock HCSL). The SSCM option implements M-LVDS compliant Transmitter and termination for CLK3. The SSCH option implements HCSL compliant Transmitter and termination.

Either the SSCM or the SSCH option can be chosen. Beside these two options always the TC option can additionally be chosen. The TC option implements always M-LVDS compliant transceiver and termination for CLK1, CLK2 and Update CLK1/3.

9 Location Overview

Figure 5 and Figure 6 are showing the position of important components. Depending on the chosen options it may be that the board does not include all components named in the location diagram. Hardware revision v2.1 implements the SSCM option and v2.3 the SSCH option

Figure 5: Location Diagram of the NAT-MCH CLK Module v2.1 (top-view)

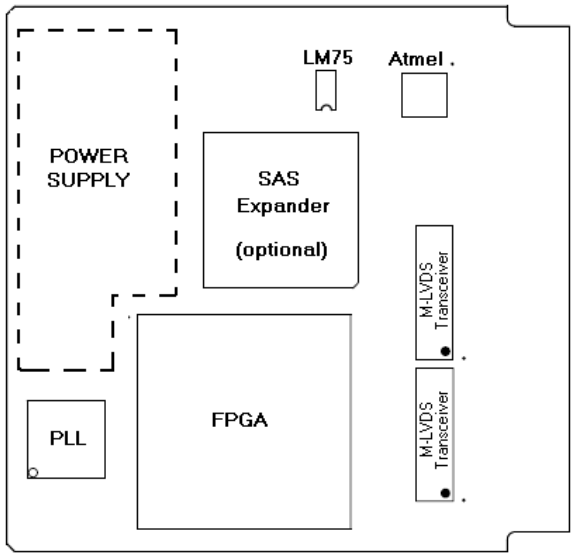


Figure 6: Location diagram of the NAT-MCH CLK Module v2.1 (bottom-view)

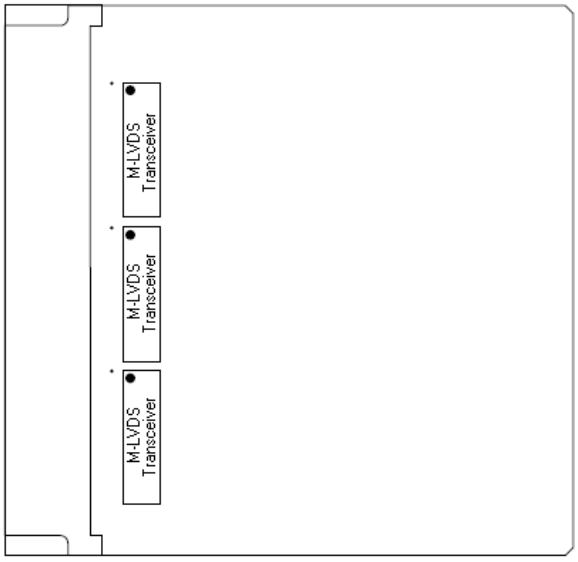


Figure 7: Location Diagram of the NAT-MCH CLK Module v2.3 (top-view)

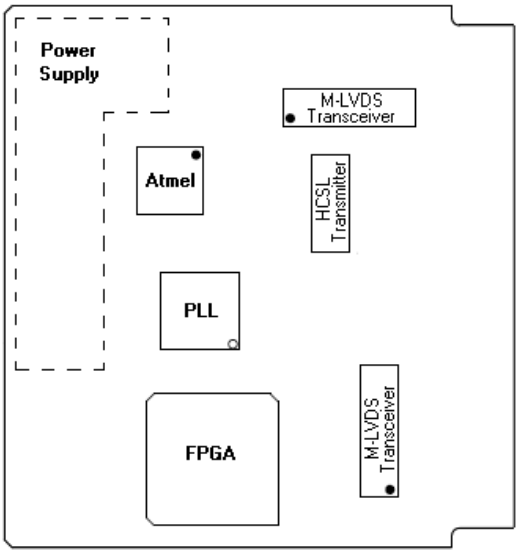
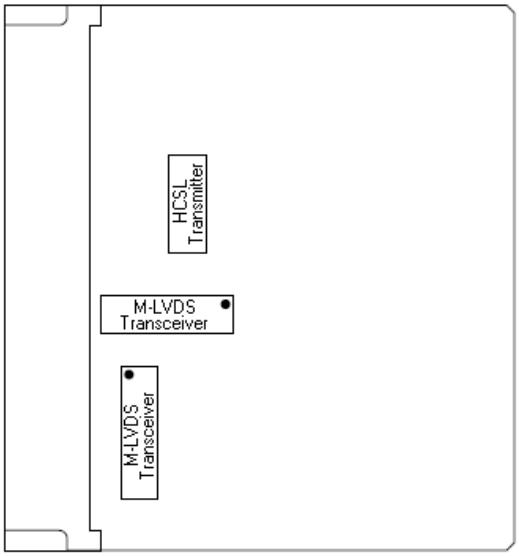


Figure 8: Location Diagram of the NAT-MCH CLK Module v2.3 (bottom-view)



10 Connectors

10.1 Connector Overview

Since hardware revision v2.1 and v2.3 of the CLK Module are compatible to the other MCH modules all connectors are at the same position. Therefore Figure 9 and Figure 10 are guilty for both Hardware revisions.

Figure 9: Connectors of the NAT-MCH CLK Module (top view)

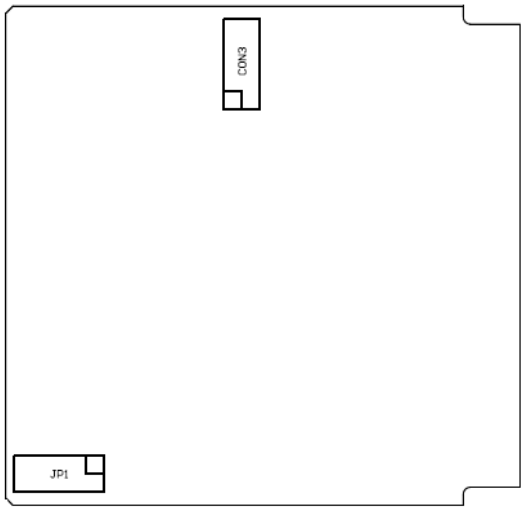
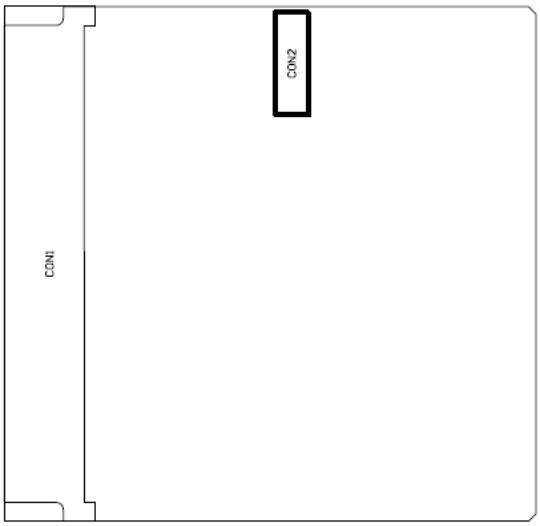


Figure 10: Connectors of the NAT-MCH CLK Module (bottom view)



Please refer to the following tables for the pin assignment of the **NAT-MCH CLK Module**.

10.2 MCH Connector CON1

Table 3: MCH Connector CON1

Pin No.	MCH-Signal	MCH-Signal	Pin No.
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	CLK3_Tx+	CLK3_Rx+	163
9	CLK3_Tx-	CLK3_Rx-	162
10	GND	GND	161
11	CLK1_Tx+	CLK1_Rx+	160
12	CLK1_Tx-	CLK1_Rx-	159
13	GND	GND	158
14	TxFB-1+	RxFB-1+	157
15	TxFB-1-	RxFB-1-	156
16	GND	GND	155
17	TxFB-2+	RxFB-2+	154
18	TxFB-2-	RxFB-2-	153
19	GND	GND	152
20	TxFB-3+	RxFB-3+	151
21	TxFB-3-	RxFB-3-	150
22	GND	GND	149
23	TxFB-4+	RxFB-4+	148
24	TxFB-4-	RxFB-4-	147
25	GND	GND	146
26	TxFB-5+	RxFB-5+	145
27	TxFB-5-	RxFB-5-	144
28	GND	GND	143
29	TxFB-6+	RxFB-6+	142
30	TxFB-6-	RxFB-6-	141
31	GND	GND	140
32	CLK3-1+	CLK3-7+	139
33	CLK3-1-	CLK3-7-	138
34	GND	GND	137
35	CLK3-2+	CLK3-8+	136
36	CLK3-2-	CLK3-8-	135
37	GND	GND	134

Pin No.	MCH-Signal	MCH-Signal	Pin No.
38	CLK3-3+	CLK3-9+	133
39	CLK3-3-	CLK3-9-	132
40	GND	GND	131
41	CLK3-4+	CLK3-10+	130
42	CLK3-4-	CLK3-10-	129
43	GND	GND	128
44	CLK3-5+	CLK3-11+	127
45	CLK3-5-	CLK3-11-	126
46	GND	GND	125
47	CLK3-6+	CLK3-12+	124
48	CLK3-6-	CLK3-12-	123
49	GND	GND	122
50	CLK1-1+	CLK2-1+	121
51	CLK1-1-	CLK2-1-	120
52	GND	GND	119
53	CLK1-2+	CLK2-2+	118
54	CLK1-2-	CLK2-2-	117
55	GND	GND	116
56	CLK1-3+	CLK2-3+	115
57	CLK1-3-	CLK2-3-	114
58	GND	GND	113
59	CLK1-4+	CLK2-4+	112
60	CLK1-4-	CLK2-4-	111
61	GND	GND	110
62	CLK1-5+	CLK2-5+	109
63	CLK1-5-	CLK2-5-	108
64	GND	GND	107
65	CLK1-6+	CLK2-6+	106
66	CLK1-6-	CLK2-6-	105
67	GND	GND	104
68	CLK1-7+	CLK2-7+	103
69	CLK1-7-	CLK2-7-	102
70	GND	GND	101
71	CLK1-8+	CLK2-8+	100
72	CLK1-8-	CLK2-8-	99
73	GND	GND	98
74	CLK1-9+	CLK2-9+	97
75	CLK1-9-	CLK2-9-	96
76	GND	GND	95
77	CLK1-10+	CLK2-10+	94
78	CLK1-10-	CLK2-10-	93

Pin No.	MCH-Signal	MCH-Signal	Pin No.
79	GND	GND	92
80	CLK1-11+	CLK2-11+	91
81	CLK1-11-	CLK2-11-	90
82	GND	GND	89
83	CLK1-12+	CLK2-12+	88
84	CLK1-12-	CLK2-12-	87
85	GND	GND	86

10.3 Connector Con2: Interface to Basic-PCB

Connector CON2 connects the **NAT-MCH CLK Module** with the **Basic-PCB**

Table 4: Connector to Basic-PCB CON2

Pin No.	Signal	Signal	Pin No.
1	+12V	+12V	2
3	+12V	+12V	4
5	EXTREF_OUT_P	+3.3V MP	6
7	EXTREF_OUT_N	SPICLK	8
9	GND	EXTREF_IN	10
11	MOSI	MISO	12
13	GND	/SPISEL_HUB PCB	14
15	SCL	nRESET_CLK-PCB	16
17	SDA	nRESET_HUB-PCB	18
19	GND	GND	20

10.4 Connector CON3: Interface to Hub-PCB

Connector CON3 connects the **CLK Module** with the **HUB-PCB**.

Table 5: Connector to Hub-PCB CON3

Pin No.	Signal	Signal	Pin No.
1	+12V	+12V	2
3	+12V	+12V	4
5	PCIeCLK_P	+3.3V MP	6
7	PCIeCLK_N	SPICLK	8
9	GND	expansion3	10
11	MOSI	MISO	12
13	GND	/SPISEL_HUB PCB	14
15	SCL	nRESET_CLK-PCB	16
17	SDA	nRESET_HUB-PCB	18
19	GND	GND	20

10.5 Connector JP1: Altera FPGA Programming Port

Connector JP1 connects the serial programming-port of the Altera FPGA device.

Table 6: Altera FPGA Programming Port

Pin No.	Signal	Signal	Pin No.
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATAO	/CSO	8
9	ASDI	GND	10

11 NAT-MCH CLK Module Programming Notes

11.1 SPI Interface

The SPI interface on the **CLK Module** is used only for maintenance purposes, e.g. updating the microcontroller firmware.

11.2 I²C Interface

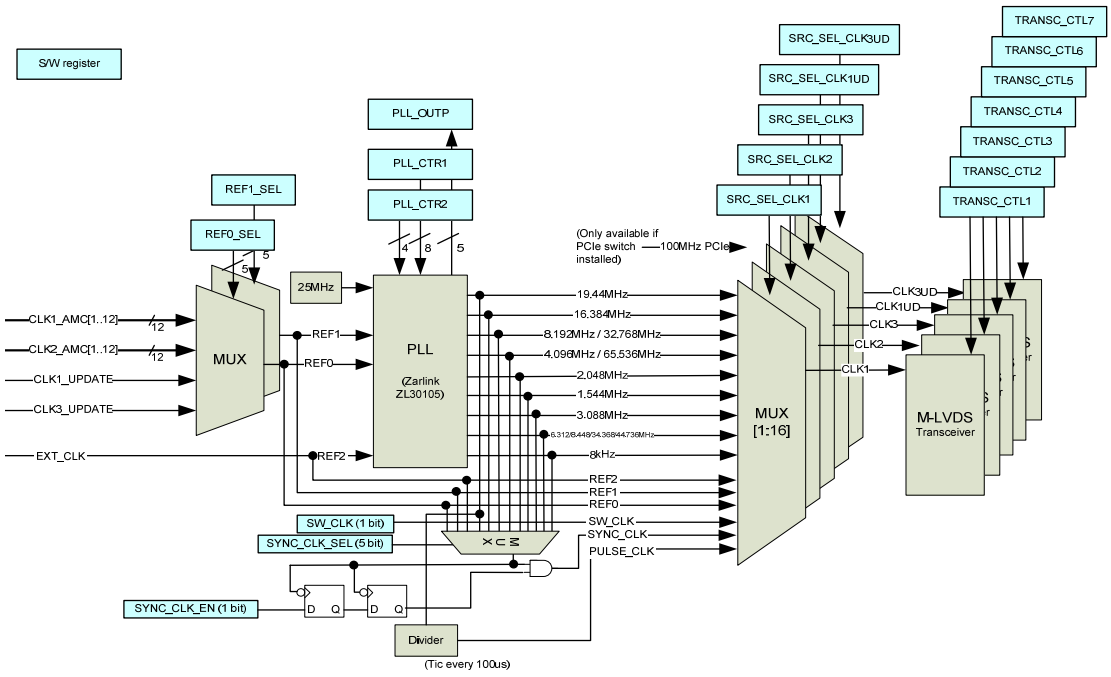
The I²C interface is the main communication interface between the microcontroller and the CPU of the **Basic-Module**. All communication is based on IPMI Messages.

11.3 Register

Functions that are controlled by following registers are realized within the FPGA. Only red cycles on register Firmware Version Register are directly answered by the Atmel Microcontroller.

To get a better understanding of the (multiplexer-) functions that can be controlled by the following registers, Figure 11 shows a detailed overview.

Figure 11: Detailed Functional overview



11.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH CLK Module**.

Table 7: Board Identifier Register

Board Identifier - Address 0x00								
Default value 0xb4								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	BOARD_ID							

11.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH CLK Module**.

Table 8: PCB Revision Register

PCB Revision - Address 0x01								
Default value 0xXX								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB_REV							

Bit 7 to 4 contains the major revision and bit 3 to 0 contains the minor revision. That means if the PCB revision is e.g. v1.3 the PCB Revision register contains the value 0x13.

11.3.3 Firmware Version Register

The Atmel Version Register contains the Version of the Atmel firmware.

Table 9: FW_VERSION Register

FW Version - Address 0x02								
Default value # of running Firmware version								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FW_VERSION							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the Firmware running on the Atmel is v1.3 the Firmware Version register contains the value 0x13.

11.3.4 FPGA Revision Register

The FPGA Revision Register contains the revision code of the Altera FPGA.

Table 10: FPGA Revision Register

FPGA Revision - Address 0x03								
Default value # of running FPGA revision								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FPGA_REV							

Bit 7 to 4 contains the major version and bit 3 to 0 contains the minor version. That means if the FPGA is running with the image v1.3 the FPGA Version register contains the value 0x13

11.3.5 Reference 0 Selection Register

The value of the Reference 0 Selection Register decides which source is connected to REF0 of the PLL.

Table 11: REF0_SEL Register

Reference 0 Selection - Address 0x04								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	**REF0_SEL**				

Table 12: REF0_SEL - Register Bits

Bit	Name	Function
[4..0]	REF0_SEL	**Reference Select for REF0 input of the PLL** 0x01 – CLK2 of AMC1 0x02 – CLK2 of AMC2 : 0x0C – CLK2 of AMC12 0x0D – CLK1 Update (from 2nd MCH) 0x0E – CLK3 Update (from 2nd MCH) 0x11 – CLK1 of AMC1 0x12 – CLK1 of AMC2 : 0x1C – CLK1 of AMC12 all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

11.3.6 Reference 1 Selection Register

The value of the Reference 1 Selection Register decides which source is connected to REF1 of the PLL.

Table 13: REF1_SEL Register

Reference 1 Selection - Address 0x05								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	**REF1_SEL**				

Table 14: REF1_SEL - Register Bits

Bit	Name	Function
[4..0]	REF1_SEL	**Reference Select for REF1 input of the PLL** 0x01 – CLK2 of AMC1 0x02 – CLK2 of AMC2 : 0x0C – CLK2 of AMC12 0x0D – CLK1 Update (from 2nd MCH) 0x0E – CLK3 Update (from 2nd MCH) 0x11 – CLK1 of AMC1 0x12 – CLK1 of AMC2 : 0x1C – CLK1 of AMC12 all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

11.3.7 Source Selection 1 Register

The value of the Source Selection 1 Register decides which output (of the PLL) is connected to the CLK1 Transceiver.

Table 15: SRC_SEL1 Register

Source Selection 1 - Address 0x06								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	**SRC_SEL_CLK1**				

Table 16: SRC_SEL1 - Register Bits

Bit	Name	Function
[4..0]	SRC_SEL_ CLK1	**Selects the output of the PLL which is connected to CLK1** 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz (stratum3) 0x14 – holdover all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

The SRC_SEL bits in combination with the OUTSEL bits (refer to the PLL Control 2 Register) set the frequency, which is transmitted to the AMCs.

11.3.8 Source Selection 2 Register

The value of the Source Selection 2 Register decides which output (of the PLL) is connected to the CLK2 Transceiver.

Table 17: SRC_SEL2 Register

Source Selection 2 – Address 0x07								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	**SRC_SEL_CLK2**				

Table 18: SRC_SEL2 - Register Bits

Bit	Name	Function
[4..0]	SRC_SEL_ CLK2	**Selects the output of the PLL which is connected to CLK2** 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz (stratum3) 0x14 – holdover all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

The SRC_SEL bits in combination with the OUTSEL bits (refer to the PLL Control 2 Register) set the frequency, which is transmitted to the AMCs.

11.3.9 Source Selection 3 Register

The value of the Source Selection 3 Register decides which output (of the PLL) is connected to the CLK3 Transceiver.

Table 19: SRC_SEL3 Register

Source Selection 3 – Address 0x08								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	**SRC_SEL_CLK3**				

Table 20: SRC_SEL3 - Register Bits

Bit	Name	Function
[4..0]	SRC_SEL_ CLK3	**Selects the output of the PLL which is connected to CLK3** 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0A – PCIeCLK 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz (stratum3) 0x14 – holdover all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

The SRC_SEL bits in combination with the OUTSEL bits (refer to the PLL Control 2 Register) set the frequency, which is transmitted to the AMCs.

11.3.10 Source Selection CLK1 Update Register

The value of the Source Selection CLK1 Update Register decides which output (of the PLL) is connected to the Update CLK1 Transceiver.

Table 21: SRC_SEL_CLK1_UD Register

Source Selection CLK1 Update – Address 0x09								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	SRC_SEL_CLK1_UD				

Table 22: SRC_SEL_CLK1_UD - Register Bits

Bit	Name	Function
[4..0]	SRC_SEL_ CLK1_UD	**Selects the output of the PLL which is connected to CLK1 Update** 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz (stratum3) 0x14 – holdover all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

The SRC_SEL_CLK1_UD bits in combination with the OUTSEL bits (refer to the PLL Control 2 Register) set the frequency, which is transmitted to the second MCH.

11.3.11 Source Selection CLK3 Update Register

The value of the Source Selection CLK3 Update Register decides which output (of the PLL) is connected to the Update CLK3 Transceiver.

Table 23: SRC_SEL_CLK3_UD Register

Source Selection CLK3 Update – Address 0x0A								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	SRC_SEL_CLK3_UD				

Table 24: SRC_SEL_CLK3_UD - Register Bits

Bit	Name	Function
[4..0]	SRC_SEL_ CLK3_UD	**Selects the output of the PLL which is connected to CLK3 Update** 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz (stratum3) 0x14 – holdover all other values result in no connection
[7..5]	-	**no function** write as 0 and ignore when read

The SRC_SEL_CLK1_UD bits in combination with the OUTSEL bits (refer to the PLL Control 2 Register) set the frequency, which is transmitted to the second MCH.

11.3.12 Transceiver Control 1 Register

The value of the Transceiver Control 1 Register controls the receive function of all M-LVDS transceiver and the transmit function of the Update M-LVDS transceiver.

Table 25: TRANSC_CTL1 Register

Transceiver Control 1 - Address 0x0B								
Default value 0x70								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	**nRE_UP**	**nRE_CLK2**	**nRE_CLK1**	-	-	**DE_CLK3 UP**	**DE_CLK1 UP**

Table 26: TRANSC_CTL1 - Register Bits

Bit	Name	Function
0	DE_CLK1UP	Setting this bit to a logic high enables the transmit function for CLK1 Update.
1	DE_CLK3UP	Setting this bit to a logic high enables the transmit function for CLK3 Update.
[3..2]	-	**no function** write as 0 and ignore when read
4	nRE_CLK1	Clearing this bit enables global the read function for CLK1 *Note: A signal can only be received or transmitted over CLK1, not both. That means if the* nRE_CLK1 *bit is cleared it has to be ensured by software that all* DE_CLK1 *bits and the* Source Selection 1 Register *are cleared.*
5	nRE_CLK2	Clearing this bit enables global the read function for CLK2 *Note: A signal can only be received or transmitted over CLK1, not both. That means if the* nRE_CLK1 *bit is cleared it has to be ensured by software that all* DE_CLK1 *bits and the* Source Selection 2 Register *are cleared.*
6	nRE_UP	Clearing this bit enables the read function for CLK1 update and CLK3 update
7	-	**no function** write as 0 and ignore when read

11.3.13 Transceiver Control 2 Register

The value of the Transceiver Control 2 Register controls the transmit function of the M-LVDS transceiver for CLK1, AMC1-8.

Table 27: TRANSC_CTL2 Register

Transceiver Control 2 - Address 0x0C								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**DE_CLK1-8**	**DE_CLK1-7**	**DE_CLK1-6**	**DE_CLK1-5**	**DE_CLK1-4**	**DE_CLK1-3**	**DE_CLK1-2**	**DE_CLK1-1**

Table 28: TRANSC_CTL2 - Register Bits

Bit	Name	Function
0	DE_CLK1-1	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 1.
1	DE_CLK1-2	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 2.
2	DE_CLK1-3	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 3.
3	DE_CLK1-4	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 4.
4	DE_CLK1-5	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 5.
5	DE_CLK1-6	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 6.
6	DE_CLK1-7	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 7.
7	DE_CLK1-8	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 8.

11.3.14 Transceiver Control 3 Register

The value of the Transceiver Control 3 Register controls the transmit function of the M-LVDS transceiver for CLK1, AMC9-12.

Table 29: TRANSC_CTL3 Register

Transceiver Control 3 - Address 0x0D								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	**DE_CLK1-12**	**DE_CLK1-11**	**DE_CLK1-10**	**DE_CLK1-9**

Table 30: TRANSC_CTL3 - Register Bits

Bit	Name	Function
0	DE_CLK1-9	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 9.
1	DE_CLK1-10	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 10.
2	DE_CLK1-11	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 11.
3	DE_CLK1-12	Setting this bit to a logic high enables the transmit function for CLK1 for AMC Slot 12.
[7..4]	-	**no function** write as 0 and ignore when read

11.3.15 Transceiver Control 4 Register

The value of the Transceiver Control 4 Register controls the transmit function of the M-LVDS transceiver for CLK2, AMC1-8.

Table 31: TRANSC_CTL4 Register

Transceiver Control 4 - Address 0x0E								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**DE_CLK2-8**	**DE_CLK2-7**	**DE_CLK2-6**	**DE_CLK2-5**	**DE_CLK2-4**	**DE_CLK2-3**	**DE_CLK2-2**	**DE_CLK2-1**

Table 32: TRANSC_CTL4 - Register Bits

Bit	Name	Function
0	DE_CLK2-1	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 1.
1	DE_CLK2-2	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 2.
2	DE_CLK2-3	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 3.
3	DE_CLK2-4	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 4.
4	DE_CLK2-5	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 5.
5	DE_CLK2-6	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 6.
6	DE_CLK2-7	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 7.
7	DE_CLK2-8	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 8.

11.3.16 Transceiver Control 5 Register

The value of the Transceiver Control 5 Register controls the transmit function of the M-LVDS transceiver for CLK2, AMC9-12.

Table 33: TRANSC_CTL5 Register

Transceiver Control 5 - Address 0x0F								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	**DE_CLK2-12**	**DE_CLK2-11**	**DE_CLK2-10**	**DE_CLK2-9**

Table 34: TRANSC_CTL5 - Register Bits

Bit	Name	Function
0	DE_CLK2-9	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 9.
1	DE_CLK2-10	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 10.
2	DE_CLK2-11	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 11.
3	DE_CLK2-12	Setting this bit to a logic high enables the transmit function for CLK2 for AMC Slot 12.
[7..4]	-	**no function** write as 0 and ignore when read

11.3.17 Transceiver Control 6 Register

The value of the Transceiver Control 6 Register controls the transmit function of the M-LVDS transceiver for CLK3, AMC1-8.

Table 35: TRANSC_CTL6 Register

Transceiver Control 6 - Address 0x10								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**DE_CLK3-8**	**DE_CLK3-7**	**DE_CLK3-6**	**DE_CLK3-5**	**DE_CLK3-4**	**DE_CLK3-3**	**DE_CLK3-2**	**DE_CLK3-1**

Table 36: TRANSC_CTL6 - Register Bits

Bit	Name	Function
0	DE_CLK3-1	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 1.
1	DE_CLK3-2	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 2.
2	DE_CLK3-3	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 3.
3	DE_CLK3-4	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 4.
4	DE_CLK3-5	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 5.
5	DE_CLK3-6	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 6.
6	DE_CLK3-7	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 7.
7	DE_CLK3-8	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 8.

11.3.18 Transceiver Control 7 Register

The value of the Transceiver Control 7 Register controls the transmit function of the M-LVDS transceiver for CLK3, AMC9-12.

Table 37: TRANSC_CTL7 Register

Transceiver Control 7 - Address 0x11								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	**DE_CLK3-12**	**DE_CLK3-11**	**DE_CLK3-10**	**DE_CLK3-9**

Table 38: TRANSC_CTL7 - Register Bits

Bit	Name	Function
0	DE_CLK3-9	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 1.
1	DE_CLK3-10	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 2.
2	DE_CLK3-11	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 3.
3	DE_CLK3-12	Setting this bit to a logic high enables the transmit function for CLK3 for AMC Slot 4.
[7..4]	-	**no function** write as 0 and ignore when read

11.3.19 PLL Control 1 Register

The PLL Control 1 Register manages together with the PLL_CTR2 Register the control inputs of the Zarlink PLL.

Table 39: PLL_CTR1 Register

PLL Control 1 - Address 0x12								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**OUT_SEL 2**	**OUT_SEL 1**	**OUT_SEL 0**	**MODE_ SEL1**	**MODE_ SEL0**	**REF_SEL1**	**REF_SEL0**	**PLL_RST**

Table 40: PLL_CTR1 – Register Bits

Bit	Name	Function
0	PLL_RST	Setting this bit to a logic high resets the PLL
[2..1]	REF_SEL	**Selects which Reference input is the active reference of the PLL** 0b00 – REF0 Reference as defined by REF0_SEL Register 0b01 – REF1 Reference as defined by REF1_SEL Register 0b10 – REF2 (External reference CLK from face Plate connector) 0b11 – REF2
[4..3]	MODE_SEL	**Selects the PLL MODE** 00 – Normal Mode 01 – Holdover Mode 10 – Free running Mode 11 – Automatic (Normal with automatic Holdover and automatic reference switching)
[7..5]	OUT_SEL	this bit selects the signals on the combined output clock pins OUTSEL2 : Generated outputs 0 : C2o, /C4o, C8o, /C16o 1 : C2o, /C16o, C32, C65o OUTSEL[1..0]: Generated outputs 00 : C6o 01 : C8.4o 10 : C34o

11.3.20 PLL Control 2 Register

The PLL Control 2 Register manages together with the PLL_CTR1 Register the control inputs of the Zarlink PL L.

Table 41: PLL_CTR2 Register

PLL Control 2 - Address 0x13								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-				**HMS**	**SEC_ MSTR**	**TIE_ CLEAR**	**FAST-LOCK**

Table 42: PLL_CTR2 - Register Bits

Bit	Name	Function
0	**FAST-LOCK**	set temporarily high to allow the PLL to quickly lock to the input reference (one second locking time)
1	**TIE_ CLEAR**	A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase.
2	**SEC_MSTR**	Clearing this bit selects the Primary Master mode of operation with 1.8 Hz or 3.6 Hz DPLL loop filter bandwidth. Setting this bit selects Secondary Master mode which forces the PLL to clear its TIE corrector circuit and lock to the selected reference using a high bandwidth loop filter and a phase slope limiting of 9.5 ms/s.
3	**HMS**	The HMS input controls phase accumulation during the transition from Holdover or Freerun mode to Normal mode on the same reference. A logic low at this bit will cause the PLL to maintain the delay stored in the TIE corrector circuit when it transitions from Holdover or Freerun mode to Normal mode. A 1 on this bit will cause the PLL to measure a new delay for its TIE corrector circuit thereby minimizing the output phase movement when it transitions from Holdover or Freerun mode to Normal mode.
[7..4]	-	**no function** write as 0 and ignore when read

11.3.21 PLL Output Signals Register

The PLL Output Signals Register shows the state of the PLL Output signals.

Table 43: PLL_Outp Register

PLL Output Signals - Address 0x14								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	-	-	-	**HOLD-OVER**	**LOCK**	**REF_FAIL 2**	**REF_FAIL 1**	**REF_FAIL 0**

Table 44: PLL_Outp - Register Bits

Bit	Name	Function
0	REF_FAIL0	A logic high shows that the Reference, that is connected to REF0 of the PLL has failed
1	REF_FAIL1	A logic high shows that the Reference, that is connected to REF1 of the PLL has failed
2	REF_FAIL2	A logic high Shows that the external Reference, that is connected to REF2 of the PLL has failed
3	LOCK	This output goes to a logic high when the PLL is frequency locked to the selected input reference
4	HOLDOVER	This bit goes to a logic high whenever the PLL goes into holdover mode
[7..5]	-	no function write as 0 and ignore when read

11.3.22 Reserved Register

The Reserved Register bytes are used for N.A.T. internal tests. Do not change the value of these Registers.

Table 45: RES_1 Register

Reserved 1 - Address 0x15								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

Table 46: RES_2 Register

Reserved 2 - Address 0x16								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

Table 47: RES_3 Register

Reserved 3- Address 0x17								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

Table 48: RES_4 Register

Reserved 4 - Address 0x18								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

Table 49: RES_5 Register

Reserved 5 - Address 0x19								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

Table 50: RES_6 Register

Reserved 6 - Address 0x1A								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-

11.3.23 Synchronized Clock Register

The Synchronized Clock Register contains extended features to choose a source that can be distributed to all AMCs.

Table 51: SYNC_CLK Register

Synchronized Clock - Address 0x1B								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	**SYNC_CLK_EN**	**SW_CLK**	**SYN_CLK_SEL**				

Table 52: SYNC_CLK - Register Bits

Bit	Name	Function
[4..0]	SYNC_CLK_SEL	The Sync Clock Selection bits control the SYNC_CLK multiplexer. The output of this multiplexer can be selected as a source for the CLK1-3. 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK all other values result in no connection Note: The output of the SYNC_CLK multiplexer is low until the SYNC_CLK_EN bit is set.
5	SW_CLK	The SW_CLK can be selected as source, to be transmitted to the AMCs. The actual value of this bit is then transmitted to the AMCs.
6	SYNC_CLK_EN	A logic high in this bit enables the output of the SYNC_CLK multiplexer.
7	-	no function write as 0 and ignore when read

11.3.24 LED2 Control Register

The LED2 Control Register selects the LED2 function.

Table 53: LED2_CTR Register

LED2 Control - Address 0x1C								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W
Func	-	-	-	-	-	LED2_CTR		

Table 54: LED2_CTR - Register Bits

Bit	Name	Function
[2..0]	LED2_CTR	**selects the LED2 function** 0b000 – LED2 is on if the PLL is locked and blinks fast if PLL is in holdover state (not supported with FPGA version 1.2) 0b001 – LED2 is off 0b010 – LED2 is on 0b011 – LED2 blinks fast 0b100 – LED2 blinks slow
[7..3]	-	**no function** write as 0 and ignore when read

11.3.25 Holdover Function Control Register

The value of the Holdover Function Control Register controls the mode of the holdover function.

Table 55: H_OVER_FUNKT_CTL Register

Holdover Function Control - Address 0x2d								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Func	H_OVER_MUX					HOLDOVER	MODE	

Table 56: H_OVER_FUNKT_CTL - Register Bits

Bit	Name	Function
[1..0]	MODE	**These bits control the functionality of the holdover function.** 00 = Holdover function in reset 01 = Automatic holdover/switch-back (Switches over to internal generated 10MHz clock if reference fails. Switches back to reference if reference is again valid.) 10 = Automatic holdover, no switch-back 11 = permanent connected to internal generated 10MHz Clock
2	HOLDOVER	**Shows the state of the holdover function.** 0 – Holdover inactive (Clock selected by H_OVER_MUX is used) 1 – Holdover active (internal generated 10MHz clock is used)
[7..3]	H_OVER_ MUX	**Selects the input of the Holdover function** 0x00 – external clock (from face plate) 0x01 – CLK2 of AMC1 0x02 – CLK2 of AMC2 : 0x0C – CLK2 of AMC12 0x0D – CLK1 Update (from 2nd MCH) 0x0E – CLK3 Update (from 2nd MCH) 0x11 – CLK1 of AMC1 0x12 – CLK1 of AMC2 : 0x1C – CLK1 of AMC12 all other values result in no connection

11.3.26 External Reference Output Control Register

The value of the External Reference Output Control Register enables and configures the external clock outpu.

Table 57: EXT_REF_OUTP_CTL Register

External ReferenceOutput Control - Address 0x2E								
Default value 0x00								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**EN_OUTP**	**HIGH-AMPL**	**-EXT_REF_OUT_MUX**					

Table 58: EXT_REF_OUTP_CTL Register Bits

Bit	Name	Function
[5..0]	EXT_REF_OUT_MUX	These bits control the EXT_REF_OUT_MUX multiplexer. The output of this multiplexer is driven out of the external reference clock connector on the MCH face-plate. 0x01 – C19o 0x02 – #C16o 0x03 – C8/C32o 0x04 – #C4/C65o 0x05 – C2o 0x06 – C1.5o 0x07 – C3o 0x08 – C6/8.4/34/44o 0x09 – F16o 0x0B – PLL_REF0 0x0C – PLL_REF1 0x0D – EXTREF_IN 0x0E – TIC_100u 0x0F – RES (do not use!) 0x10 – RES (do not use!) 0x11 – SW_CLK 0x12 – SYNC_CLK 0x13 – 20MHz from Stratum 3 oscillator (only HW v2.3) 0x14 – Output of holdover function 0x21 – CLK2 of AMC1 0x22 – CLK2 of AMC2 : 0x2C – CLK2 of AMC12 0x2D – CLK1 Update (from 2nd MCH) 0x2E – CLK3 Update (from 2nd MCH)

		0x31 – CLK1 of AMC1 0x32 – CLK1 of AMC2 : 0x3C – CLK1 of AMC12 all other values result in no connection
6	HIGH-AMPL	**Selects the Amplitude of the Output signal** The CLK-Module output connects via two signals to the Base-Module, EXTREF_OUT_P and EXTREF_OUT_N (refer to Table 4:). If enabled, the selected signal is driven out via EXTREF_OUT_P. Depending on the HIGH-AMPL bit either the complementary of the selected signal or a "0" is driven out via EXTREF_OUT_N. Since there is an AC-coupling between the CLK-Module and the connector the complimentary signal results in higher amplitude of the output signal at the connector. Even if one contact of the connector is connected to ground on the cable side. 0 – low amplitude 1 – high amplitude
7	EN_OUTP	**Enables the output** 0 – disabled 1 – enabled

Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Zarlink, ZL30105 T1/E1/SDH Stratum 3 Redundant System Clock Synchronizer for AdvancedTCA™ and H.110, 11/05

Appendix B: Document's History

Revision	Date	Description	Author
1.0	12.02.2008	initial revision	ks
1.1	13.02.2008	Changed SYNC_CLK register description	ks
1.2	05.06.2008 12.08.2008	Added description of holdover function and external reference clock interface.	ks
1.3	02.10.2008	Added description of HCSL and M-LVDS differences and different ordering / assembly options Added PLL input and output frequencies to chapter 1	ks
14	10.11.2008	Added register description for External Reference Output Control	ks