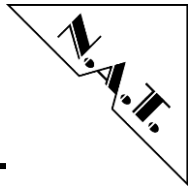
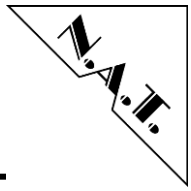


NAT-MCH
Clock-Module for Physics
Technical Reference Manual V 1.3
CLK-PHYS Module
HW Version 1.0



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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF5470
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)

1 Introduction

The **NAT-MCH** consists of the **NAT-MCH BASE-Module**, which can be expanded with additional PCBs. The **NAT-MCH BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **NAT-MCH BASE-Module** are:

- management of up to 12 AMCs, two cooling units (CUs) and one or more power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

To meet also the optional requirements of the MicroTCA specification, a **NAT-MCH CLK-Module** as well as a **NAT-MCH CLK-PHYS-Module** and different **NAT-MCH HUB-Modules** are available. With the **NAT-MCH CLK-PHYS-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs and a second MCH
- reception of clock signals from either of 12 AMCs, a second MCH or from the front panel input and redistribution

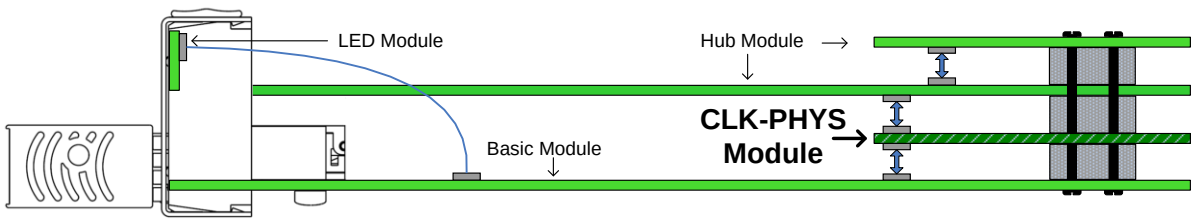
Through the extension of the **NAT-MCH** with a **NAT-MCH HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **NAT-MCH HUB-Module** that fits best to their applications. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express
  - Serial Rapid IO
  - 10Gigabit Ethernet

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH** is shown in *Figure 1*.

Figure 1: Arrangement of different NAT-MCH-Modules



This Technical Reference Manual describes the **NAT-MCH CLK-PHYS-Module**. With the **NAT-MCH CLK-PHYS-Module**, the 2nd tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed.

2 NAT-MCH CLK-PHYS Module Basics

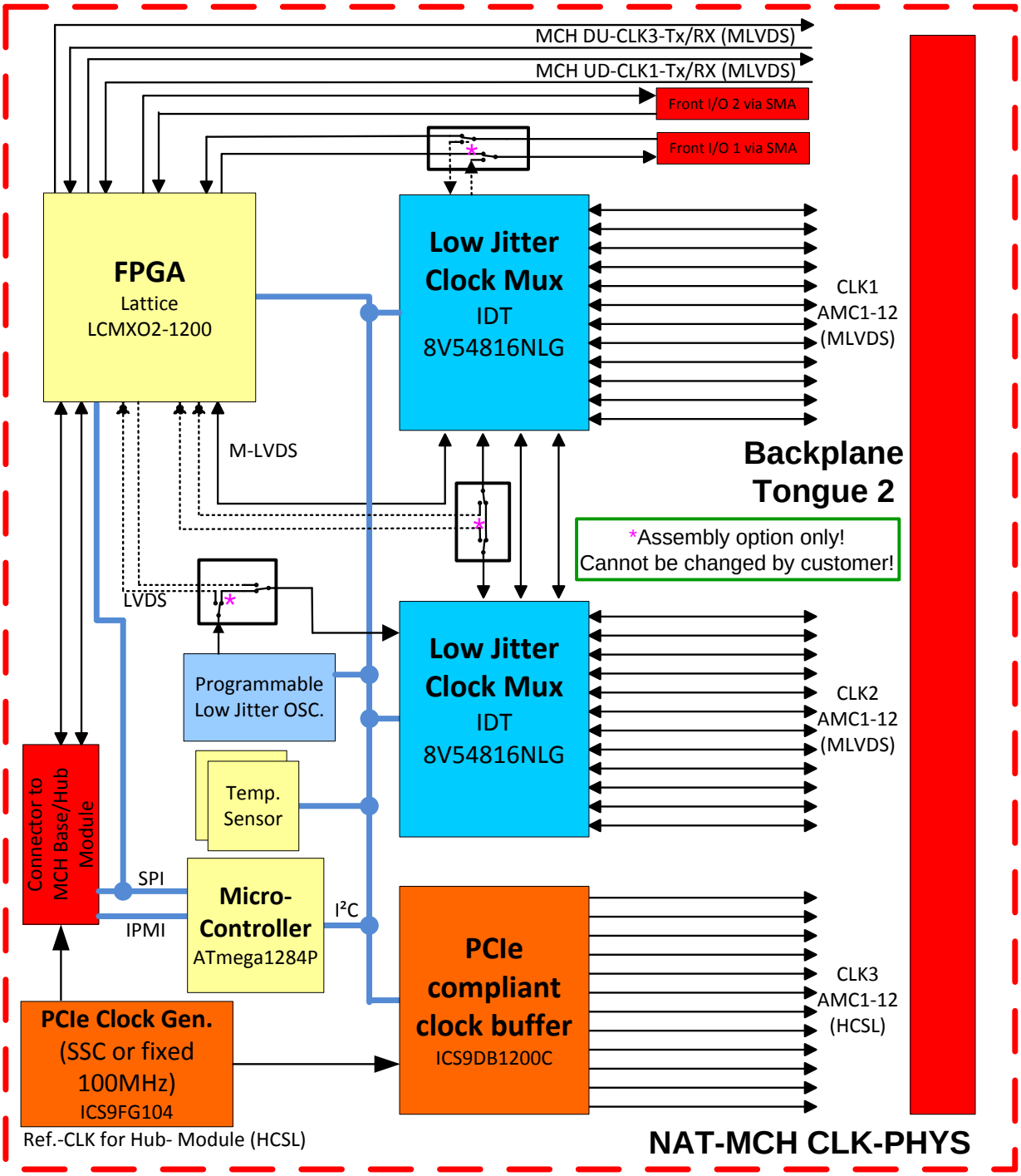
2.1 Major Features

- Multiplexing support of AMC clocks CLK1* and CLK2* for up to 12 AMCs
- support of update CLK1 and CLK3 for a second **NAT-MCH** in a redundant system
- support of two front panel reference clock I/O
- clock signals can be distributed over all backplane CLK1 and CLK2 connections and the front panel interface
- a PCI Express compliant clock signal can be distributed via CLK3 to all 12 AMCs

* Please refer to **Appendix A**: Correlation between MicroTCA and AMC Clock Naming for a brief description of the correlation between the MicroTCA and AMC clock interface naming

2.2 Block Diagram

Figure 2: NAT-MCH CLK-PHYS-Module – Block Diagram



2.3 Location Diagram

The following location diagrams show the position of important components. Depending on the chosen options it may be that the board does not include all components named in the location diagram.

Figure 3: NAT-MCH CLK-PHYS Module – Location Diagram (top)

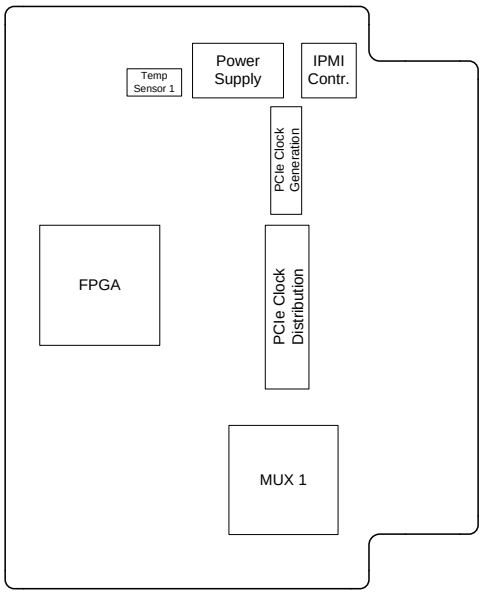
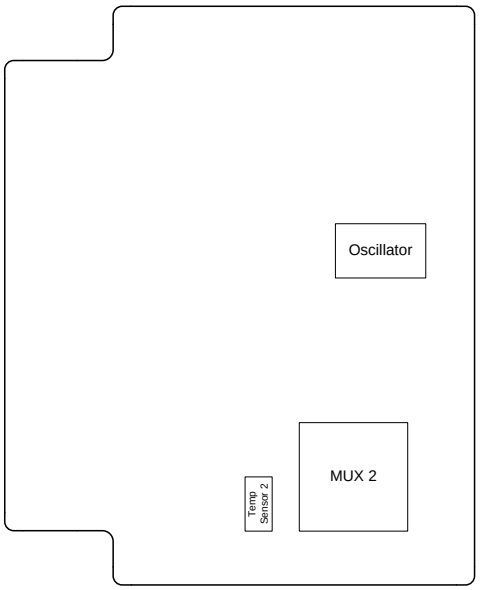


Figure 4: NAT-MCH CLK-PHYS Module – Location Diagram (bottom)



3 Functional Blocks

The **NAT-MCH CLK-PHYS-Module** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 Microprocessor

An Atmel 8-bit microprocessor resides on the **NAT-MCH CLK-PHYS-Module**. By this microprocessor, the main CPU of the base board can configure all multiplexers implemented in the FPGA and enable the transceivers for the connection to each AMC. The firmware can be updated by the CPU of the **NAT-MCH BASE-Module** via SPI interface. The base board CPU communicates with the **NAT-MCH CLK-PHYS-Module** via IPMI (using the I²C interface).

3.2 FPGA

To extend clock switching functionality of the multiplexing units the **NAT-MCH CLK-PHYS-Module** comes with a small Lattice FPGA. It can also be used to implement customized logic as frequency dividers or logic to generate pulses.

3.3 NAT-MCH CLK-PHYS-Multiplexing Function

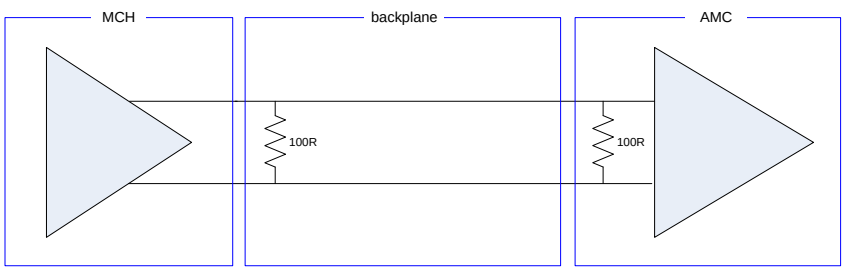
Two low jitter multiplexing units – MUX1 and MUX2 – are working on the **NAT-MCH CLK-PHYS-Module**. In combination with a Lattice FPGA they ensure flexible multiplexing of CLK1 and CLK2 from various AMCs, front input signals and a clock signal generated by a programmable low jitter oscillator.
The module offers obligatory connections as well as variable links determined by assembly-options. Please refer to the block diagram for detailed information.

3.4 M-LVDS / HCSL Transceiver

The MicroTCA R1.0 Specification recommends that all clock interfaces are equipped with M-LVDS compliant driver/receiver and termination. Contrary to that the AMC.0 R2.0 allows for FCLKA (formerly CLK3) also HCSL compliant driver/receiver and termination.

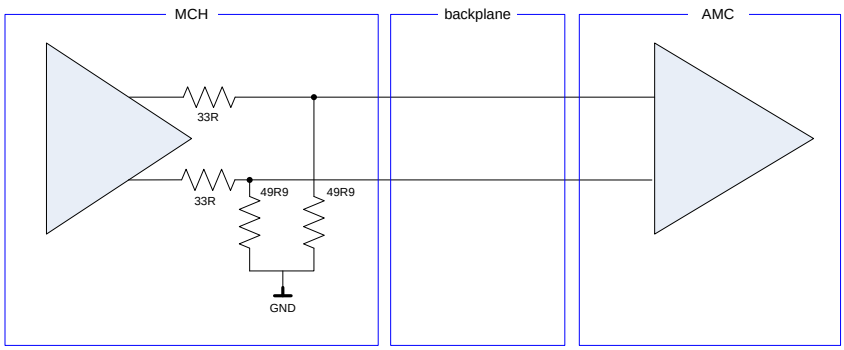
The main difference between the two signal specifications is the different termination. That makes it difficult to realize both with the same hardware; M-LVDS uses a dual differential termination between the two complimentary clock lines at both ends of the bus. This termination is shown in Figure 5.

Figure 5: M-LVDS-Termination



HCSL uses a source-only termination with two series and term-to-ground resistors. This termination is depicted in Figure 6.

Figure 6: HCSL-Termination



Please Note: It is important that not only the **NAT-MCH CLK-PHYS-Module** and the **AMC-Modules** fit together regarding the termination, also the backplane needs to be selected adequate.

The backplane shall have a 100Ohm termination if M-LVDS is used (refer to Figure 5); in case HCSL is used the backplane shall have no termination (refer to Figure 6).

3.5 PCIe compliant reference clock generation

If the **NAT-MCH** is equipped with a **NAT-MCH HUB-Module PCIe** the 100MHz PCIe reference clock is generated on the **NAT-MCH CLK-PHYS-Module** and passed to the **NAT-MCH HUB-Module**. In that case the **NAT-MCH CLK-PHYS-Module** will distribute that clock to all AMCs requesting a reference clock.

(In systems that follow the scope approach, the PCIe endpoints are connected directly via the backplane without using the switch on the **NAT-MCH**. In those systems often a PCIe reference clock is missing.)

3.6 Clock Interfaces

3.6.1 CLK-Interfaces

The **NAT-MCH CLK-PHYS-Module** implements clock interfaces to 12 AMCs.

3.6.1.1 CLK1 and CLK2

These interfaces can be used to send a clock signal to the AMCs, or to receive a reference clock signal from any of the 12 AMCs.

3.6.1.2 CLK3

The buffer device used here provides HCSL compliant outputs, as recommended for a PCIe reference clock.

3.6.2 Update-CLK

The **NAT-MCH CLK-PHYS-Module** implements 2 update channels (update CLK1 and CLK3). These channels are full-duplex connections to a second **NAT-MCH**. They can only be used to send and receive clock signals (not the PCI Express clock signal).

3.6.3 External Reference Clock Transceiver Module

The **NAT-MCH CLK-PHYS-Module** supports a dual external reference clock in- or output. Reference clock signals can be received or transmitted via connectors on the **NAT-MCH BASE-Module's** face plate.
Depending on the assembly option different external reference clock transceiver modules can be chosen. The available transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL) and the supported connector. At the moment the following external clock transceiver modules are available:

3.6.3.1 Coax-IO

The Coax-IO transceiver module supports two SMA connectors at the face plate. Each connector is connected to its independent amplifier circuit which can be configured as receiver or transmitter.

Configured as transmitter the output of the **NAT-MCH CLK-PHYS-Module** is connected to the SMA connector via an output amplifier that resides on the transceiver module.

A differential amplifier circuit comes into operation if configured as receiver. The receiver part is designed to be able to work with a wide range of input voltages, as well as signal forms (e.g. sine wave, rectangle...).
To be independent of any DC-offset the receiver part is also connected via AC-coupling.
The main part of the amplifier is a comparator that transfers the input signal from the SMA connector into a rectangle signal with a peak to peak voltage of 3.3V. Refer to Table 2: for the electrical characteristics.

Table 2: Coax-IO Electrical characteristics

Parameter	Min.	Typ.	Max.	Unit
Input Voltage peak to peak	0.3		5	V
Output Current		16		mA
Input Frequency	1		50M	Hz
Termination Resistance		50		Ω

SMA_CON1 is hardwired to the FPGA; SMA_CON2 is either hardwired to the FPGA as well or directly connected to MUX1 (assembly option, see block diagram).

3.6.3.2 RJ45-Clock

The RJ45 Clock uses the second RJ45 connector at the **NAT-MCH BASE-Module** face plate for the clock interface instead of the Ethernet uplink.

The following table shows how the contacts of the second RJ45 connector are assigned if the RJ45-Clock is used.

Table 3: 2nd RJ45-Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	N.C.	N.C.	2
3	Extref2_p	Extref1_p	4
5	Extref1_n	Extref2_n	6
7	N.C.	N.C.	8

The signals are directly connected to MLVDS compliant IOs of the **NAT-MCH CLK-PHYS-Module's** FPGA. To prevent damage, do not apply signals to this interface that are not compliant with the MLVDS signal standard.

3.6.3.3 Other External Reference Clock Transceiver Modules

Please contact N.A.T. GmbH if the available clock transceiver modules do not satisfy the needs for your application.

3.7 Interfaces to other NAT-MCH Modules

3.7.1 NAT-MCH BASE-Module

The Microprocessor on the **NAT-MCH CLK-PHYS-Module** can be programmed by the CPU on the **NAT-MCH BASE-Module** via a SPI interface. Normal communication between the Microprocessor and the CPU is done by IPMI messages via the I²C interface.

The external clock interface on the front panel is connected to the **NAT-MCH CLK-PHYS-Module** via the interface to the **NAT-MCH BASE-PCB** (via connector CON2).

3.7.2 NAT-MCH-HUB-Module PCIe

The **NAT-MCH CLK-PHYS-Module** can transmit a PCI Express compliant clock signal to the **HUB-Module**. This is only possible with the **NAT-MCH HUB-Module PCIe**.

3.8 Signal quality

Please regard that the best signal quality is achieved if the clock signal passes only one multiplexing unit, e.g. AMC12 CLK1 switched to AMC11 CLK1.

4 Hardware

4.1 Connectors

The following figures show the position of the different connectors of the **NAT-MCH CLK-PHYS-Module**.

Figure 7: NAT-MCH CLK-PHYS-Module – Connectors (top)

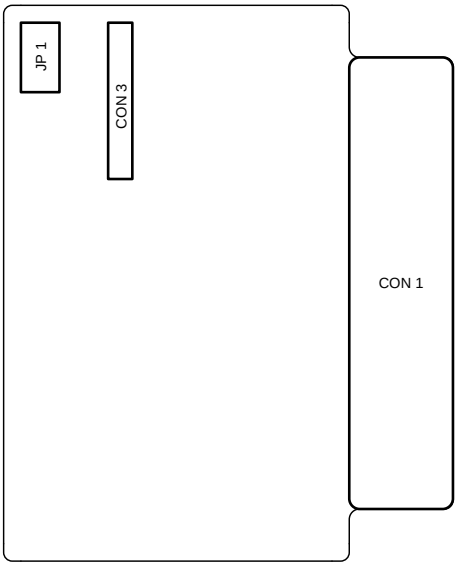
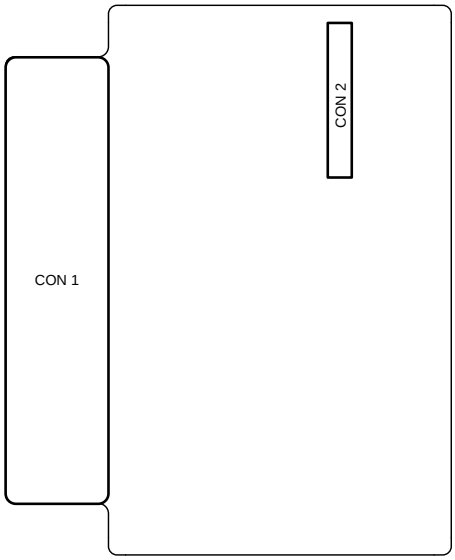


Figure 8: NAT-MCH CLK-PHYS-Module – Connectors (bottom)



Please refer to the following tables for the pin assignment of the **NAT-MCH CLK-PHYS-Module**.

4.1.1 CON1: NAT-MCH Connector

Table 4: CON1: MCH Connector – Pin Assignment

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	CLK3_Tx+	CLK3_Rx+	163
9	CLK3_Tx-	CLK3_Rx-	162
10	GND	GND	161
11	CLK1_Tx+	CLK1_Rx+	160
12	CLK1_Tx-	CLK1_Rx-	159
13	GND	GND	158
14	TxFB-1+	RxFB-1+	157
15	TxFB-1-	RxFB-1-	156
16	GND	GND	155
17	TxFB-2+	RxFB-2+	154
18	TxFB-2-	RxFB-2-	153
19	GND	GND	152
20	TxFB-3+	RxFB-3+	151
21	TxFB-3-	RxFB-3-	150
22	GND	GND	149
23	TxFB-4+	RxFB-4+	148
24	TxFB-4-	RxFB-4-	147
25	GND	GND	146
26	TxFB-5+	RxFB-5+	145
27	TxFB-5-	RxFB-5-	144
28	GND	GND	143
29	TxFB-6+	RxFB-6+	142
30	TxFB-6-	RxFB-6-	141
31	GND	GND	140
32	CLK3-1+	CLK3-7+	139
33	CLK3-1-	CLK3-7-	138
34	GND	GND	137
35	CLK3-2+	CLK3-8+	136
36	CLK3-2-	CLK3-8-	135
37	GND	GND	134
38	CLK3-3+	CLK3-9+	133
39	CLK3-3-	CLK3-9-	132
40	GND	GND	131
41	CLK3-4+	CLK3-10+	130
42	CLK3-4-	CLK3-10-	129
43	GND	GND	128
44	CLK3-5+	CLK3-11+	127
45	CLK3-5-	CLK3-11-	126
46	GND	GND	125
47	CLK3-6+	CLK3-12+	124

Pin #	MCH-Signal	MCH-Signal	Pin #
48	CLK3-6-	CLK3-12-	123
49	GND	GND	122
50	CLK1-1+	CLK2-1+	121
51	CLK1-1-	CLK2-1-	120
52	GND	GND	119
53	CLK1-2+	CLK2-2+	118
54	CLK1-2-	CLK2-2-	117
55	GND	GND	116
56	CLK1-3+	CLK2-3+	115
57	CLK1-3-	CLK2-3-	114
58	GND	GND	113
59	CLK1-4+	CLK2-4+	112
60	CLK1-4-	CLK2-4-	111
61	GND	GND	110
62	CLK1-5+	CLK2-5+	109
63	CLK1-5-	CLK2-5-	108
64	GND	GND	107
65	CLK1-6+	CLK2-6+	106
66	CLK1-6-	CLK2-6-	105
67	GND	GND	104
68	CLK1-7+	CLK2-7+	103
69	CLK1-7-	CLK2-7-	102
70	GND	GND	101
71	CLK1-8+	CLK2-8+	100
72	CLK1-8-	CLK2-8-	99
73	GND	GND	98
74	CLK1-9+	CLK2-9+	97
75	CLK1-9-	CLK2-9-	96
76	GND	GND	95
77	CLK1-10+	CLK2-10+	94
78	CLK1-10-	CLK2-10-	93
79	GND	GND	92
80	CLK1-11+	CLK2-11+	91
81	CLK1-11-	CLK2-11-	90
82	GND	GND	89
83	CLK1-12+	CLK2-12+	88
84	CLK1-12-	CLK2-12-	87
85	GND	GND	86

4.1.2 CON2: Interface to NAT-MCH BASE-Module

Connector CON2 connects the **NAT-MCH CLK-PHYS-Module** with the **BASE-Module.**

Table 5: CON2: Connector to NAT-MCH BASE-Module – Pin Assignment

Pin #	Signal	Signal	Pin #
1	/SPISEL_CLKPCB	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_OUT_P	+3.3V MP	14
15	EXTREF_OUT_N	SPICLK	16
17	GND	EXTREF_IN	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUB PCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

4.1.3 CON3: Interface to NAT-MCH HUB-Module

Connector CON3 connects the **NAT-MCH CLK-PHYS-Module** with a **NAT-MCH HUB-Module**.

Table 6: CON3: Connector to NAT-MCH HUB-Module – Pin Assignment

Pin #	Signal	Signal	Pin #
1	N.C.	INT_HUB	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_P	+3.3V MP	14
15	PCIeCLK_N	SPICLK	16
17	GND	expansion3	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	nRESET_CLK-PCB	24
25	SDA	nRESET_HUB-PCB	26
27	GND	GND	28

5 Programming Notes

5.1 SPI Interface

The SPI interface on the **NAT-MCH CLK-PHYS-Module** is used only for maintenance purposes, e.g. updating the microcontroller firmware or the FPGA image.

5.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **NAT-MCH BASE-Module**. All communication is based on IPMI Messages.

5.3 Register and signal mapping

The **CLK-PHYS-Module** can generate, receive and transmit various clock signals.

Different clock signals can be received by the **CLK-PHYS-Module** via interfaces at the **NAT-MCH BASE-Module's** face plate or the backplane interfaces, e.g. CLK1/2 connected to AMCs as well as CLK1/3_UD connected to a redundant **NAT-MCH**. The signal mapping of the multiplexer ports is described in the following tables:

Table 7: MUX1 – Signal Mapping

MUX Port	Mapped to
0	Front SMA – CLK 1
1	MUX Interconnect 1
2	MUX Interconnect 2
3	FPGA **or** MUX Interconnect 3*
4	AMC 12 – CLK 1
5	AMC 11 – CLK 1
6	AMC 10 – CLK 1
7	AMC 9 – CLK 1
8	AMC 8 – CLK 1
9	AMC 7 – CLK 1
10	AMC 6 – CLK 1
11	AMC 5 – CLK 1
12	AMC 4 – CLK 1
13	AMC 3 – CLK 1
14	AMC 2 – CLK 1
15	AMC 1 – CLK 1

* assembly option

Table 8: MUX2 – Signal Mapping

MUX Port	Mapped to
0	AMC 2 – CLK 2
1	AMC 3 – CLK 2
2	AMC 4 – CLK 2
3	AMC 5 – CLK 2
4	AMC 7 – CLK 2
5	MUX Interconnect 1
6	MUX Interconnect 2
7	AMC 8 – CLK 2
8	AMC 9 – CLK 2
9	AMC 10 – CLK 2
10	AMC 11 – CLK 2
11	AMC 12 – CLK 2
12	OSC **or** FPGA Interconnect*
13	FPGA **or** MUX Interconnect 3*
14	AMC 6 – CLK 2
15	AMC 1 – CLK 2

* assembly option

Please note that the mapping determined by assembly option cannot be changed by the customer!
For further information on how to change the signal mapping by clock script please refer to the **NAT-MCH BASE-Module** manual, chapter "Programming Notes".

Additionally the **NAT-MCH CLK-PHYS-Module** can generate clock signals on its own. Therefore a low jitter programmable oscillator resides on the module which can generate various frequencies depending on assembled type and programming.

Beside receiving or generating clock signals the **NAT-MCH CLK-PHYS-Module** is also able to transmit clock signals. This can be done by the backplane interfaces (CLK1/2/3 and CLK1/3_UD) as well.

The multiplexing units and other functions implemented on the **NAT-MCH CLK-PHYS-Module** can be controlled by a register interface. The following tables are showing a detailed description of the registers that are available. These registers are not intended to be used by the customer. N.A.T. offers a script based configuration interface that simplifies the complex configuration options. Please refer to chapter "**CLK-Module** Configuration" of the **NAT-MCH** User's Manual for a more detailed description of this interface.

Table 9: Register overview

	7	6	5	4	3	2	1	0
0x00	BOARD_ID							
0x01	PCB_VERS							
0x02	FW_VERS							
0x03	FPGA_VERS							
0x10-0x1F	MUX1_PORT-CTRL							
0x20-0x2F	MUX2_PORT-CTRL							

5.3.1 BOARD_ID – 0x00

Bit	Name	Description	Default	Access
7..0	BOARD_ID	The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH CLK-PHYS-Module.**	0xB4	Read Only

5.3.2 PCB_VERS – 0x01

Bit	Name	Description	Default	Access
7..4	PCB_VERS_MAJ	The PCB Version Register contains the version code of the **NAT-MCH CLK-PHYS-Module.** Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the PCB version is e.g. v3.1 the PCB Version Register contains the value 0x31.	0xXX	Read Only
3..0	PCB_VERS_MIN		0xXX	Read Only

5.3.3 FW_VERS – 0x02

Bit	Name	Description	Default	Access
7..4	FW_VERS_MAJ	The Atmel Version Register contains the version of the Atmel firmware. Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the firmware running on the Atmel is v1.3 the Firmware Version Register contains the value 0x13.	0xXX	Read Only
3..0	FW_VERS_MIN		0xXX	Read Only

5.3.4 FPGA_VERS – 0x03

Bit	Name	Description	Default	Access
7..4	FW_VERS_MAJ	The FPGA Version Register contains the version code of the Altera FPGA. Bit 7 to 4 contain the major version and bit 3 to 0 contain the minor version. That means if the FPGA is running with the image v1.3 the FPGA Version Register contains the value 0x13.	0xXX	Read Only
3..0	FW_VERS_MIN		0xXX	Read Only

5.3.5 MUX1_PORT_CTRL – 0x10-0x1F

These registers are used for port configuration of MUX1. MUX2 is assigned identically, so the following tables are valid for MUX2 as well (register 0x20-0x2F).

Register	Interface
0x10	Port 0 - Configuration
0x11	Port 1 - Configuration
0x12	Port 2 - Configuration
0x13	Port 3 - Configuration
0x14	Port 4 - Configuration
0x15	Port 5 - Configuration
0x16	Port 6 - Configuration
0x17	Port 7 - Configuration
0x18	Port 8 - Configuration
0x19	Port 9 - Configuration
0x1A	Port 10 - Configuration
0x1B	Port 11 - Configuration
0x1C	Port 12 - Configuration
0x1D	Port 13 - Configuration
0x1E	Port 14 - Configuration
0x1F	Port 15 - Configuration

The following table shows a detailed description of MUX1_Port0 configuration. As all ports are assigned identically the information is valid for ports 1-15 as well.

Bit	Name	Description	Default	Access
7	MUX1_PORT0_CFG	Port I/O configuration Bit = 0 => port configured as INPUT Bit = 1 => port configured as OUTPUT	0x00	Read/Write
6	MUX1_PORT0_TERM	Termination enable Bit = 0 => termination OFF (high impedance) Bit = 1 => termination ENABLED	0x00	Read/Write
5	MUX1_PORT0_POL	Output polarity inversion Bit = 0 => NON-inverted polarity Bit = 1 => inverted polarity	0x00	Read/Write
4	MUX1_PORT0_RES	Reserved	0x00	Read/Write
3..0	MUX1_PORT0_OUTSEL	Output port select [3…0] Port outputs the signal present at port defined by Bits [3..0]	0x00	Read/Write

6 Board Specification

Table 10: NAT-MCH CLK-PHYS Module Features

Power Consumption	12V / 0.5A max. (only **NAT-MCH CLK-PHYS-Module**)
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 2.0 IPMI Specification v2.0 Rev. 1.0

For detailed information on Jitter performance, refer to Appendix B.

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH CLK-PHYS-Module** during its usual life-time take refer to the safety note section of the **NAT-MCH BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up, check this section for installation prerequisites and requirements!

7.2.1 Requirements

The **NAT-MCH CLK-PHYS-Module** is always mounted on a **NAT-MCH BASE-Module**. Therefore please refer to the requirements section of the **NAT-MCH BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH CLK-PHYS-Module** must meet the following specifications:

- +12 V / 0.5 A max. (only **NAT-MCH CLK-PHYS-Module**, in addition to other PCBs of the **NAT-MCH**).

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

Appendix A: Correlation between MicroTCA and AMC Clock Naming

The AMC.0 Rev.1.0 as well as the MicroTCA Rev.1.0 have defined three clock interfaces that can be used to for clock distribution purposes. These interfaces are named CLK1, CLK2 and CLK3. With the new AMC.0 V2.0 specification the clocks have been renamed as well as additional clocks were defined.

Which clock of an AMC is connected to which clock of the MCH depends on the connections that are made by the backplane. That means it must not necessarily be that TCLKA of an AMC is always connected to CLK1 of the MCH. Even though, this is the standard way for a non-redundant MicroTCA Backplane.

Table 11: shows the correlation between the MicroTCA/AMC.0 Rev. 1.0 and the AMC.0 Rev. 2.0 naming.

Table 11: Correlation between MicroTCA and AMC Clock Naming

MicroTCA/AMC.0 Rev. 1.0	AMC.0 Rev. 2.0	Description
CLK1	TCLKA	Telecom Clock A
CLK2	TCLKB	Telecom Clock B
CLK3	**FCLKA**	**Fabric Clock**
X	TCLKC	Telecom Clock C
X	TCLKD	Telecom Clock D

Please refer to the AMC.0 Rev. 2.0 specification for a more detailed description of the single clock signals and their intended purpose.

Since the MicroTCA specification defines the MCH this manual is using the names that are defined by the MicroTCA.

Appendix B: Jitter performance

This appendix gives some basic values regarding the achievable jitter performance. Please note that here no simple "one number value" can be given as there are many ways to measure jitter and as the total performance of a clock path also depends on components like the backplane, the used power supply, AMC modules, etc.

The values and measurements provided below where taken by IDT. They represent the performance of the multiplexer chips when using them to connect a clock signal coming into one port to one of the output ports. Values for further scenarios will follow up in the future.

Input was CLK6, measurement taken on CLK9, all other ports configured as output; signal frequency was 125 MHz.

The results are:
Input: 56.6 fs RMS (integrated over 12 kHz – 20 MHz)
Output: 349.4 fs RMS
Additive jitter: (square root of difference of squares): 344.8 fs

Figure 9: Phase Noise Plot of Input Signal

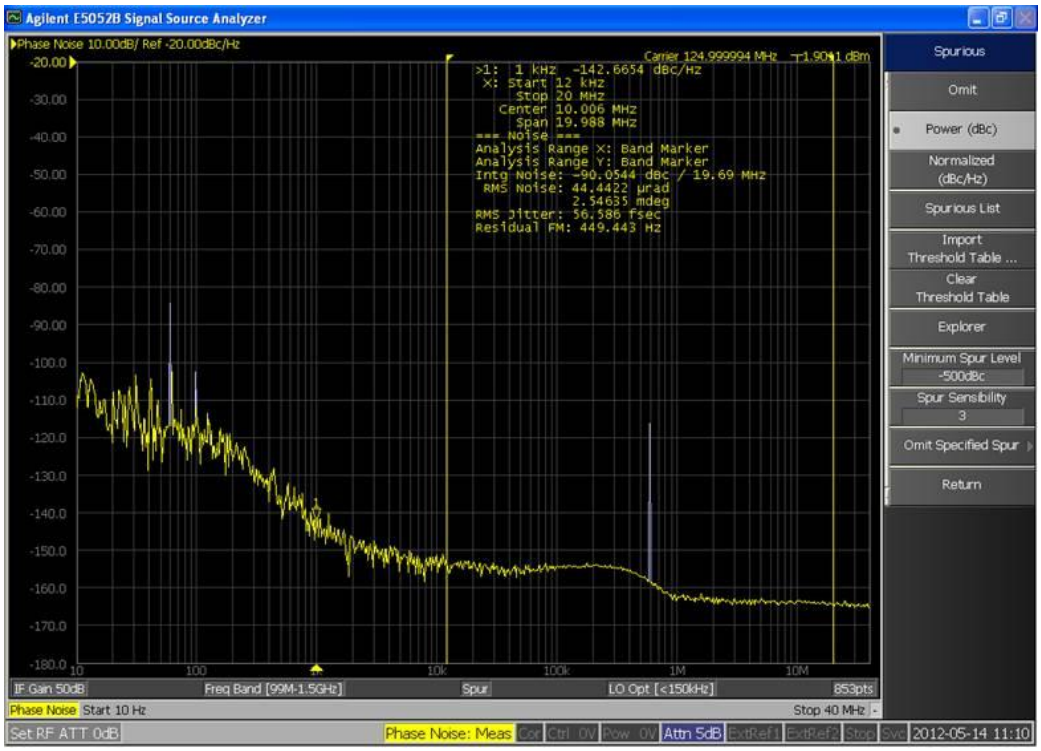
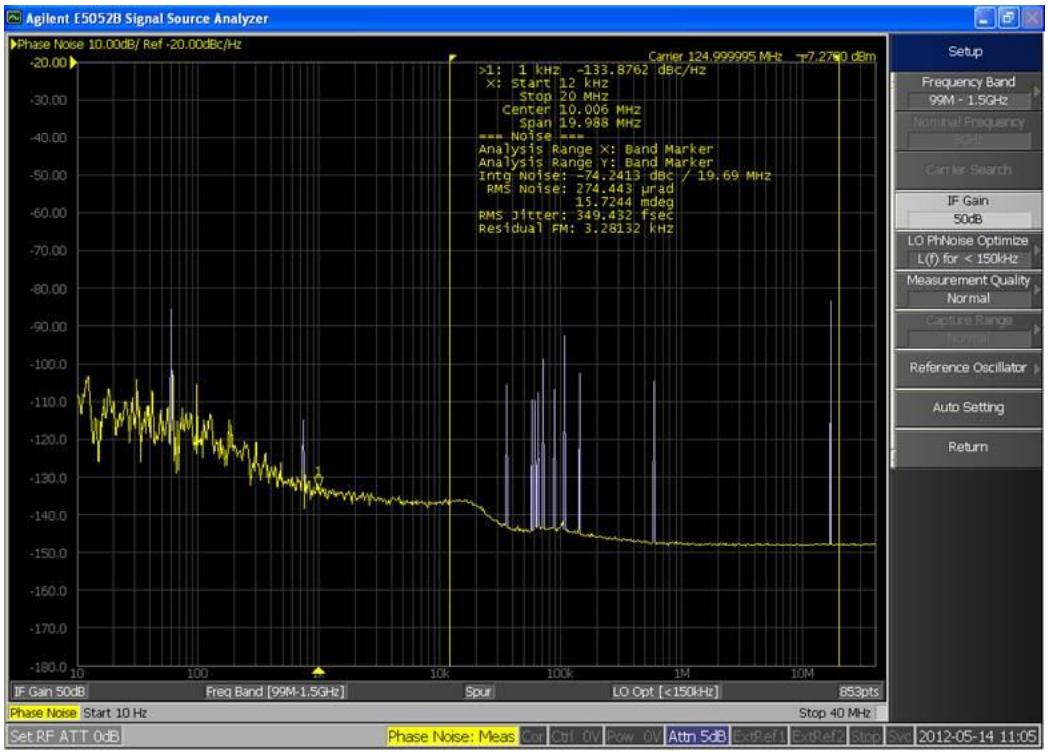


Figure 10: Phase Noise Plot of Output Signal



Appendix C: Reference Documentation

[1] IDT ICS9DB1200CTwelve Output Differential Buffer for PCIe Gen1/Gen2, 09/08
http://www.idt.com/products/getDoc.cfm?docID=18459714
[2] IDT ICS9FG104 programmable FTG for differential P4™ CPU, PCIe Clocks, 02/07
http://timing.idt.com/datasheets/ics9FG104.pdf

Appendix D: Document's History

Revision	Date	Description	Author
1.0		initial revision	se/te
1.1		No changes in contents, formatting corrections	se
1.2		Corrections block diagram	te
1.3	21.11.2013	Adaption to new layout. Typo correction	se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	SE