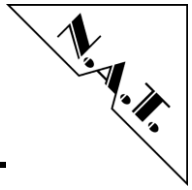
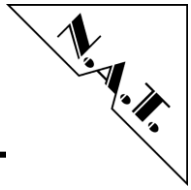


NAT-JSM
JTAG Switch Module
Technical Reference Manual V1.4
HW Revision 1.1



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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
FPGA	Field Programmable Gate Array
I/O	Input/Output
JSM	JTAG Switch Module
JTAG	Joint Test Action Group
LED	Light Emitting Diode
µTCA/MTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
SMP	Shared Management Power
TAP	Test Access Port
USB	Universal Serial Bus
XVC	Xilinx Virtual Cable

1 Introduction

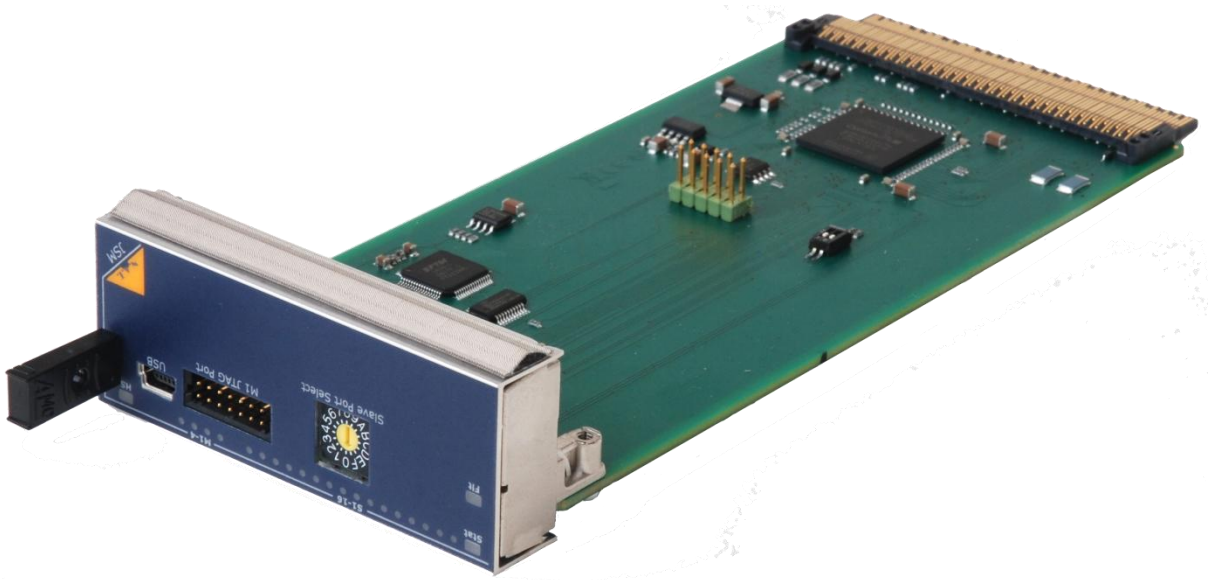
The **NAT-JSM** is an MTCA compliant JTAG switch module with a flexible design that makes it compatible with most of todays MTCA chassis providing a JSM slot.
The module detects whether it is inserted into an AMC, MCH or JSM slot; only if a JSM slot is detected the output drivers are turned on. The only prerequisite for misinsertion protection is that the pinout of the JSM-Connector follows the basic rules of the AMC-Connector.

The **NAT-JSM** can be adapted to nearly any existing JSM system connector by configuration of the onboard FPGA as long as it is based on the AMC-Connector layout.

By default the **NAT-JSM** automatically arbitrates the JTAG master port, the slave port is selected by the TAP controller. The automatic configuration can be overruled at any time by manual configuration through front panel elements.

The following figure shows a photo of the **NAT-JSM**.

Figure 1: NAT-JSM



2 Overview

2.1 Major Features

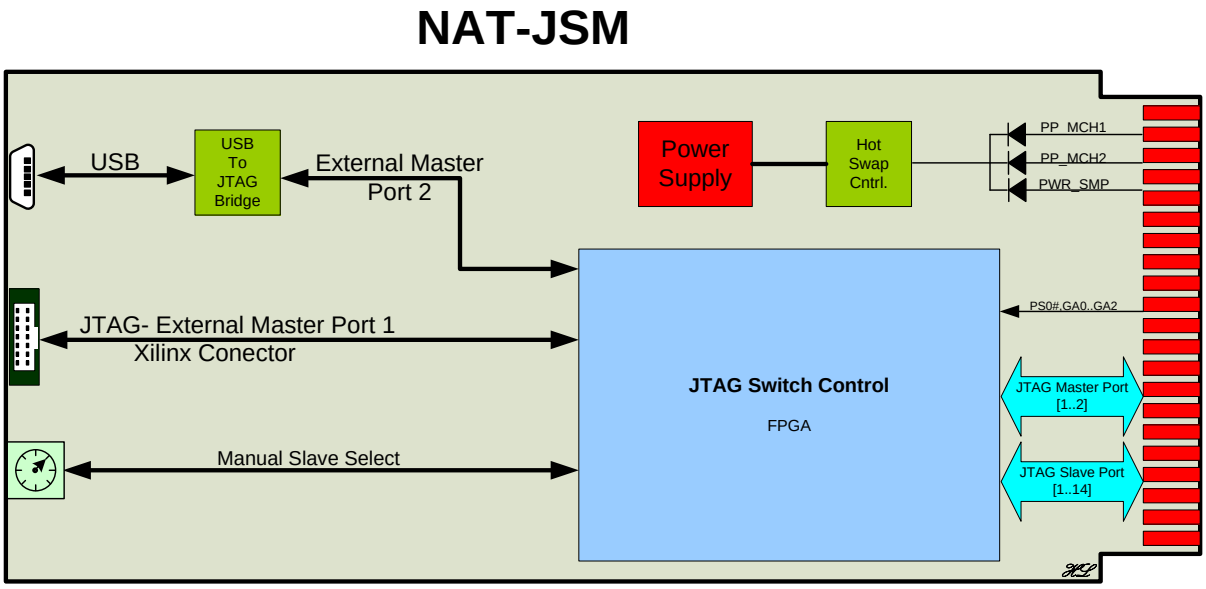
- JTAG download from MCH via WEB Interface
- JTAG programming connector at front panel
- Automatic arbitration between JTAG Masters
- Target selection through JTAG information
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Multiple JSM Pinout configurations via FPGA
- Power supply through MCH power channels or power module SMP power
- Minimal power consumption

For detailed description see the following chapter.

2.2 Block Diagram

The following figure shows a block diagram of the **NAT-JSM** board.

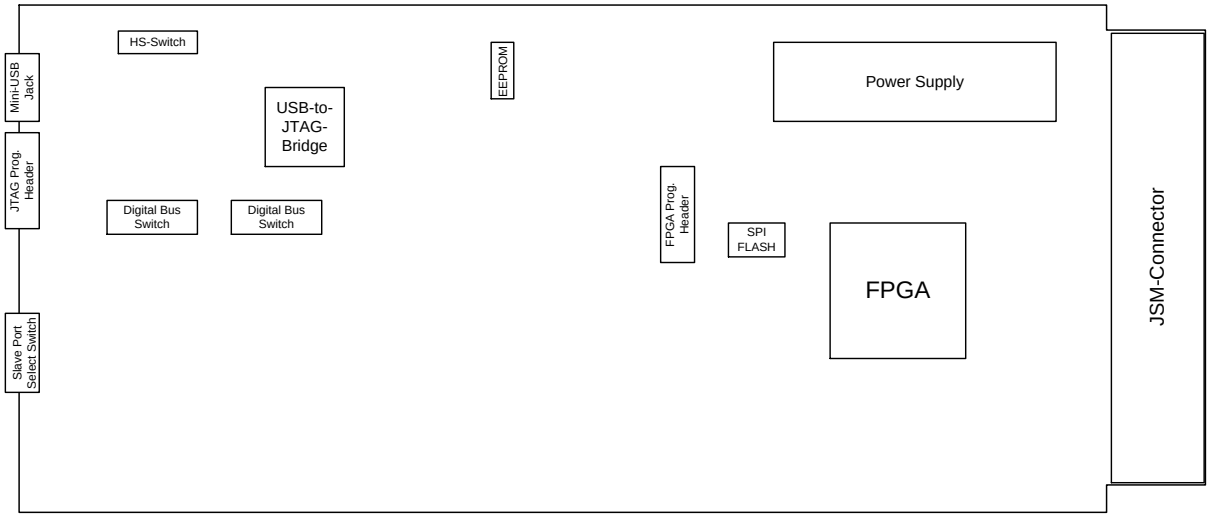
Figure 2: NAT-JSM – Block Diagram – Overview



2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: NAT-JSM – Location Diagram – Overview



3 Programming Interfaces

The NAT-JSM per default performs an automatic arbitration for the various JTAG master ports. This is means the module switches its master ports input to that master port last seen activity on.

3.1 Pin-Header Programming Interface

The NAT-JSM provides a XILINX compatible 14 pin programming header at the face plate.
With a standard XILINX programming adapter the resources in a MTCA system can be programmed or debugged.
The Interface has been tested successfully with

- Xilinx – Platform Cable USB II

The programming target is selected by the rotary switch.

3.2 USB Programming Interface

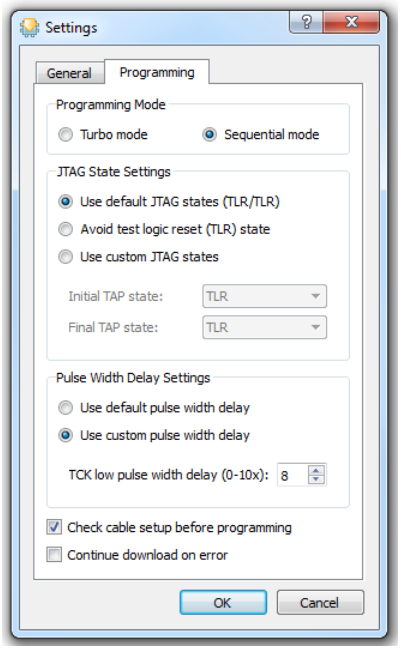
The standard USB connector at the face plate serves as programming connector for common programming adapters from various vendors. To make usage of this programming interface the software driver of the respective tool should support programming interfaces based on the FTDI FT2232 USB-to-JTAG chip.
The Interface has been tested successfully with

- Lattice – Diamond Programmer 3.0

The programming target is selected by the rotary switch or it can be selcted via the webinterface of the NAT-MCH.

In the Lattice Diamond Programmer software the "Detect Cable" function can be used to get access to the USB-to-JTAG bridge device.
Depending on the trace lengths and the used MTCA chassis it might be necessary to reduce the standard JTAG clock frequency from about 15MHz to values below 8MHz. This can be done in the "Settings" dialog under "Edit" -> "Settings" in the "Programming" tab. Here the radiobutton "Use custom pulse width delay" must be activated and the a reduction of the TCK frequency can be enabled.

Figure 4: Lattice Diamond Settings Dialog



3.3 Programming via MCH

The NAT-MCH provides TCP/IP based communicating interface for NAT-JSM. This is new server side application running on NAT-MCH to support Xilinx Virtual Cable (XVC) Protocol. Because the NAT-MCH is connected to the NAT-JSM board, the Xilinx client software has available the JTAG access to the programming targets, that are described in the *3.4 Target Selection*

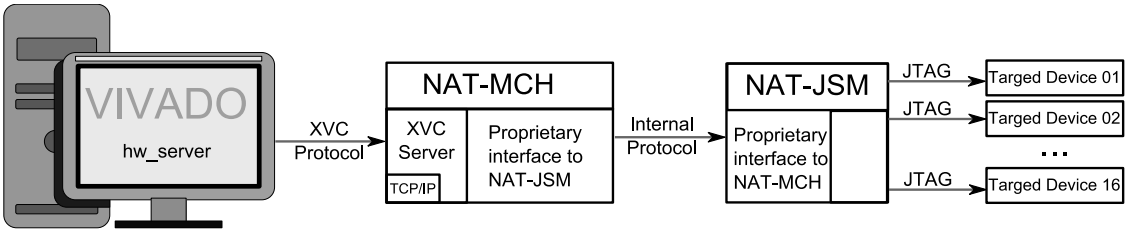
The NAT-MCH offers 16 TCP ports for 16 programming targets. The first TCP port named *Base Port* is tuneable and can be set/save by user. The other fifteen ports are automatically selected by incrementing the Base Port number. Therefore, each programming target becomes dedicated TCP port to be programmed by client software. To view the mapping between TCP port and programming target, use, please, the menu *JTAG JSM* of the web interface on the NAT-MCH.

3.3.1 Programming via Xilinx Vivado Software

The Vivado® design tools include the support of XVC protocol that allow communicating JTAG commands over IP to an embedded system so that a target Xilinx FPGA can be programmed and/or debugged. Therefore, the NAT-MCH parses the IP packets with a TCP/IP connection and converts the packets into JTAG command. After the packets are processed, the NAT-MCH communicates with NAT-JSM board over internal protocol. The NAT-JSM switches the connection to the target device and provides logical connection

between XVC server and target FPGA. Figure 5: illustrates high-level block diagram of a typical XVC topology

Figure 5: Block Diagram of XVC Topology for Programming via MCH



To initiate connection, please, open Vivado Hardware Manager. Then start a Hardware Server session with following command in the Tcl Console:

>> connect_hw_server

After that, open hardware target with following command in the Tcl Console:

>> open_hw_target -xvc_url <IP_Address>:<TCP_Port>

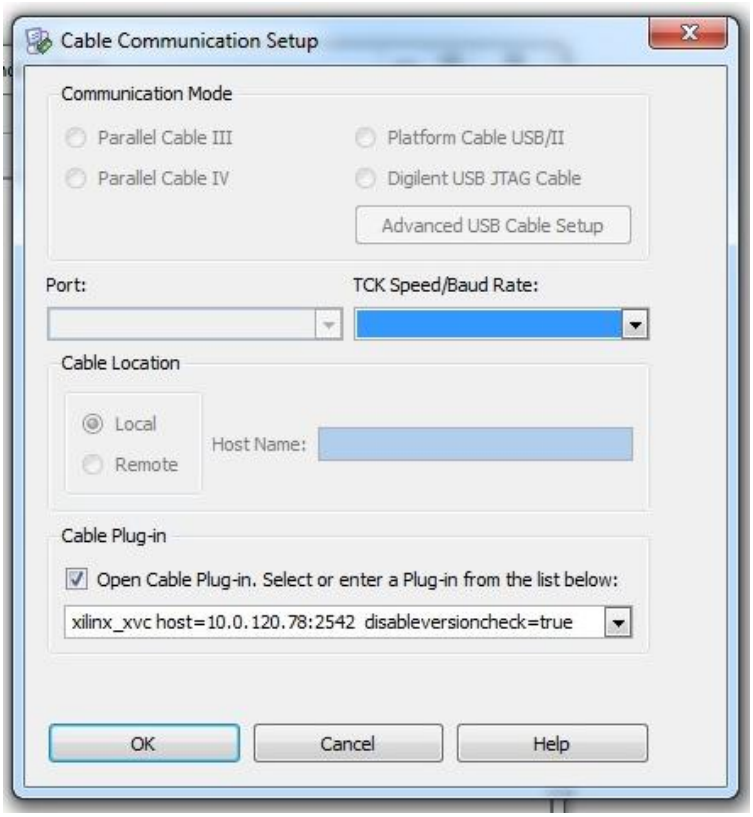
Where <IP_Address> is IP address of a NAT-MCH and <TCP Port> is TCP port assigned to particular target device [3].

3.3.2 Programming via Xilinx iMPACT Software

As alternative to the Xilinx Vivado® design tools (these support only 7-series and newer devices) the older Xilinx iMPACT Software is also capable of using the XVC protocol.
To do so, select in the "Cable Communication Setup" und "Output" -> "Cable Setup" the checkbox for "Cable Plug-in". In the text field enter the following:

Xilinx_xvc host=<IP_Address>:<TCP_Port> disableversioncheck=true

Figure 6: iMPACT Cable Communication Setup Dialog



3.4 Target Selection

When programming via one of the front interfaces, the programming target (JTAG Slave Port) can be selected by the rotary switch at the face plate:

Table 2: Rotary Switch / Slave-LED – Channel-Assignment

Rotary Switch Value	Selected Target (Slave Port)	Slave LED
0	AMC 1	1
1	AMC2	2
2	AMC3	3
3	AMC 4	4
4	AMC 5	5
5	AMC 6	6
6	AMC 7	7
7	AMC 8	8
8	AMC 9	9
9	AMC 10	10
A	AMC 11	11
B	AMC 12	12
C	Power Module 1	13
D	Power Module 2	14
E	MCH 1	15
F	MCH 2	16

Alternatively the target can be selected via the WEB interface, which overrules the rotary setting.

3.5 Master Selection

The JTAG Master port is automatically selected upon clock activity on one of the four master ports:

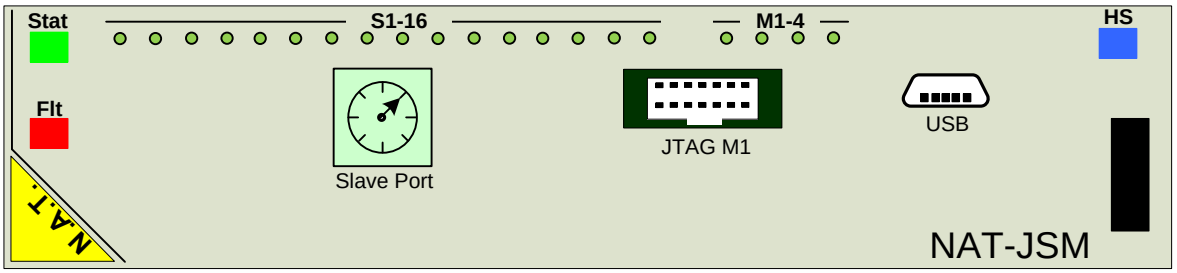
Table 3: Master-LED – Channel-Assignment

Master LED	Active Master
1	Face Plate Header M1
2	Onboard FTDI USB-JTAG Chip
3	MCH 1
4	MCH 2

3.6 Front Panel and LED

The **NAT-JSM** module is equipped with 16 green LEDs (S1-S16) indicating the chosen JTAG slave port; another 4 green LEDs (M1-M4) show the selected JTAG master port.

Figure 7: NAT-JSM – Front Panel View



Additionally the module contains the standard AMC LEDs consisting of a red Fault Indication LED, a General Purpose status LED and the Hot-Swap handle with the corresponding blue LED.

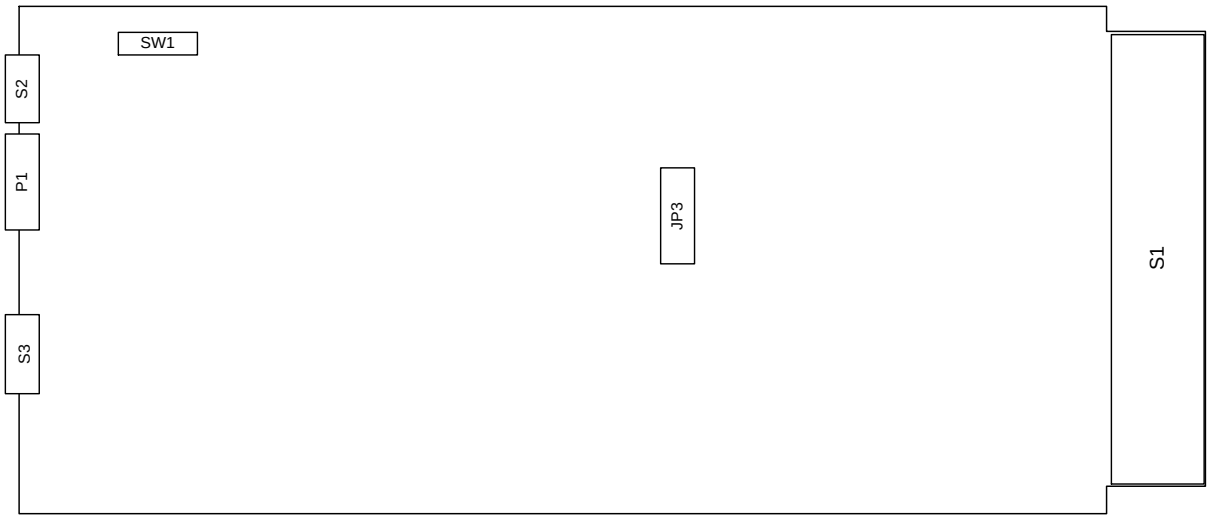
The Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

Although optically appearing as one LED, the General Purpose LED physically consists of two LEDs (green and orange) sharing the same hole in the Front Plate.
The LEDs have the following functionality:

Green LED on	: idle/ready state
Green blinking	: transfer in progress
Yellow LED on	: JTAG failure

3.7 Connectors and Switches

Figure 8: NAT-JSM – Connector and Switch Location – Overview



Please refer to the following tables to look up the connector and switch pin assignment of the **NAT-JSM**.

3.7.1 S1: JSM Connector

Table 4: S1: JSM Connector – Pin-Assignment

Pin #	JSM-Signal	JSM-Signal	Pin #
1	GND	GND	170
2	PP_MCH1	STCK1	169
3	IO_1 (PS1#) (*)	STMS1	168
4	3.3V (MP)	STDI1	167
5	GA0	STDO1	166
6	IO_2 (ETH) (*)	STRST#1	165
7	GND	GND	164
8	IO_3 (ETH) (*)	STCK2	163
9	PP_MCH1	STMS2	162
10	GND	GND	161
11	TCK1	STDI2	160
12	TMS1	STDO2	159
13	GND	GND	158
14	TDI1	STRST#2	157
15	TDO1	STCK3	156
16	GND	GND	155
17	GA1	STMS3	154
18	NC (PWR)	STDI3	153
19	GND	GND	152
20	TRST#1	STDO3	151
21	TMREQ#1	STRST#3	150
22	GND	GND	149
23	TCK2	STCK4	148
24	TMS2	STMS4	147
25	GND	GND	146
26	GA2	STDI4	145
27	PWR_SMP	STDO4	144
28	GND	GND	143
29	TDI2	STRST#4	142
30	TDO2	STCK5	141
31	GND	GND	140
32	TRST#2	STMS5	139
33	TMREQ#2	STDI5	138
34	GND	GND	137
35	PMTCK1	STDO5	136
36	PMTMS1	STRST#5	135
37	GND	GND	134
38	PMTDI1	STCK6	133
39	PMTDO1	STMS6	132
40	GND	GND	131
41	IO_4 (ENABLE#) (*)	STDI6	130
42	NC (PWR)	STDO6	129
43	GND	GND	128
44	PMTRST#1	STRST#6	127

Pin #	JSM-Signal	JSM-Signal	Pin #
45	PMTCK2	STCK7	126
46	GND	GND	125
47	PMTMS2	STMS7	124
48	PMTDI2	STDI7	123
49	GND	GND	122
50	PMTDO2	STDO7	121
51	PMTRST#2	STRST#7	120
52	GND	GND	119
53	PMTCK3	STCK8	118
54	PMTMS3	STMS8	117
55	GND	GND	116
56	IO_5 (SCL_L) (*)	STDI8	115
57	NC (PWR)	STDO8	114
58	GND	GND	113
59	PMTDI3	STRST#8	112
60	PMTDO3	STCK9	111
61	GND	GND	110
62	PMTRST#3	STMS9	109
63	PMTCK4	STDI9	108
64	GND	GND	107
65	PMTMS4	STDO9	106
66	PMTDI4	STRST#9	105
67	GND	GND	104
68	PMTDO4	STCK10	103
69	PMTRST#4	STMS10	102
70	GND	GND	101
71	IO_6 (SDA_L) (*)	STDI10	100
72	PP_MCH2	STDO10	99
73	GND	GND	98
74	NC (TCLKA+)	STRST#10	97
75	STCK12	STCK11	96
76	GND	GND	95
77	STMS12	STMS11	94
78	STDI12	STDI11	93
79	GND	GND	92
80	STDO12	STDO11	91
81	STRST#12	STRST#11	90
82	GND	GND	89
83	PS0#	NC (RX8+)	88
84	NC (PWR)	NC (RX8-)	87
85	GND	GND	86

(*) unused IO pins, name in () refer to the original usage at AMC connector

3.7.2 S2: Mini-USB Connector

The Mini-USB-Connector S2 provides a direct connection to the on-board USB-to-JTAG-Bridge.

Table 5: S2: Mini-USB Connector – Pin-Assignment

Pin#	Signal	Signal	Pin No.
1	VCC	D-	2
3	D+	nc	4
5	GND	SGND	6
7	SGND	SGND	8

3.7.3 JP3: FPGA Programming Header

Pin Header JP3 offers a FPGA programming interface via Altera Active-Serial-Header.

Table 6: JP3: FPGA Programming Header – Pin-Assignment

Pin#	Signal	Signal	Pin No.
1	DCLK_EP	GND	2
3	CONF_DONE	+3.3V	4
5	nCONFIG	nCE	6
7	DATA0_EP	nCS0	8
9	ASDI	GND	10

3.7.4 P1: JTAG Programming Header

The JTAG Programming Header P1 is located at the front plate. It is the commonly used JTAG programming interface using a 7x2 pin header with 2mm pitch.

Table 7: P1: JTAG Programming Header – Pin-Assignment

Pin#	Signal	Signal	Pin No.
1	GND	+3.3V	2
3	GND	FR_TMS	4
5	GND	FR_TCK	6
7	GND	FR_TDO	8
9	GND	FR_TDI	10
11	GND	nc	12
13	GND	FR_SRST	14

3.7.5 SW1: Hot Swap Switch

Switch SW1 is used to support hot swapping of the module.

4 Board Specification

Table 8: NAT-JSM Features – Overview

FPGA	Altera Cyclone3
JSM-Module	Single Full Size
Front-I/O	Mini-USB for USB-to-JTAG-Bridge JTAG-Programming Header
Power Supply	12V / 0.2A
Environmental Conditions	Operating: 0-60°C Storage: -40°C-85°C Humidity: 10%-90% non-condensing

5 Installation

5.1 Safety Note

To ensure proper functioning of the **NAT-JSM** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAT-JSM** read this installation section
- Before installing or uninstalling the **NAT-JSM**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAT-JSM** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power
  - Take those steps
  - Finally turn on or off the power if necessary
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAT-JSM** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

5.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

5.2.1 Requirements

The installation requires only:

- a µTCA backplane with matching JSM pinout for connecting the **NAT-JSM**
- power supply
- cooling devices

5.2.2 Power supply

The power supply for the **NAT-JSM** must meet the following specifications:

- required for the module: +12V / 0.2A max.

5.3 Statement on Environmental Protection

5.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

5.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

5.3.3 Compliance to CE Directive

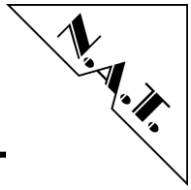
Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

5.3.4 Product Safety

The board complies with EN60950 and UL1950.

5.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.



6 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Altera CycloneIII FPGA, Device Handbook Volume 1, V2.4, 07/2012
[2] FTDI USB-to-JTAG-Bridge, Datasheet FT_000061 V2.21, 06/2012
[3] XAPP1251 v1.0 04/ 2015
[4] XVC protocol specification and example designs available
[url:https://raw.githubusercontent.com/Xilinx/XilinxVirtualCable/master/README_XVC_v1_0.txt]

Appendix B: Document's History

Revision	Date	Description	Author
1.0	10.11.2014	Initial release	se
1.0	20.4.2015	Added content	te
1.1	15.5.2015	Updated Block diagram	hl
1.2	21.5.2015 7.10.2015	Updated Chapter "Programming via MCH" Removed Chapter 3.6.3 Pinout of rotary Switch Added function of green/yellow Led Added environmental conditions Some minor corrections	Al hl
1.3	08.04.2016	Added description for using Xilinx Impact software Added description for changing Lattice Diamond TCK frequency	te
1.4	17.5.2016	Wording clarified for slave port selection	hl
1.4	18.05.2016	Added description for slave/master LED assignments	te