Meikon

N.A.T.

MAMC-XLINK
Technical Reference Manual V1.2
HW Revision 1.0, 1.1

The MAMC-XLINK has been designed by:

Meikon Ltd
10 Bringsty Common
Worcester
WR6 5UJ
Great Britain

Phone +44 1886 822208
Internet: http://www.meikon.net

and

N.A.T. GmbH
Kamillenweg 22
53757 Sankt Augustin
Germany

Phone: +49 2241 3989-0
Fax: +49 2241 3989-10
E-Mail: support@nateurope.com
Internet: http://www.nateurope.com

Disclaimer

The following documentation, compiled by Meikon Ltd. and N.A.T. GmbH (henceforth called Meikon and N.A.T.), represents the current status of the product´s development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. Meikon and N.A.T. are under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

Caution this publication may include technical inaccuracies or typographical errors.

Meikon and N.A.T. offer no warranty, either expressed or implied, for the contents of this documentation or for the product described therein, including but not limited to the warranties of merchantability or the fitness of the product for any specific purpose.

In no event will Meikon or N.A.T. be liable for any loss of data or for errors in data utilization or processing resulting from the use of this product or the documentation. In particular, Meikon or N.A.T. will not be responsible for any direct or indirect damages (including lost profits, lost savings, delays or interruptions in the flow of business activities, including but not limited to, special, incidental, consequential, or other similar damages) arising out of the use of or inability to use this product or the associated documentation, even if Meikon or N.A.T., or any authorized representative has been advised of the possibility of such damages.

The use of registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations (patent laws, trade mark laws, etc.) and therefore free for general use. In no case does Meikon or N.A.T. guarantee that the information given in this documentation is free of such third-party rights.

Neither this documentation nor any part thereof may be copied, translated, or reduced to any electronic medium or machine form without the prior written consent from Meikon or N.A.T..

This product (and the associated documentation) is governed by the Meikon and N.A.T. General Conditions and Terms of Delivery and Payment.

Note:

The release of the Hardware Manual is related to a particular HW board revision given in the document title. For earlier hardware revisions please contact Meikon or N.A.T. for the relevant Hardware Manual release.

Table of Contents

List of Tables

List of Figures

Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
b	Bit, binary
B	byte
IPMI	Intelligent Platform Management Interface Specification
MCH	µTCA Carrier Hub
µTCA	Micro Telecommunications Computing Architecture
nc	not connected
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PICMG	PCI Industrial Computer Manufacturers Group

1 Introduction

The **MAMC-XLINK** is a high performance standard Advanced Mezzanine Card, single width, full height. It can be plugged onto any ATCA carrier board supporting AMC standards. It is also designed to meet the requirements of µTCA systems.

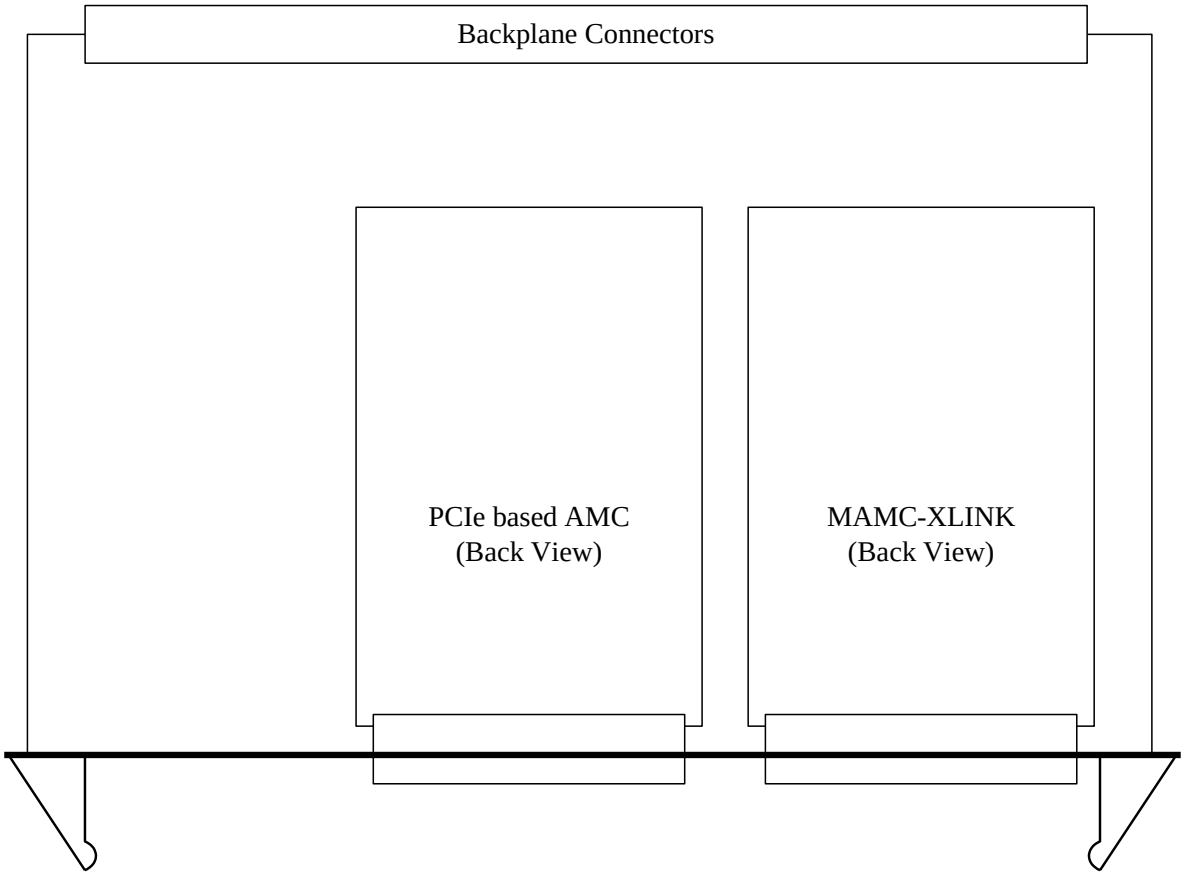
The **MAMC-XLINK** connects one lane of a PCIe backplane through a programmable Re-Driver circuitry to a PCI Express External Cable Interface Connector on the front panel.

The **MAMC-XLINK** is member of a family of XLINK boards which enable the connection of different system platforms via a PCI Express External Cable Interface. Typically one system will be a master system containing a processor card and the second system will be a slave system which does not contain a processor card and is controlled by the master system. Examples of other XLINK products are the **MPCI-XLINK** and the **MPCIe-XLINK**.

1.1 Installation

The **MAMC-XLINK** can be installed either on a carrier board or plugged into a µTCA system.

Figure 1: MAMC-XLINK on a Carrier Board (ATCA)



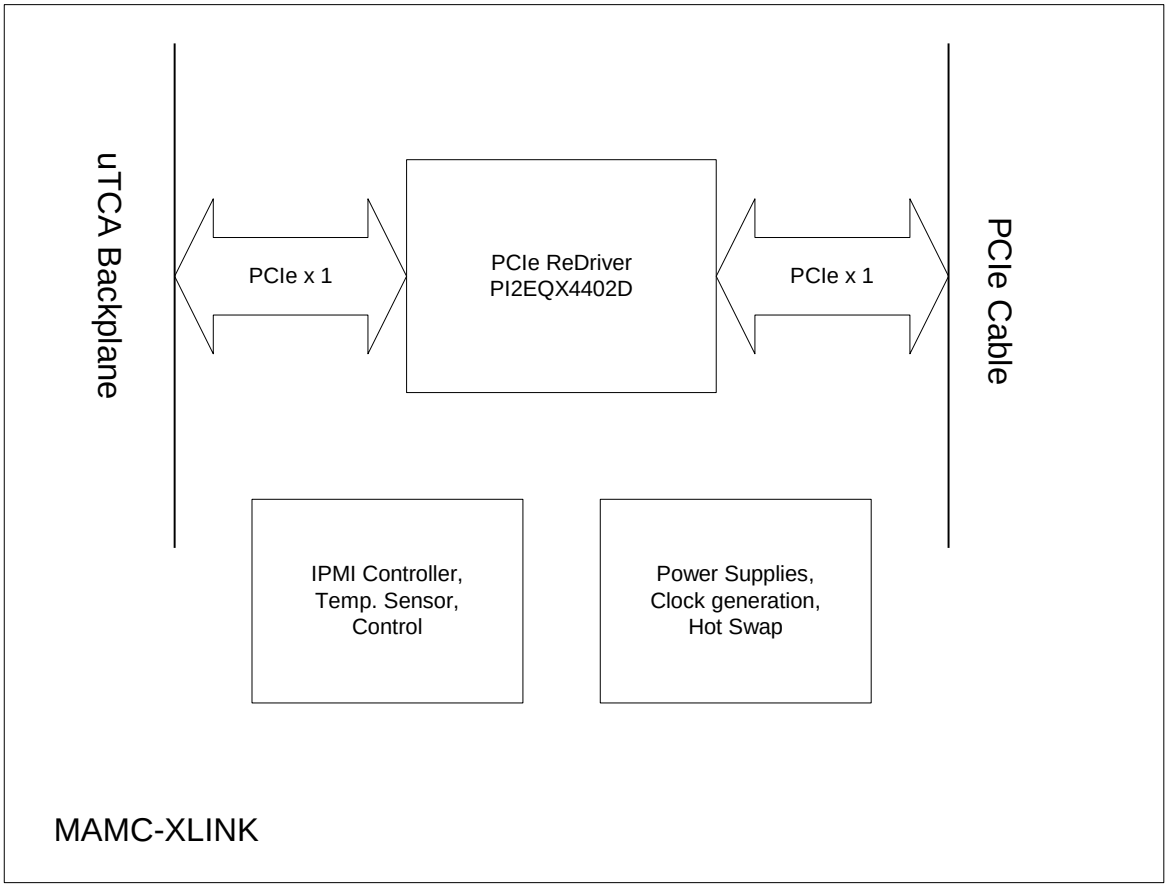
The **MAMC-XLINK** provides master functionality for the cable interface, i.e. provides clock and management signals. When connecting it to another XLINK board, please make sure that the other board does not have master functionality for the cable interface. The other board will be in a slave system. This slave system should be powerd up before the system containing the **MAMC-XLINK** to ensure that the AMC system finds the slave rack when it powers up.

1.2 Block Diagram

The **MAMC-XLINK** has the following major features implemented on-board:

- 1 Lane PCI Express Interface Rev. 1.1 to backplane
- 1 Lane PCI Express External Cable Interface Rev. 1.0 to front panel
- Re-Driver circuitry for boost and reshaping of the PCIe signals
- IPMI Controller

Figure 2: MAMC-XLINK Block Diagram



1.3 Board Features

- **PCI Express Interface**

  The **MAMC-XLINK** includes a 1 – lane PCI Express interface. The PCI Express interface connects to Port 4 of the Fat Pipe Region of the AMC backplane connector. The implementation of PCIe conforms to the AMC.1 specification.

- **PCI Express External Cable Interface**

  The **MAMC-XLINK** includes a 1 – lane PCI Express External Cable Interface. The PCI Express External Cable Interface connects to a special PCI Express External Cable connector. The implementation of PCI Express External Cable Interface conforms to the PCI Express External Cabling Specification, Rev. 1.0.

- **IPMI Controller**

  The **MAMC-XLINK** implements an IPMB interface which conforms to the AMC.0 specification. The IPMI firmware complies to the IPMI – Intelligent Platform Management Interface Specification, v1.5., Revision 1.1.

- **Re-Driver Circuitry**

  The **MAMC-XLINK** includes Re-Driver circuitry, in order to guarantee PCIe signal quality at the receiver portion of the PCI Express External Cable Interface.

- **Clock Selection**

  The **MAMC-XLINK** offers the choice to select between a local PCIe clock and the backplane clock FCLKA, which is defined in the AMC.0 specification.

1.4 Board Specification

Table 2: MAMC-XLINK Features

AMC-Module	standard Advanced Mezzanine Card, single width, full height	
Front-I/O	1-lane PCI Express External Cable Connector	
Firmware	IPMI firmware	
Power consumption	12V 0.2A max. Payload Power 3.3V 0.1A max. Management Power	
Environmental conditions	Temperature (operating):	0°C to +70°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 1.0	
	PICMG µTCA.0 Rev. 1.0	
	PCI Express Base Specification Rev. 1.1	
	PCI Express External Cabling Specification, Rev. 1.0	
	IPMI Specification v2.0 Rev. 1.0	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **MAMC-XLINK** take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life.

- Before installing or removing the **MAMC-XLINK** read this installation section
- Before installing or removing the **MAMC-XLINK**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or removing the **MAMC-XLINK** on a carrier board or in a rack:

- Check all installed boards and modules for steps that you have to take before turning on or off the power.
- Take those steps.
- Finally turn on or off the power if necessary.
- Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.

- Before touching integrated circuits take all precautions required for handling electrostatic devices.
- Ensure that the **MAMC-XLINK** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module

- is bolted to the front panel or rack
- and shielded by a screened enclosure

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- an ATCA carrier board, or a µTCA backplane for connecting the **MAMC-XLINK**, with a PCI Express lane connected to Port 4
- power supply
- cooling devices

2.2.2 Power supply

The power supply for the **MAMC-XLINK** must meet the following specifications:

- +12V 0.2A Payload Power
- +3.3V 0.1A Management Power

2.2.3 Automatic Power Up

In the following situations the **MAMC-XLINK** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +12V voltage level drops below 10V (payload power)
- when +3.3V voltage level drops below 3.08V (management power)

or when the carrier board / backplane signals AMC Disable.

2.2.4 Thermal Considerations

The **MAMC-XLINK** can be operated in a temperature range of 0°C to +70°C if the air velocity does not fall below 1 m/s.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) states that all electrical and electronic equipment being put on the European market after June 30th, 2006 may contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin, any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of the Meikon / N.A.T. hardware products are exempt from the RoHS directive it is the policy of Meikon / N.A.T. to produce compliant products wherever possible. Since January 31st, 2005 Meikon / N.A.T. has stipulated RoHS compliant components from its suppliers. RoHs compliance is also mandatory in the production process.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) mandates that manufacturers of electrical and electronic equipment which is put onto the European market have to contribute to the reuse, recycling and other forms of recovery of such waste. This directive makes reference to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Although the main focus is on household use, the directive also affects business-to-business relationships. The directive is quite restrictive on how household waste has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This is due to the fact that industrial electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be dismantled when it comes to their disposal at the end of their life cycle.

As Meikon / N.A.T. products are sold solely to industrial customers, at the time of purchase the customer agrees to take the responsibility for a WEEE compliant disposal of the used Meikon / N.A.T. product. All Meikon / N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with ordinary waste.

If you have any questions on the policy of Meikon / N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact Meikon / N.A.T. by phone or e-mail.

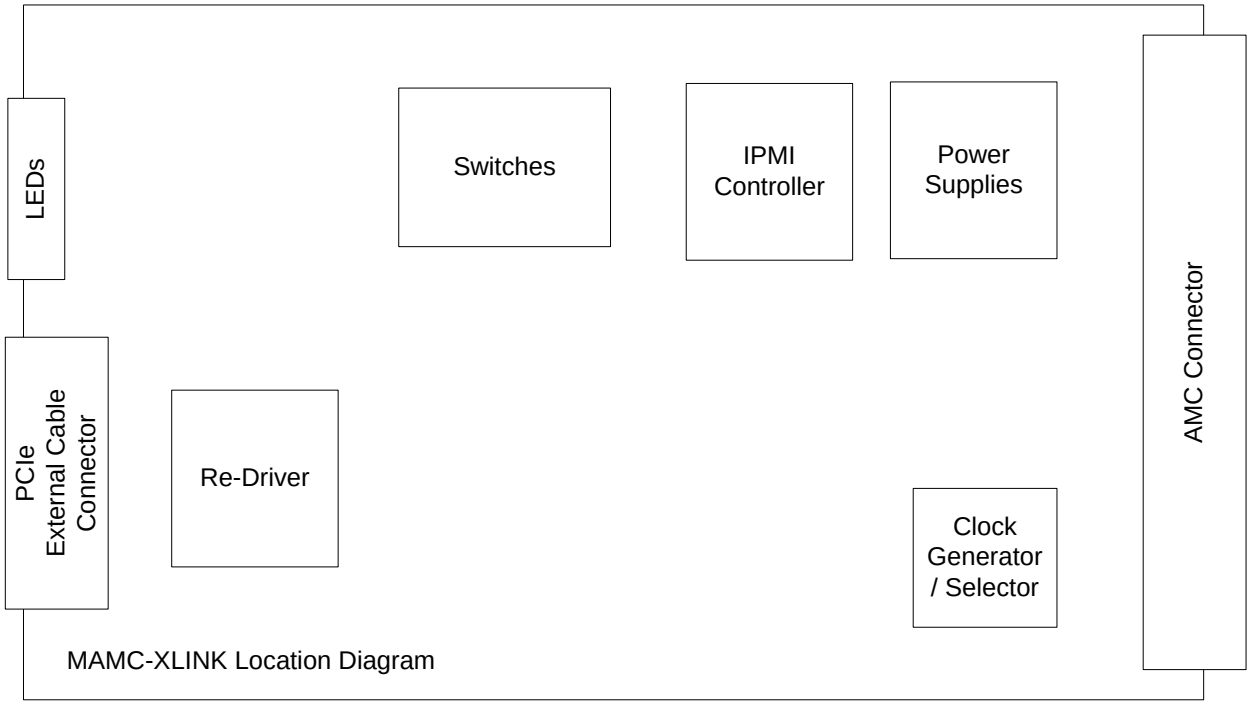
2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

2.4 Location Overview

Figure 3 "Location diagram of the **MAMC-XLINK**" shows the position of major components. Some of the components may not be populated depending on the board version..

Figure 3: Location Diagram of the MAMC-XLINK



3 Functional Blocks

The **MAMC-XLINK** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 Re-Driver Circuitry

The **MAMC-XLINK** includes a Re-Driver circuitry, in order to guarantee PCIe signal quality at the receiver portion of the PCI Express External Cable Interface. There are different cables with different lengths on the market, which comply to the PCI Express External Cable Interface Specification. Although the specification does not specify individual cable lengths, transmission characteristics require that the cable length should not exceed 7m. The Pericom PI2EQX4402D Re-Driver device installed on the **MAMC-XLINK** allows the user to adapt transmission charateristics to different cable lengths. As cable types and lengths will differ, it is not possible to give specific settings for the re-driver under all conditions. The user may need to adjust the settings if the default settings do not result in a satisfactory performance. With the **MAMC-XLINK** this can be done either in Software (by means of programming the IPMI controller appropriately), or by switch settings. Please refer to chapters 5.6, 5.7, and 6.3 for a more detailed explanation. The PI2EQX4402D Re-Driver device implements four unidirectional ports, two of which are used on the **MAMC-XLINK**. Port A is used to drive the PCIe line from the AMC backplane to the PCI Express Cable Interface connector, Port C is used to drive the PCIe line from the PCI Express Cable Interface connector to the AMC backplane. Ports B and D are permanently disabled.

3.2 IPMI Controller

The AVR ATmega645 microcontroller used to implement IPMI functionality integrates an SPI Programming Interface, an I^2C interface, analogue inputs, and interrupt capabilities on some port pins. IPMI firmware makes use of some of these features. Please refer to chapters 4.2 and 6 for a more detailed explanation.

3.3 IPMB Interface

The **MAMC-XLINK** implements an IPMB interface consisting of an AVR ATmega645 microcontroller and a temperature sensor. The IPMB controller also manages the hot swap functionality and the geographical address as requested by the AMC.0 specification.

3.4 AMC Clock Interface

AMC backplane clock port FCLKA (Clock 3) is connected to a clock selector, in order to be used as a reference clock for PCI Express. FCLKA is only received. FCLKA is routed to a multiplexer, which allows programming the clock source of the PCI Express External Cable Interface to be either FCLKA, or an internal differential 100 MHz reference clock.
The **MAMC-XLINK** is always clock master of the PCI Express External Cable Interface, i.e. the clock is transmitted to the cable interface, but not received from there.

3.5 Cable Interface Control Signals

The PCI Express External Cable Interface implemented on the **MAMC-XLINK** supports the following Cable Interface control signals:

CPERST#, CPRSNT#, CWAKE#, CPWRON

For definition, usage, sensing, and programming of these control signals please refer to chapter 6.3 and to the PCI Express External Cable Interface Specification.

4 Hardware Description

4.1 AMC Port Definition

Table 3: AMC Port Definition

	Port No.	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	unassigned
	CLK2		unassigned
	CLK3		Reference Clock 3 (FCLKA, PCI Express Clock)
	0	Common Options Region	unassigned
	1		unassigned
	2		unassigned
	3		unassigned
	4	Fat Pipes	PCI Express Lane 0
	5		unassigned
	6		unassigned
	7		unassigned
Extended Connector	8	Region	unassigned
	9		unassigned
	10		unassigned
	11		unassigned
	12	Extended Options Region	unassigned
	13		unassigned
	14		unassigned
	15		unassigned
	CLK4/5		unassigned
	17		unassigned
	18		unassigned
	19		unassigned
	20		unassigned

For proper operation, the **MAMC-XLINK** requires a PCI Express Lane to be connected to Port 4 of the AMC connector.

4.2 Definition of ATmega645 Port Pins

ATmega645 port pins are used to communicate with the PCI Express External Cabling Interface and to set up some Re-Driver configuration as follows:

Table 4: ATmega645 Port Pin Usage (Port A)

Signal Function	ATmega645 Port A Pin	Description
/HS_SW	PA7	Hot Swap Switch
PWRGD	PA6	Power Good Indicator
/IALERT	PA5	Power Good Indicator
GA_PALLUP	PA4	driver for Geographical Address sensing
GA2	PA3	Geographical Address 2
GA1	PA2	Geographical Address 1
GA0	PA1	Geographical Address 0
/AMC_ENABLE	PA0	Enable AMC module

Table 5: ATmega645 Port Pin Usage (Port B)

Signal Function	ATmega645 Port B Pin	Description
/CPRSNT	PB7	PCIe Cable Interface present indicator
not used	PB6	*pin is unconnected*
/PWRON	PB5	Power On PCIe Cable Interface control pin
/PERST	PB4	PCIe Reset Output
MISO	PB3	SPI programming interface
MOSI	PB2	SPI programming interface
SCLK	PB1	SPI programming interface
not used	PB0	*pin is unconnected*

Table 6: ATmega645 Port Pin Usage (Port C)

Signal Function	ATmega645 Port C Pin	Description
EN_A	PC7	enable Port A programmability
SEL_A6	PC6	SEL6 Re-Driver Port A
SEL_A5	PC5	SEL5 Re-Driver Port A
SEL_A4	PC4	SEL4 Re-Driver Port A
SEL_A3	PC3	SEL3 Re-Driver Port A
SEL_A2	PC2	SEL2 Re-Driver Port A
SEL_A1	PC1	SEL1 Re-Driver Port A
SEL_A0	PC0	SEL0 Re-Driver Port A

Table 7: ATmega645 Port Pin Usage (Port D)

Signal Function	ATmega645 Port D Pin	Description
EN_C	PD7	enable Port C programmability
SEL_C6	PD6	SEL6 Re-Driver Port C
SEL_C5	PD5	SEL5 Re-Driver Port C
SEL_C4	PD4	SEL4 Re-Driver Port C
SEL_C3	PD3	SEL3 Re-Driver Port C
SEL_C2	PD2	SEL2 Re-Driver Port C
SEL_C1	PD1	SEL1 Re-Driver Port C
SEL_C0	PD0	SEL0 Re-Driver Port C

Table 8: ATmega645 Port Pin Usage (Port E)

Signal Function	ATmega645 Port E Pin	Description
PCIE_CLKSEL	PE7	select the PCIe clock
CWAKE#	PE6	CWAKE# signal from Cable Interface
SDA	PE5	I^2C bus to AMC backplane, IPMB
SCL	PE4	I^2C bus to AMC backplane, IPMB
/RED_LED	PE3	controls the red LED on the front panel
/BLUE_LED	PE2	controls the blue LED on the front panel
SDA_INT	PE1	internal I^2C bus to Temperature Sensor
SCL_INT	PE0	internal I^2C bus to Temperature Sensor

Table 9: ATmega645 Port Pin Usage (Port F)

Signal Function	ATmega645 Port F Pin	Description
not used	PF7	*pin is unconnected*
not used	PF6	*pin is unconnected*
not used	PF5	*pin is unconnected*
not used	PF4	*pin is unconnected*
not used	PF3	*pin is unconnected*
not used	PF2	*pin is unconnected*
1.8V_SENSE	PF1	analogue/digital converter sense input for +1.8V supply voltage
3.3V_SENSE	PF0	analogue/digital converter sense input for +3.3V supply voltage

Table 10: ATmega645 Port Pin Usage (Port G)

Signal Function	ATmega645 Port G Pin	Description
/RST_IPMI	PG5	RESET input to IPMI controller
	PG4	controls the yellow LED on the front panel
	PG3	controls the green LED on the front panel
not used	PG2	*pin is unconnected*
LED4	PG1	controls LED 4 on the front panel LED block
LED3	PG0	controls LED 3 on the front panel LED block

4.3 Front Panel LEDs

The front panel LEDs are divided into 2 groups:

- the LEDs specified by the AMC.0 standard
- a block of 4 LEDs above the PCI Express External Cable connector

4.3.1 AMC Standard LEDs

The AMC standard defines 4 LEDs, located on the lower / right side of the front panel, two of which are mandatory, and two of which are optional. The **MAMC-XLINK** supports all of these LEDs.

There are two general status LEDs, a blue LED, and a red LED. These LEDs are controlled by IPMI firmware. The other two LEDs, a green LED and a yellow LED, are optional. They are supplied, but their use depends on user's software.

4.3.2 4 LED Block

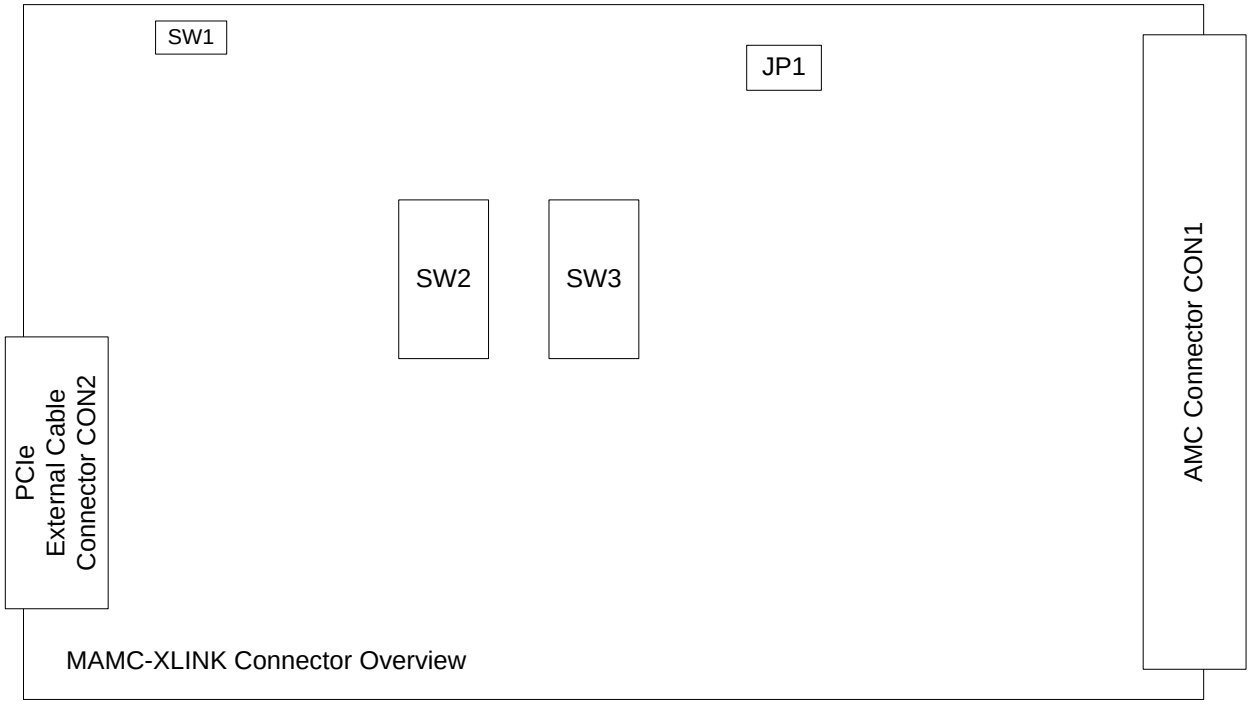
There is a 4 LED block located above the PCI Express External Cable connector. LEDs 1 and 2 of this block show the link status of the Re-Driver PCIe lines. LEDs 3 and 4 are programmable by the user.

All programmable LEDs are controlled by the ATmega645 microcontroller. For further information on how to program these LEDs please refer to the ATmega325/3250/645/6450/V Product Data Book, or turn to Meikon / N.A.T. for further assistance.

5 Connectors and Switches

5.1 Connector Overview

Figure 4: Connectors of the MAMC-XLINK



Please refer to the following tables to look up the connector pin assignment of the **MAMC-XLINK**.

5.2 AMC Connector CON1

Table 11: AMC Connector CON1

Pin No.	AMC-Signal	AMC-Signal	Pin No.
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	NC	163
9	PWR	NC	162
10	GND	GND	161
11	XLINK1_P	NC	160
12	XLINK1_N	NC	159
13	GND	GND	158
14	RLINK1_P	NC	157
15	RLINK1_N	NC	156
16	GND	GND	155
17	GA1	NC	154
18	PWR	NC	153
19	GND	GND	152
20	NC	NC	151
21	NC	NC	150
22	GND	GND	149
23	NC	NC	148
24	NC	NC	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134

Pin No.	AMC-Signal	AMC-Signal	Pin No.
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PET0_P_P4	NC	127
45	PET0_N_P4	NC	126
46	GND	GND	125
47	PER0_P_P4	NC	124
48	PER0_N_P4	NC	123
49	GND	GND	122
50	NC	NC	121
51	NC	NC	120
52	GND	GND	119
53	NC	NC	118
54	NC	NC	117
55	GND	GND	116
56	IPMB_SCL	NC	115
57	PWR	NC	114
58	GND	GND	113
59	NC	NC	112
60	NC	NC	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	NC	NC	97
75	NC	NC	96
76	GND	GND	95
77	NC	NC	94
78	NC	NC	93

Pin No.	AMC-Signal	AMC-Signal	Pin No.
79	GND	GND	92
80	FCLKA_P	NC	91
81	FCLKA_N	NC	90
82	GND	GND	89
83	/PS0	NC	88
84	PWR	NC	87
85	GND	GND	86

5.3 Front Panel Connector CON2

Table 12: shows the pin assignment of PCI Express External Cable Interface connector.

Table 12: Pin Assignment of the Front Panel Connector CON2

Pin No.	Signal	Signal	Pin No.
A1	CPER0_N	GND	B1
A2	CPER0_P	not connected	B2
A3	not connected	CWAKE#	B3
A4	SB_RTN	CPRSNT#	B4
A5	CFRECLK_N	GND	B5
A6	CFRECLK_P	not connected	B6
A7	not connected	CPWRON	B7
A8	CPERST#	CPET0_N	B8
A9	GND	CPET0_P	B9

5.4 AVR Programming Port Connector JP1

Connector JP1 connects the SPI- or programming port of the AVR ATmega645 microcontroller.

Table 13: ATmega645 Programming Port JP1

Pin No.	Signal	Signal	Pin No.
1	MISO	+3.3V	2
3	SCLK	MOSI	4
5	/RST_IPMI	GND	6

5.5 Hot Swap Switch SW1

Switch SW1 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

5.6 DIL Switch SW2

The PI2EQX4402D Re-Driver device implements four unidirectional ports, two of which are used on the **MAMC-XLINK**. DIL switch SW2 is used to set the line transmission characteristics of Re-Driver A, which drives the PCIe line from the AMC backplane to the PCI Express Cable Interface connector.

Table 14: Switch Assignment of DIL Switch SW2

Switch No.	Signal	Default Setting
Pos. 1	SEL_A0	on
Pos. 2	SEL_A1	on
Pos. 3	SEL_A2	on
Pos. 4	SEL_A3	on
Pos. 5	SEL_A4	on
Pos. 6	SEL_A5	on
Pos. 7	SEL_A6	on
Pos. 8	not used	on

5.7 DIL Switch SW3

The PI2EQX4402D Re-Driver device implements four unidirectional ports, two of which are used on the **MAMC-XLINK**. DIL switch SW3 is used to set the line transmission characteristics of Re-Driver C, which drives the PCIe line from the PCI Express Cable Interface connector to the AMC backplane.

Table 15: Switch Assignment of DIL Switch SW3

Switch No.	Signal	Default Setting
Pos. 1	SEL_C0	on
Pos. 2	SEL_C1	on
Pos. 3	SEL_C2	on
Pos. 4	SEL_C3	on
Pos. 5	SEL_C4	on
Pos. 6	SEL_C5	on
Pos. 7	SEL_C6	on
Pos. 8	not used	on

The default settings for both switches SW2 and SW3 have been successfully tested with various cable lengths and should work without change with most user applications.

6 MAMC-XLINK Programming Notes

6.1 AMC Control Signals

The AMC control signals /AMC_ENABLE, GA2 – 0, GA_PULLUP are sensed or set by IPMI firmware. The same applies for control of the AMC LEDs and handling of hot swap events. For further information please turn to N.A.T. GmbH.

6.2 Selecting the PCIe Clock Source

The PCIe clock source can either be the FCLKA clock taken from the AMC backplane, or a local 100 MHz oscillator. ATmega645 microcontroller's port pin PE7 selects the clock source. When PE7 is set "low", FCLKA is the clock source. When PE7 is set "high", the internal oscillator sources the PCI Express External Cable Interface.

6.3 PCI Express External Cable Interface Control Signals

The PCI Express External Cable Interface control signals **CPERST#, CPRSNT#, CWAKE#, CPWRON** are controlled by firmware.

CPERST# is sent downstream the PCI Express External Cable Interface by the MAMC-XLINK either when programmed by port pin PB4 of the ATmega645 microcontroller, or as long as no module is sensed downstream, i.e. **CPRSNT#** is "high".

By driving **CPRSNT#** "low" the downstream system indicates to the upstream system that it has been powered up and is functional. This signal is sensed by ATmega645 microcontroller firmware.

By driving **CWAKE#** "low" the downstream system indicates to the upstream system that it shall power up. This function is optional and not implemented.

CPWRON# is sent downstream the PCI Express External Cable Interface by the **MAMC-XLINK** when programmed by port pin PB5 of the ATmega645 microcontroller, in order to tell the downstream system that it shall power up. This function is optional, and its implementation depends on the hardware of the downstream system. **MAMC-XLINK** firmware doesn't use this feature.

For further information on how to handle these control signals please refer to the PCI Express External Cable Interface Specification and contact N.A.T. GmbH.

6.4 Programming the Re-Driver Device Strapping Pins

The Pericom PI2EQX4402D Re-Driver device installed on the **MAMC-XLINK** allows the user to adapt transmission charateristics to different cable lengths. This strapping may be done either by software or by setting the 2 DIL switches SW2 and SW3. By default, setting the strapping pins by software is disabled.

When the DIL switches are used for strapping, ATmega645 microcontroller's port pins PC7 and PD7 have to be set to "high", which can either be done by programming these port pins appropraitely, or by not programming them at all (default). In this case a pull-up resistor pulls the enable signals high.

6.4.1 Re-Driver Strapping Pins Description

The Re-Driver Strapping Pins set the transmission line driver characteristics. Their influence on the transmission line driver characteristics is as follows:

Table 16: Re-Driver Strapping Pins SEL0 – 2, Equalizer Selection

SEL0	SEL1	SEL2	Compliance Channel
0	0	0	No Equalisation
0	0	1	[0:1.5dB] @ 1.25 GHz
0	1	0	[0:2.5dB] @ 1.25 GHz
0	1	1	[0:3.5dB] @ 1.25 GHz
1	0	0	[0:4.5dB] @ 1.25 GHz
1	0	1	[0:5.5dB] @ 1.25 GHz
1	1	0	[0:6.5dB] @ 1.25 GHz
1	1	1	[0:7.5dB] @ 1.25 GHz

Table 17: Re-Driver Strapping Pins SEL3 – 4, Output Swing Control

SEL3	SEL4	Swing
0	0	1 x
0	0	0.8 x
0	1	1.2 x
0	1	1.4 x

Table 18: Re-Driver Strapping Pins SEL5 – 6, Output De-emphasis Adjustment

SEL5	SEL6	De-emphasis
0	0	0 dB
0	0	-2.5 dB
0	1	-3.5 dB
0	1	-4.5 dB

If the setting of the transmission line driver characteristics shall be done by software, please turn to Meikon / N.A.T. GmbH for further assistance.

6.5 Setup of the Serial Interfaces

6.5.1 I^2C Interfaces

There are two I^2C interfaces connected to the ATmega645 microcontroller's port pins.
The 1st one connects port pins PE0 (Clk) and PE1 (Data) to a LM75 temperature sensor. The address of this sensor is 0.
The 2nd I^2C interface is connected to port pins PE4 (Clk) and PE5 (Data). This I^2C interface is routed to the IPMB interface of the AMC backplane.
IPMI firmware programs these two interfaces.

6.5.2 SPI Interface

The SPI interface is connected to port pins PB3 (SPIMISO), PB2 (SPIMOSI), and PB1 (SCLK). It is used for in-system-programming of the AVR ATmega645 microcontroller.

7 Known Bugs / Restrictions

- Re-Driver link sense circuitry not functionable, link status not diplayed correctly on LEDs 1 and 2

Appendix A: Reference Documentation

[1] Pericom, PI2EQX4402D 2.5Gbps x2 Lane Serial PCI Express Repeater / Equalizer with Signal Detect feature, 11/06
[2] Atmel, ATmega325/3250/645/6450/V Product Data, Rev. 2570L, 08/07
[3] PCI Local Bus Specification, Revision 3.0, February 3, 2004
[4] PCI Express Base Specification, Revision 2.0, December 20, 2006
[5] IPMI – Intelligent Platform Management Interface Specification, v1.5. Revision 1.1, February 20, 2002
[6] AdvancedTCA Base Specification (PICMG 3.0 R1.0), December 30, 2002, and as amended by ECN 3.0-1.0-001
[7] PCI Express External Cabling Specification, Revision 1.0, January 4, 2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	01.19.2009	initial revision	ga
1.1	05.05.2010	correction of typos	ga
1.2	13.07.2011	Altered in figure one AMC next to XLINK module	te