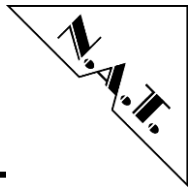
**NAMC-MPX**
**CPU AMC Module**
**Technical Reference Manual V1.2**
**HW Revision 1.2**



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# Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

The following table gives a list of the abbreviations used in this document.

**Table 1: List of used abbreviations**

| Abbreviation | Description |
|---|---|
| AMC | Advanced Mezzanine Card |
| BDM | Background Debug Mode |
| CPU | Central Processing Unit |
| DDR SDRAM | Double Data Rate Synchronous Dynamic RAM |
| DIP SW | Dual In-Line Switch |
| DUART | Dual Universal Asynchronous Receiver/Transmitter |
| ECC | Error Correcting Code |
| EEPROM | Electrically Erasable PROM |
| FCLK | Fabric Clock |
| FPGA | Field Programmable Gate Array |
| GbE | Gigabit Ethernet |
| H.110 | Timeslot Interchange Bus |
| I²C | Inter-Integrated Circuit |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| iTDM | Internal TDM |
| JTAG | Joint Test Action Group |
| LED | Light Emitting Diode |
| MAC | Media Access Control |
| MCC | Memory Chip Controller |
| MPX | Microsys PPC Extendable Module |
| PCB | Printed Circuit Board |
| PCI(e) | Peripheral Component Interconnect (Express) |
| PLL | Phase Locked Loop |
| PHY | Physical Layer Device |
| (P)ROM | (Programmable) Read Only Memory |
| RAM | Random Access Memory |
| RGMII | Reduced Gigabit Media Independent Interface |
| SATA | Serial Advanced Technology Attachment |
| SD-Card | Secure Digital Memory Card |
| SDRAM | Synchronous Dynamic RAM |
| SerDes | Serializer/Deserializer |
| SRIO | Serial Rapid I/O |
| SPI FLASH | Serial Peripheral Interface FLASH |
| TCKL | Telecom Clock |
| TSI | Time Slot Interchanger |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| XAUI | 10 GbE (via 4x 3.125 GB/s) |

# 1 Introduction

The **NAMC-MPX** as modular platform element for MPX modules is dedicated to versatile embedded markets such as industrial controls, automation, (tele-)communication, defense&aerospace and medical area.

As carrier board based on AMC form factor, the **NAMC-MPX** provides a sophisticated infrastructure and offers two Ethernet, one USB, and one RS232 interface at the front panel. At the common options region of the AMC connector (port 0/1) are two GbE interfaces, two SATA (port 2 and port 3) as well as optional fat pipe interfaces as PCIe, SRIO, or XAUI at port 4-7.

The distinctive feature of the **NAMC-MPX** is the combination of N.A.T.'s basic AMC board with the powerful **MPX2020** module by MicroSys (**M**icroSys **P**PC E**X**tendable Module). This MPX module offers versatile I/O functionality as DUART, Ethernet, $I^2C$ and PCIe.

It will be possible to adopt other Microsys MPX extension boards to the **NAMC-MPX** carrier; what demands slight changes in design of the carrier board. For further information please contact N.A.T. Europe.

# 2 Overview

## 2.1 Major Features

Main features of the **NAMC-MPX** are determined by the extension board **MPX2020:**

- Freescale QorIQ P2020 with dual e500v2 Power Architecture @1.2 GHz
- Up to 2 GB DDR 2 SDRAM
- Up to 512 MB NAND-Flash

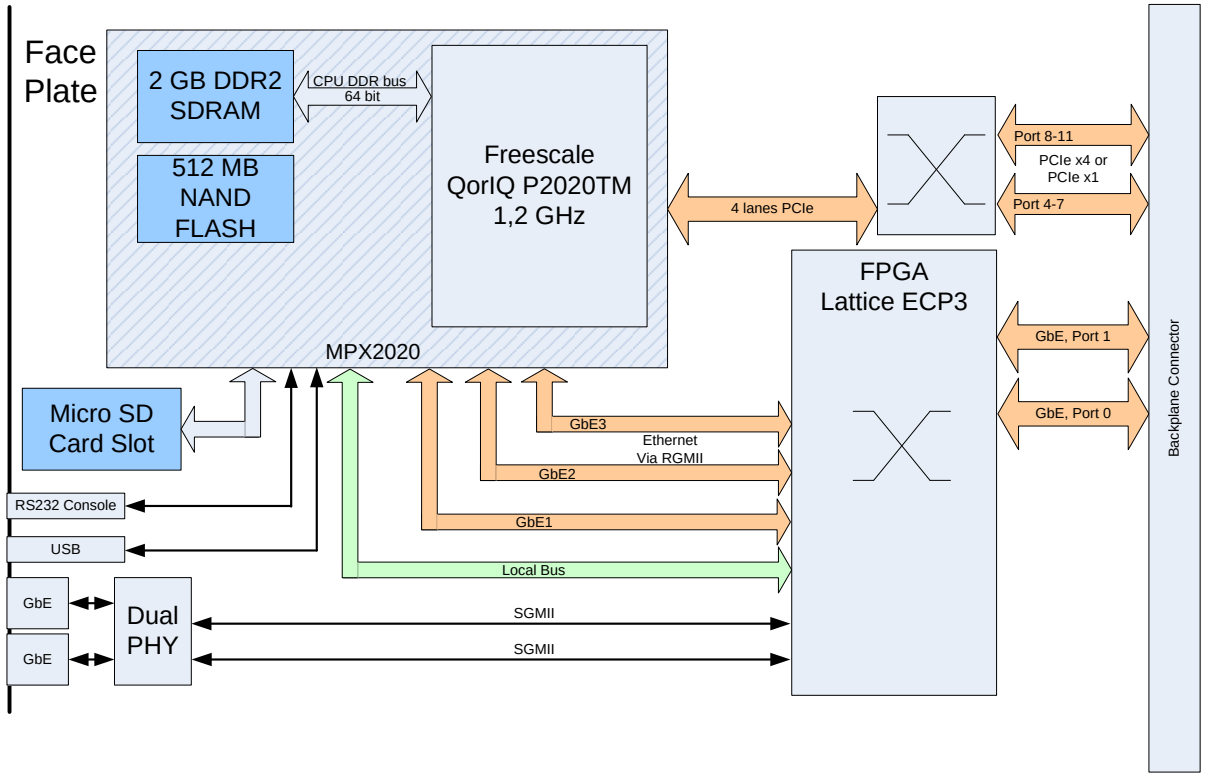
Features of the **NAMC-MPX** Base Board:

- Micro SD Card slot
- Lattice ECP3-FPGA
- PCIe Interface
- 2x 10/100/1000-BaseT Ethernet Front Panel Ethernet
- 2x Gigabit Ethernet at AMC Ports 0/1
- Optional: iTDM Interface
  - 1024 bidirectional 64kbit/s channels
  - 125µs-mode and 1ms-mode support (mixture possible)
- Optional: H.110 alike Backplane TSI bus
- USB Type A Jack on Front Panel
- RS232 Debug Connector on Front Panel (via Mini-USB Jacket)

## 2.2 Block Diagram

The following figure shows a detailed block diagram of the **NAMC-MPX** base board with the **MPX2020** extension board attached.

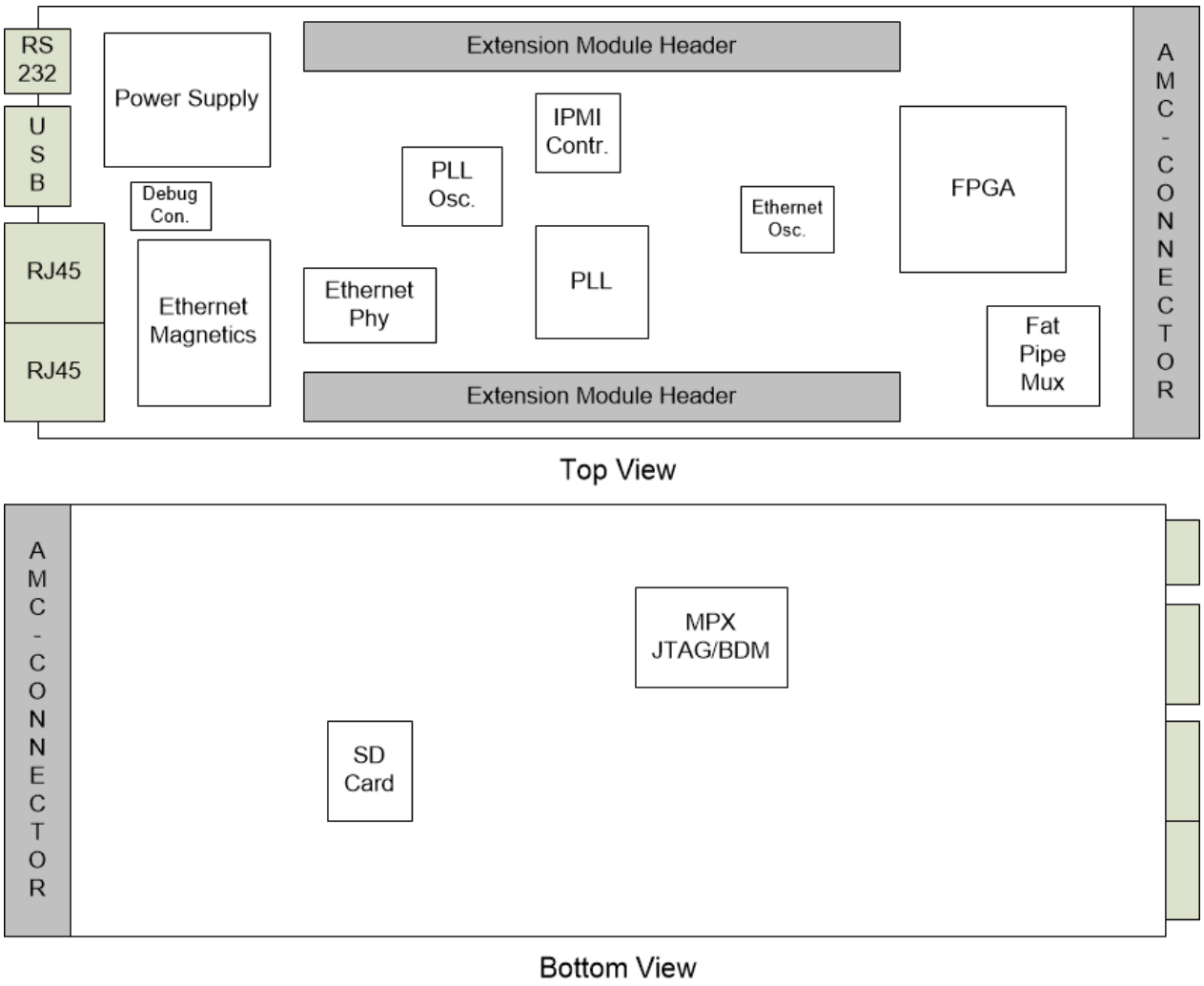
**Figure 1: NAMC-MPX – Block Diagram – Overview**



## 2.3 Location Diagram

The following figure shows the position of important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

**Figure 2: NAMC-MPX – Location Diagram Base Board – Overview**




For further information regarding a location diagram of the **MPX2020** extension board please refer to the Microsys **MPX2020** specification.

# 3 Board Features

The **NAMC-MPX** can be divided into a number of functional blocks, which are described in the following paragraphs.

## 3.1 CPU (MPX2020 Extension Board)

The Freescale QorIQ P2020 is a versatile communications processor that integrates on one chip a high-performance microprocessor and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.
The core is a dual core e500v2 running at 1.2 GHz with 32 Kbytes of L1 cache and 512 Kbytes of Level 2 cache.

## 3.2 Memory

### 3.2.1 DDR2 SDRAM (MPX2020 Extension Board)

The DDR2 SDRAM memory with ECC support is 64 bit wide; up to 2 GB can be assembled. The interface is implemented in the QorIQ P2020. By programming several registers the RAM controller can be adapted to different RAM architectures.

### 3.2.2 FLASH (MPX2020 Extension Board)

FLASH memory is connected to the de-multiplexed upper 16 data bits D0 – 15 and to the latched address lines. De-multiplexing of the local address/data bus of the CPU, as well as address latching, is performed by an FPGA. It can be programmed by the CPU or through the BDM port.

### 3.2.3 Micro SD-Card Slot (NAMC-MPX Base Board)

The **NAMC-MPX** is equipped with an SD-Card Slot that features up to 2 GB additional non-volatile memory.

## 3.3 FPGA

Beside some power/up reset logic the Lattice ECP3-FPGA is the Ethernet connection cross point on the **NAMC-MPX**. It establishes connectivity and performs the necessary conversion between:

- Front GbE 1
- Front GbE 2
- Backplane AMC Port 0 GbE
- Backplane AMC Port 1 GbE
- CPU RGMII interface 0
- CPU RGMII interface 1
- CPU RGMII interface 2

## 3.4 PCI Express and SRIO Interface

The P2020 CPU includes a 4-Lane SerDes unit, which is used to equip the **NAMC-MPX** with x4 PCIe by default. The configuration options include the following:

- PCIe x4 on Ports 4-7 or Ports 8-11
- PCIe x1 on Port 4 or Port 8

## 3.5 Ethernet

### 3.5.1 Front Panel Ethernet

On its face plate the **NAMC-MPX** is equipped with two RJ45 jacks, which offer a 10/100/1000-BaseT Ethernet interface each, handled by a Broadcom dual PHY device (BCM5482). The PHY's MAC side interfaces are then further connected to the FPGA. Within here it can be selected whether the CPU's two Ethernet controllers operate via the backplane Ethernet lines, via the front Ethernet ports or use a combination of both. Future FPGA versions could offer application specific switching functionality at this point.

### 3.5.2 Backplane Ethernet

The FPGA internal SerDes Ethernet is connected to the P2020's Ethernet MAC through RGMII interfaces, which are fed through the FPGA. It connects to the backplane Ethernet, the physical layer of which is 1000BaseX. Within FPGA logic the CPU Ethernet data is multiplexed with the iTDM data and transferred through the same physical port.

## 3.6 iTDM

The **NAMC-MPX** implements an optional serial iTDM backplane interface, the physical layer of which is 1000BaseX. The iTDM interface connects to Port 0/1 of the Common Options Region of the AMC backplane connector and shares the ports with the CPU Ethernet path.
One task of the FPGA residing on the **NAMC-MPX** is offering a powerful TDM to iTDM conversion engine to the board. This can be used for directly connecting channels from the line interface of other AMC boards to the **NAMC-MPX**.

## 3.7 Backplane TDM

The **NAMC-MPX** implements an 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. It bridges to a module-internal TDM bus, which connects to the MCC ports of the P2020 QUICCEngine. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Extended Options Region of the AMC connector.

## 3.8 USB Interface

The front panel connector J3 is a USB Type A jack that connects to the CPU internal USB controller. It can be used to implement various USB functionality covering both host or device behaviour.

## 3.9 RS232 Interface

The RS232 interface is physically presented in a Mini-USB Type B jacket. It is normally used for debugging purpose along with a standard terminal program (default baud rate: 19200).

## 3.10AMC Clock Interface

The **NAMC-MPX** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D and FCLKA.
All TCLK ports are connected directly to the FPGA and can be used for reception of any clock or can be configured to drive a clock signal. This infrastructure can be used for distributing recovered reference clocks from the line interfaces or to synchronize the **NAMC-MPX** to an external clock.

## 3.11 $I^2C$-Devices and IPMB

The **NAMC-MPX** implements an IPMB interface consisting of an ATmega1284P IPMI-Microcontroller, a temperature sensor (LM95241 – I²C-Address: 0x56), and the Hot-Swap controller (LTC4215 – I²C-Address: 0x96).
Please note that the 7-bit I²C-Address is left aligned in the notation, meaning that in the most-right bit (LSB) the I²C R/W bit resides.

Additionally, the IPMB-Bus of the AMC connector is attached to the IPMI-Controller.

The IPMI-Controller manages also the geographical address as requested by the AMC specification.

# 4 Hardware

## *4.1 AMC Port Definition*

**Table 2: AMC Port Definition**

| | Port # | AMC Port Mapping Strategy | Ports used as |
|---|---|---|---|
| Basic Connector | CLK1 | Clocks | Reference Clock 1 / TCLKA |
| | CLK2 | | Reference Clock 2 / TCLKB |
| | CLK3 | | Reference Clock 3 / FCLKA |
| | 0 | Common Options Region | 1000BaseX Ethernet Channel 1 (iTDM and CPU Ethernet), default |
| | 1 | | 1000BaseX Ethernet Channel 2 (iTDM and CPU Ethernet), redundant |
| | 2 | | unassigned |
| | 3 | | unassigned |
| | 4 | Fat Pipes | SerDes Lane 0 |
| | 5 | | SerDes Lane 1 |
| | 6 | | SerDes Lane 2 |
| | 7 | | SerDes Lane 3 |
| Extended Connector | 8 | Region | SerDes Lane 0 Alternative |
| | 9 | | SerDes Lane 1 Alternative |
| | 10 | | SerDes Lane 2 Alternative |
| | 11 | | SerDes Lane 3 Alternative |
| | 12 | Extended Options Region | TDM Bus D0-3 (H.110 extended) |
| | 13 | | TDM Bus D4-7 (H.110 extended) |
| | 14 | | optional clock lines (H.110 extended)/ unassigned |
| | 15 | | Unassigned |
| | 16 | | TCLKC / TCLKD |
| | 17 | | Unassigned |
| | 18 | | Unassigned |
| | 19 | | Unassigned |
| | 20 | | Unassigned |

## 4.2 Front Panel and LED

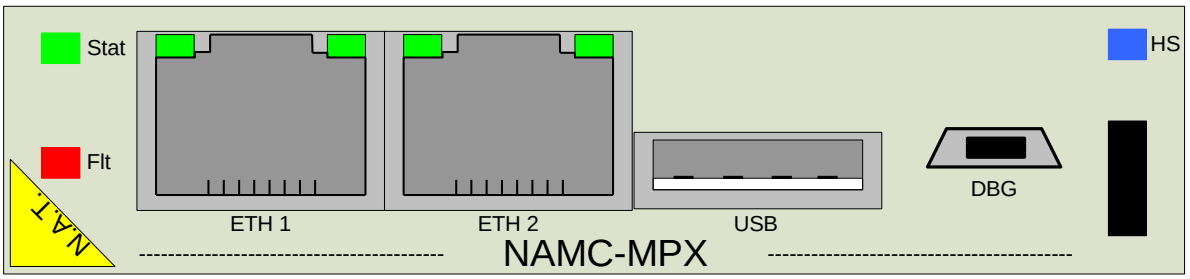
The **NAMC-MPX** module is equipped with 4 bicolour LEDs integrated in the RJ45 interface jacks. They are driven by the Ethernet PHY and can be programmed to various link indication modes.

Additionally the module contains the standard AMC LEDs consisting of a fault indication LED controlled by the IPMI controller and a general purpose status LED controlled by the FPGA/CPU.

The Fault Indication LED turns to "On" if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to "Off" again.

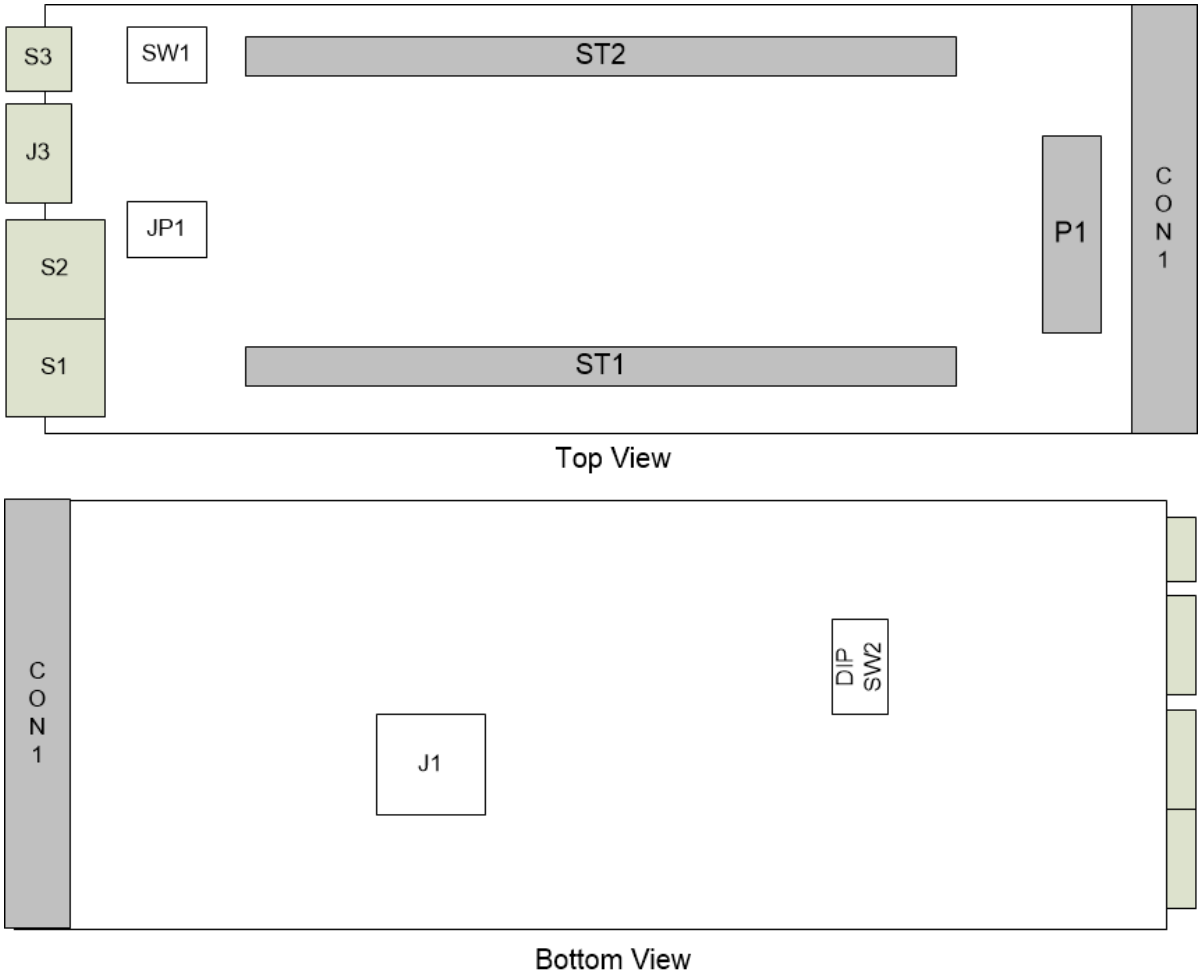
Standard behaviour of the status LED is as follows:
The LED is timely multiplexed to display the status of both backplane Ethernet links operating via AMC port 0/1 combined with the link status between the FPGA and the front Ethernet PHY device. A period of solid green indicates here a link on AMC port0, a period of fast green blinking indicates a link on AMC port 1 and a period of solid orange indicates a link between the front Ethernet PHY and the FPGA.

**Figure 3: NAMC-MPX – Front Panel**



## 4.3 Connectors and Switches

**Figure 4: NAMC-MPX – Connector and Switch Location – Overview**




Please refer to the following tables to look up the connector pin assignment of the **NAMC-MPX**.

### *4.3.1 CON1: AMC Connector*

**Table 3: CON1: AMC Connector – Pin Assignment**

| Pin # | AMC-Signal | AMC-Signal | Pin # |
|---|---|---|---|
| 1 | GND | GND | 170 |
| 2 | PWR | TDI | 169 |
| 3 | /PS1 | TDO | 168 |
| 4 | PWR_IPMB | /TRST | 167 |
| 5 | GA0 | TMS | 166 |
| 6 | RESVD | TCK | 165 |
| 7 | GND | GND | 164 |
| 8 | RESVD | NC | 163 |
| 9 | PWR | NC | 162 |
| 10 | GND | GND | 161 |
| 11 | PORT0_TX_P | NC | 160 |
| 12 | PORT0_TX_N | NC | 159 |
| 13 | GND | GND | 158 |
| 14 | PORT0_RX_P | NC | 157 |
| 15 | PORT0_RX_N | NC | 156 |
| 16 | GND | GND | 155 |
| 17 | GA1 | NC | 154 |
| 18 | PWR | NC | 153 |
| 19 | GND | GND | 152 |
| 20 | PORT1_TX_P | NC | 151 |
| 21 | PORT1_TX_N | NC | 150 |
| 22 | GND | GND | 149 |
| 23 | PORT1_RX_P | NC | 148 |
| 24 | PORT1_RX_N | NC | 147 |
| 25 | GND | GND | 146 |
| 26 | GA2 | NC | 145 |
| 27 | PWR | NC | 144 |
| 28 | GND | GND | 143 |
| 29 | NC | NC | 142 |
| 30 | NC | NC | 141 |
| 31 | GND | GND | 140 |
| 32 | NC | TCLKD_P | 139 |
| 33 | NC | TCLKD_N | 138 |
| 34 | GND | GND | 137 |
| 35 | NC | TCLKC_P | 136 |
| 36 | NC | TCLKC_N | 135 |
| 37 | GND | GND | 134 |
| 38 | NC | NC | 133 |
| 39 | NC | NC | 132 |
| 40 | GND | GND | 131 |
| 41 | /ENABLE | NC | 130 |
| 42 | PWR | NC | 129 |
| 43 | GND | GND | 128 |
| 44 | PORT4_TX_P | RESVD | 127 |

| Pin # | AMC-Signal | AMC-Signal | Pin # |
|---|---|---|---|
| 45 | PORT4_TX_N | TDM_REF | 126 |
| 46 | GND | GND | 125 |
| 47 | PORT4_RX_P | TDM_FS | 124 |
| 48 | PORT4_RX_N | TDM_CLK | 123 |
| 49 | GND | GND | 122 |
| 50 | PORT5_TX_P | TDM7 | 121 |
| 51 | PORT5_TX_N | TDM6 | 120 |
| 52 | GND | GND | 119 |
| 53 | PORT5_RX_P | TDM5 | 118 |
| 54 | PORT5_RX_N | TDM4 | 117 |
| 55 | GND | GND | 116 |
| 56 | IPMB_SCL | TDM3 | 115 |
| 57 | PWR | TDM2 | 114 |
| 58 | GND | GND | 113 |
| 59 | PORT6_TX_P | TDM1 | 112 |
| 60 | PORT6_TX_N | TDM0 | 111 |
| 61 | GND | GND | 110 |
| 62 | PORT6_RX_P | PORT11_TX_P | 109 |
| 63 | PORT6_RX_N | PORT11_TX_N | 108 |
| 64 | GND | GND | 107 |
| 65 | PORT7_TX_P | PORT11_RX_P | 106 |
| 66 | PORT7_TX_N | PORT11_RX_N | 105 |
| 67 | GND | GND | 104 |
| 68 | PORT7_RX_P | PORT10_TX_P | 103 |
| 69 | PORT7_RX_N | PORT10_TX_N | 102 |
| 70 | GND | GND | 101 |
| 71 | IPMB_SDA | PORT10_RX_P | 100 |
| 72 | PWR | PORT10_RX_N | 99 |
| 73 | GND | GND | 98 |
| 74 | TCLKA_P | PORT9_TX_P | 97 |
| 75 | TCLKA_N | PORT9_TX_N | 96 |
| 76 | GND | GND | 95 |
| 77 | TCLKB_P | PORT9_RX_P | 94 |
| 78 | TCLKB_N | PORT9_RX_N | 93 |
| 79 | GND | GND | 92 |
| 80 | FCLKA_P | PORT8_TX_P | 91 |
| 81 | FCLKA_N | PORT8_TX_N | 90 |
| 82 | GND | GND | 89 |
| 83 | /PS0 | PORT8_RX_P | 88 |
| 84 | PWR | PORT8_RX_N | 87 |
| 85 | GND | GND | 86 |

### *4.3.2 J1: Micro SD Card Slot*

J1 connects directly to the SD Card interface and offers the option to use Micro SD Cards as removable Flash Memory on the **NAMC-MPX** board.

**Table 4: J1: Micro SD-Card Slot – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | SD_DAT2 | SD_DAT3 | 2 |
| 3 | SD_CMD | +3.3V | 4 |
| 5 | SD_CLK | GND | 6 |
| 7 | SD_DAT0 | SD_DAT1 | 8 |

### *4.3.3 J3: USB Connector*

Connector J3 offer access to the CPU's USB interface.

**Table 5: J3: USB Connector – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | VBUS | USB_D_N | 2 |
| 3 | USB_D_P | GND | 4 |

### *4.3.4 JP1: RS232 Connector*

The Debug Terminal Connector JP1 offers the option to connect to UART1 of the CPU to realize a serial terminal interface. This connector can be used as alternative to the front panel connector S3.

**Table 6: JP1: RS232 Connector – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | RxDA | GND | 2 |
| 3 | TxDA | | |

### *4.3.5 P1: MXP JTAG Connector*

Connector P1 connects to the CPU's JTAG Interface.

**Table 7: P1: MPX JTAG Connector – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | MPX_TDO | GND | 2 |
| 3 | MPX_TDI | MPX_TRST | 4 |
| 5 | nc | +3.3V | 6 |
| 7 | MPX_TCK | MPX_CKSTI | 8 |
| 9 | MPX_TMS | nc | 10 |
| 11 | nSRST | GND | 12 |
| 13 | nHRST | nc | 14 |
| 15 | nMPX_CKSTO | GND | 16 |

### *4.3.6 S1/S2: RJ45 Ethernet*

Connectors S1 and S2 offer access to a 10/100/1000-BaseT Ethernet interface each.

**Table 8: S1/S2: RJ45 Connectors – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | TRD0+ | TRD0- | 2 |
| 3 | TRD1+ | TRD2+ | 4 |
| 5 | TRD2- | TRD1- | 6 |
| 7 | TRD3+ | TRD3- | 8 |

### *4.3.7 S3: RS232 Front Panel Connector*

Connector S3 offers access to a RS232 interface connected to UART1 of the CPU.

**Table 9: S3: RS232 Front Panel Connector – Pin Assignment**

| Pin # | Signal | Signal | Pin # |
|---|---|---|---|
| 1 | RTS_SCC1 | RxD_SCC1 | 2 |
| 3 | TxD_SCC1 | CTS_SCC1 | 4 |
| 5 | GND | | |

### *4.3.8 ST1/ST2: Extension Module Connector*

Connectors ST1/ST2 connect to the extension module mounted on the **NAMC-MPX**. Please refer to the documentation of the respective MPX module for detailed information.

### *4.3.9 SW1: Hot Swap Switch*

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

### *4.3.10DIP SW2: Boot Mode Select / Reserved*

The table below gives an overview of the operating parameters configurable via DIP SW2. Details are given in the following subchapters.

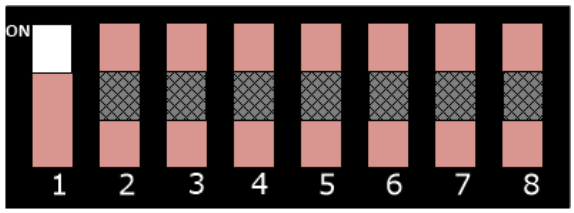
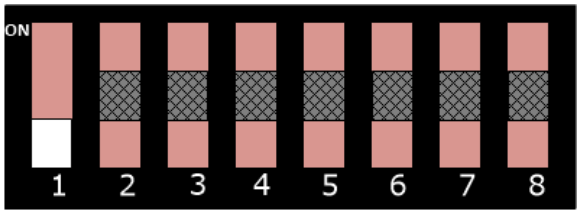
**Table 10: DIP SW2: Pin-Assignment – Overview**

| Switch # | Function |
|---|---|
| 1 | Boot Mode Select |
| 2-8 | Reserved |

#### 4.3.10.1 DIP SW2: Switch 1 – Boot Mode Select Switch

By operating switch 1 of DIP SW2 to ON, the SD-Card is selected as boot source. If switch 1 of DIP SW2 is turned to OFF, the FLASH memory is selected as boot source.

**Table 11: DIP SW2: Switch 1 – Boot Mode Select – Pin-Assignment**

| DIP SW2 – Switch 1 | Function |
|---|---|
|  | Boot source: SD-Card |
|  | Boot source: FLASH |

***Default:***
Switch 1 of DIP SW2 is toggled to OFF; FLASH memory is selected for booting.

# 5 NAMC-MPX Programming Notes

## 5.1 FPGA Memory Map

**Table 12: FPGA Memory Map**

| | Logical Block | Description |
|---|---|---|
| **0x00000..0x000ff** | General Purpose Status | General Purpose Read-Only |
| **0x00100..0x001ff** | General Purpose Registers | General Purpose Read/Write |
| **0x01000..0x01fff** | FPGA SPI Flash Interface | |
| **0x02000..0x02fff** | Atmel SPI Interface | |
| **0x10000..0x1ffff** | GigabitEthernet Interface Block | |
| **0x20000..0x2ffff** | Local TDM Block | |
| **0x80000..0xfffff** | iTDM Block | |

## 5.2 FPGA Register Description General Purpose Status Registers - 0x00..0x1ff

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x00** | Reserved | | | | | | | | PCB_VERS | | | | | | | |
| **0x02** | DEV_VERS | | | | | | | | FPGA_VERS | | | | | | | |
| **0x04** | TEST_VAL_1 | | | | | | | | | | | | | | | |
| **0x06** | TEST_VAL_2 | | | | | | | | | | | | | | | |
| **0x08** | Board_ID | | | | | | | | | | | | | | | |
| **0x0A** | DIP_SW_ST | | | | | | | | R. | FPGA_PIN_ST | | | | | | |
| **0x0C** | Reserved | | | | | | | | | | | | | | | |
| **0x0E** | Reserved | | | | | | | | | | | | | | | |
| **0x10** | CARRIER_ID | | | | | | | | GEO_ADDRESS | | | | | | | |
| **0x12** | FPGA_INF_1 | | | | | | | | FPGA_INF_2 | | | | | | | |

#### 5.2.1.1 FPGA Register Description – PCB_VERS – 0x00

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..8** | | Reserved | 0x00 | Read Only |
| **7..0** | PCB_VERS | PCB version determined by level of unused pins hardcoded on PCB | HW init | Read Only |

#### 5.2.1.2 FPGA Register Description – DEV_VERS / FPGA_VERS – 0x02

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..8** | DEV_VERS | Development version | na | Read Only |
| **7..0** | FPGA_VERS | FPGA version | na | Read Only |

#### 5.2.1.3 FPGA Register Description – TEST_VAL_1 – 0x04

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..0** | TEST_1 | Random number for testing purposes | 0xAA55 | Read Only |

#### 5.2.1.4 FPGA Register Description – TEST_VAL_2 – 0x06

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..0** | TEST_2 | Random number for testing purposes | 0xDEAD | Read Only |

#### 5.2.1.5 FPGA Register Description – BOARD_ID – 0x08

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..0** | BOARD_ID | Holds the internal Board-ID | 0x0b17 | Read Only |

#### 5.2.1.6 FPGA Register Description – DIP_SW_ST / FPGA_PIN_ST – 0x0A

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..8** | DIP_SW_ST | DIP Switch Status | | Read Only |
| **7** | | Reserved | | Read Only |
| **7..0** | FPGA_PIN_ST | FPGA Pin Status – reflects assembly option | | Read Only |

#### 5.2.1.7 FPGA Register Description – CARRIER_ID / GEO_ADDRESS – 0x10

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..8** | CARRIER_ID | Carrier Manager ID<br>0x80 + 2*Carrier Number | na | Read Only |
| **7..0** | GEO_ADDRESS | Geographical Address (Slot ID)<br>0x72: AMC1<br>0x74: AMC2<br>0x76: AMC3<br>0x78: AMC4<br>0x7A: AMC5<br>0x7C: AMC6<br>0x7E: AMC7<br>0x80: AMC8<br>0x82: AMC9<br>0x84: AMC10<br>0x86: AMC11<br>0x88: AMC12 | na | Read Only |

#### 5.2.1.8 FPGA Register Description – FPGA_INF_1 / FPGA_INF_2 – 0x12

This register can be used to deliver further information from the Microcontroller to the FPGA; not used yet.

| Bit | Name | Description | Default | Access |
|---|---|---|---|---|
| **15..8** | FPGA_INF_1 | Tbd | | Read Only |
| **7..0** | FPGA_INF_2 | Tbd | | Read Only |

# 6 Board Specification

**Table 13: NAMC-MPX with MPX2020 Specification – Overview**

| | |
|---|---|
| **Processor*** | Freescale QorIQ P2020<br>dual e500v2 Power Architecture 1.2 GHz |
| **AMC-Module** | Standard Advanced Mezzanine Card, single width |
| **Front-I/O** | 2x RJ45 Ethernet, USB Type A, RS232 (Mini-USB) |
| **Main Memory*** | Up to 2 GB DDR2 SDRAM |
| **FLASH PROM*** | Up to 512 MB NAND-Flash |
| **Removable FLASH** | Micro-SD-Card slot |
| **Firmware** | OK1 and LINUX BSP |
| **Power Consumption (NAMC-MPX with MPX2020 installed)** | 12V, 2.0A max. |
| **Operating Temperature** | 0°C – +55°C with forced cooling |
| **Storage Temperature** | -40°C - +85°C |
| **Humidity** | 10% – 90% rh non-condensing |
| **Standards compliance** | PICMG AMC.0 Rev. 2.0<br>PICMG AMC.1 Rev. 1.0<br>PICMG AMC.2 Rev. 1.0 (Type E2)<br>PCI Express Base Specification Rev. 1.1<br>PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)<br>PICMG SFP.1 Rev. 1.0 (Internal TDM)<br>IPMI Specification v2.0 Rev. 1.0<br>PICMG µTCA.0 Rev. 1.0 |

* located on **MPX2020** extension board

# 7 Installation

## *7.1 Safety Note*

To ensure proper functioning of the **NAMC-MPX** during its usual lifetime take the following precautions before handling the board.

**CAUTION**
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAMC-MPX** read this installation section
- Before installing or uninstalling the **NAMC-MPX**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-MPX** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
    - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-MPX** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

## 7.2 Installation Prerequisites and Requirements

**IMPORTANT**
Before powering up check this section for installation prerequisites and requirements!

### 7.2.1 Requirements

The installation requires only:

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-MPX**
- power supply
- cooling devices

### 7.2.2 Power supply

The power supply for the **NAMC-MPX** must meet the following specifications:

- required for the module: +12V / 2.0A max.

### 7.2.3 Automatic Power Up

In the following situations the **NAMC-MPX** will automatically be reset and proceed with a normal power up:

- The voltage sensor generates a reset
  - when +12V voltage level drops below 10V
  - when +3.3V voltage level drops below 3.08V
- when the carrier board / backplane signals a PCIe Reset.

# 7.3 Statement on Environmental Protection

### 7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

### 7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

### *7.3.3 Compliance to CE Directive*

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

### *7.3.4 Product Safety*

The board complies with EN60950 and UL1950.

### *7.3.5 Compliance to REACH*

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

# 8 Known Bugs / Restrictions

none

# Appendix A: Reference Documentation

[1] Freescale, QorIQ P2020 Data Sheet, Rev.2, 8/7/2013
[2] Lattice, ECP3 Handbook, Version 2.7EA, April 2014
[3] Atmel, 8-bit Atmel Microcontroller Data Sheet, Rev. 8272E–AVR–04/2013

# Appendix B: Document's History

| Revision | Date | Description | Author |
|---|---|---|---|
| 1.1 | 14.07.2011 | initial revision | se/te |
| 1.2 | 18.05.2013 | Address, phone and fax updated, words updatedPost / Telefon geändert, rote Wörter | fh |
| | 15.10.2013 | Adaption to HW Version 1.2<br>Added Connector Overview<br>Adaption to new layout<br>Typo correction, minor changes | se |
| | 22.01.2014 | Added FPGA Register Description | se |
| | 13.08.2014 | Added chapter 3.3 FPGA<br>Update chapter 3.11 I²C-Devices and IPMB<br>Update chapter 4.2 Front Panel and LED<br>Update chapter 7.3 RoHS-Directive / REACH<br>Update Abbreviation List<br>Minor changes | Se |
| | 23.09.2014 | Minor changes | se |