NAMC-8560-8E1/T1/J1
Telecom AMC Module
Technical Reference Manual V1.8
HW Revision 1.2

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

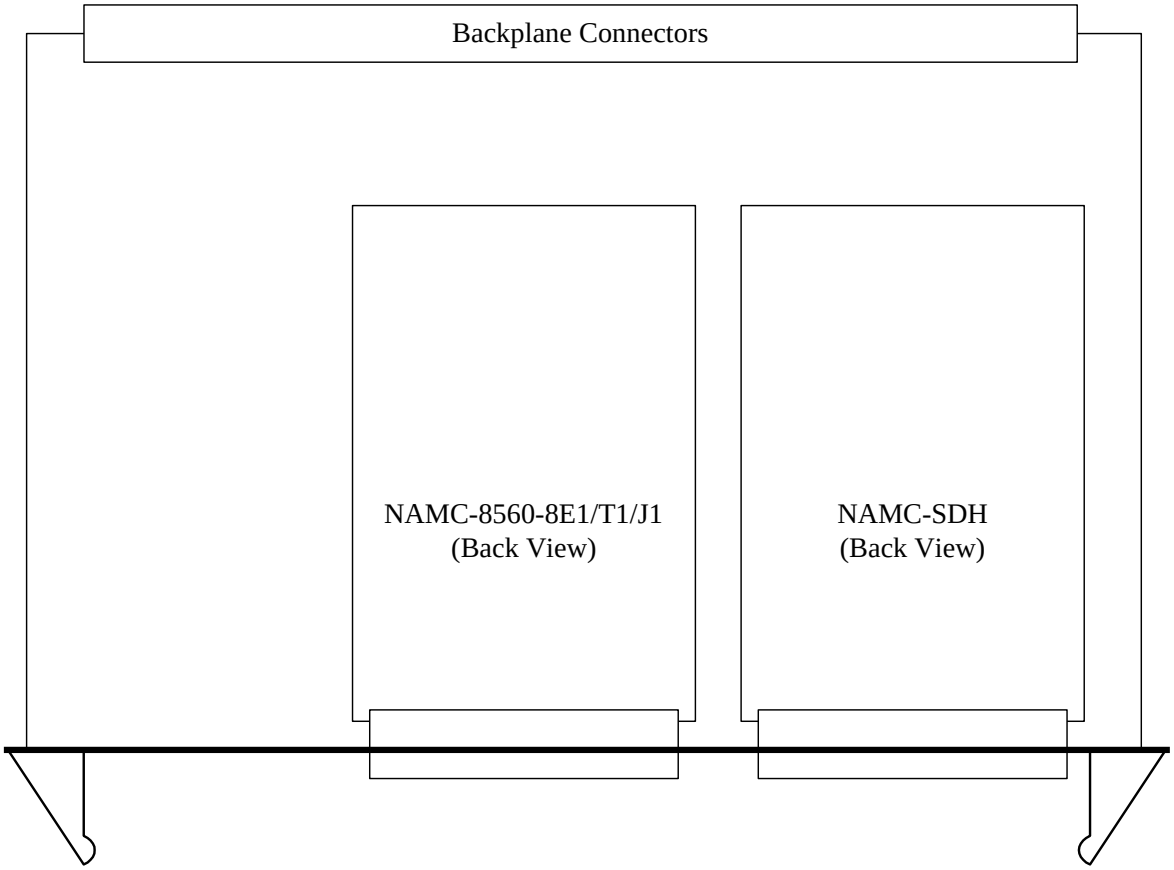
Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Dual Data Rate
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
FLASH	Reprogrammable ROM
FPGA	Field Programmable Gate Array
H.110	Time-Slot Interchange Bus
iTDM	internal TDM
J1	1,544 Mbit G.703 Interface (Japan)
LIU	Line Interface Unit
MCH	µTCA Carrier Hub
MPC8560	Embedded Processor from Freescale
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI-X	Extended PCI
PowerQUICC III	MPC8560
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCC	Serial Communication Controller of the MPC8560
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC8560
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner

1 Introduction

The **NAMC-8560-8E1/T1/J1** is a high performance standard Advanced Mezzanine Card, single width, double height. It can be plugged onto any ATCA carrier board supporting AMC standards. It is also designed to meet the requirements of µTCA systems.

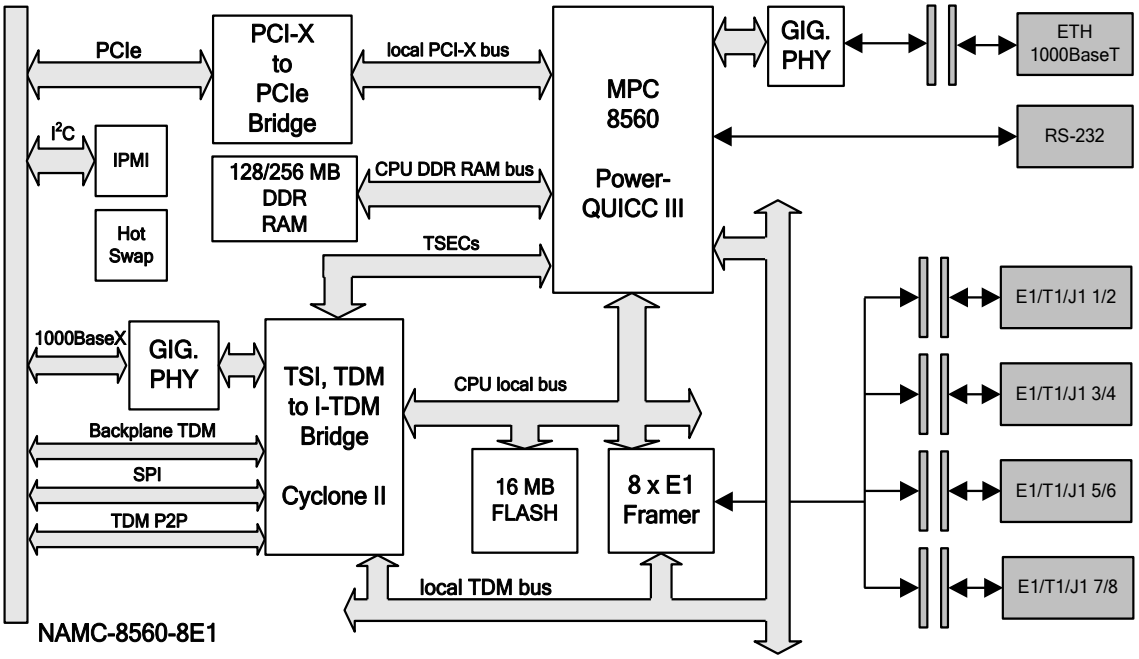
Figure 1: NAMC-8560-8E1/T1/J1 on a carrier board (ATCA)



The **NAMC-8560-8E1/T1/J1** has the following major features implemented on-board:

- PowerQUICC III MPC8560 based Embedded PowerPC Architecture
- 128 – 256 MB main Memory (DDR SDRAM)
- 16 – 32 MB FLASH
- 1 Lane PCI Express Interface Rev. 1.1
- 8 x E1 / T1 / J1 Primary Rate Line Interface
- 1000BaseT Ethernet channel on Front Panel
- Front-Panel RS232 serial I/O
- 1000BaseBX Control Path
- H.110 alike Backplane TSI bus
- SPI Backplane Bus
- 1000BaseBX iTDM Interface
- TDM Point to Point Interface

Figure 2: NAMC-8560-8E1/T1/J1 Block Diagram



1.1 Board Features

- **CPU**

  Depending on the assembled CPU the PowerQUICC III runs with a core clock frequency of 667 - 1000 MHz. The CPM frequency may be set to 267 or 333 MHz (assembly option).

- **Memory**

  SDRAM: The **NAMC-8560-8E1/T1/J1** provides 128 – 256 MB DDR SDRAM onboard (assembly option). The DDR SDRAM is 64 bit wide.

  Default: 128 MB installed

  FLASH PROM: The 16 bit wide Flash PROM provides a capacity of 16 – 64 MB (assembly option).

  Default: 16 MB installed

- **Interfaces**

  Port numbers given show both possibilities of connecting the respective port to the backplane in a redundant system. The 1st port number is the default connection, the 2nd is the connection when connecting to the redundant MCH of a µTCA system. To which port the actual connection is routed is decided during initialisation by the IPMI communication between the active MCH and the IPMI controller onboard the **NAMC-8560-8E1/T1/J1**. Unless the IPMI controller tells the MPC8560 CPU differently, the default connection is the 1st port number given.

  PCIe: The **NAMC-8560-8E1/T1/J1** includes a 1 – lane PCI Express interface. This is implemented in a PEX8111 PCI-X to PCIe bridge (PLX). The PCI Express interface connects to Port 4/8 of the Fat Pipe Region of the AMC backplane connector. The implementation of PCIe conforms to the AMC.1 specification.

  Control Path: The **NAMC-8560-8E1/T1/J1** implements a serial Type P Control Path, the physical layer of which is 1000BaseX. The Type P Control Path connects to Port 0/1 of the Common Options Region of the AMC backplane connector. The Control Path is connected to TSEC2 Ethernet MAC of the MPC8560 CPU through the iTDM FPGA, and shares the port with iTDM. The 1000BaseX physical layer device used is the Freescale MC92604.

iTDM: The **NAMC-8560-8E1/T1/J1** implements a serial iTDM backplane interface, the physical layer of which is 1000BaseX. The iTDM interface connects to Port 0/1 of the Common Options Region of the AMC backplane connector, and shares the port with the Type P Control Path. The iTDM interface is implemented in FPGA logic and conforms to the SFP.0 and SFP.1 specifications. The 1000BaseX physical layer device used is the Freescale MC92604.

IPMB: The **NAMC-8560-8E1/T1/J1** implements an IPMB interface which conforms to the AMC.0 specification.

- **Rear I/O**

TDM: The **NAMC-8560-8E1/T1/J1** implements a 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz. Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. It bridges to an module – internal TDM bus, which connects to the MCC ports of the MPC8560 CPM, and to the IDT 82P2288 framer. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Common Options Region of the AMC connector.

SPI: The **NAMC-8560-8E1/T1/J1** implements a SPI bus interface on the backplane, in order to enable Rear-I/O Modules to be programmed. The SPI interface connects to port 20 of the Common Options Region of the AMC connector.

TDM P2P: A TDM Point to Point interface is implemented in FPGA logic. It is supposed to connect to additional framers on a Rear I/O Module. It bridges to a module – internal TDM bus, which connects to the MCC ports of the MPC8560 CPM. The TDM Point to Point interface connects to ports 18 – 19 of the Common Options Region of the AMC connector.

- **Front Panel I/O**

E1/T1/J1: The AMC module carries an IDT 82P2288 framer, which implements eight E1/T1/J1 interfaces.

Ethernet: The 1000 Mbit Ethernet TSEC1 interface supplied by the PowerQUICC III is connected to a 1000BaseT interface through a National DP83865 physical layer device.

RS232: The front panel RS232 interface available on the **NAMC-8560-8E1/T1/J1** is connected to SCC1 of the MPC8560 CPM.

1.2 Board Specification

Table 2: NAMC-8560-8E1/T1/J1 Features

Processor	PowerQUICC III MPC8560 (667, 833 or 1000 MHz) based Embedded PowerPC Architecture	
AMC-Module	standard Advanced Mezzanine Card, single width, double height	
Front-I/O	5 RJ45 connectors, 1 Mini-USB connector	
Main Memory	128 - 256 MByte DDR SDRAM	
Flash PROM	16 – 64 MByte Flash PROM. On board programmable	
Firmware	OK1, VxWorks, LINUX BSP (on request)	
Power consumption (with MPC8560 / 667 MHz)	12V 2.0A max.	
Environmental conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 1.0	
	PICMG AMC.2 Rev. 1.0 (Type E2)	
	PCI Express Base Specification Rev. 1.1	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	PICMG SFP.1 Rev. 1.0 (Internal TDM)	
	IPMI Specification v2.0 Rev. 1.0	
	PICMG µTCA.0 Rev. 1.0	
	ITU-T G.703 (for E1/T1 Standard)	
	ITU-T G.823 (Jitter Attenuation)	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NAMC-8560-8E1/T1/J1** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAMC-8560-8E1/T1/J1** read this installation section
- Before installing or uninstalling the **NAMC-8560-8E1/T1/J1**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-8560-8E1/T1/J1** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-8560-8E1/T1/J1** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-8560-8E1/T1/J1**
- power supply
- cooling devices

2.2.2 Power supply

The power supply for the **NAMC-8560-8E1/T1/J1** must meet the following specifications:

- required for the module:
  +12V / 2.0A max.

2.2.3 Automatic Power Up

In the following situations the **NAMC-8560-8E1/T1/J1** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +12V voltage level drops below 8V
- when +3.3V voltage level drops below 3.08V

or when the carrier board / backplane signals a PCIe Reset.

2.2.4 Thermal Considerations

The **NAMC-8560-8E1/T1/J1** can be operated in a temperature range of 0°C to +50°C if the air velocity does not fall below 1 m/s. This minimum velocity is required in the region of the CPU's heat sink, the residual area should be passed by air with a minimum velocity of 0,5 m/s.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

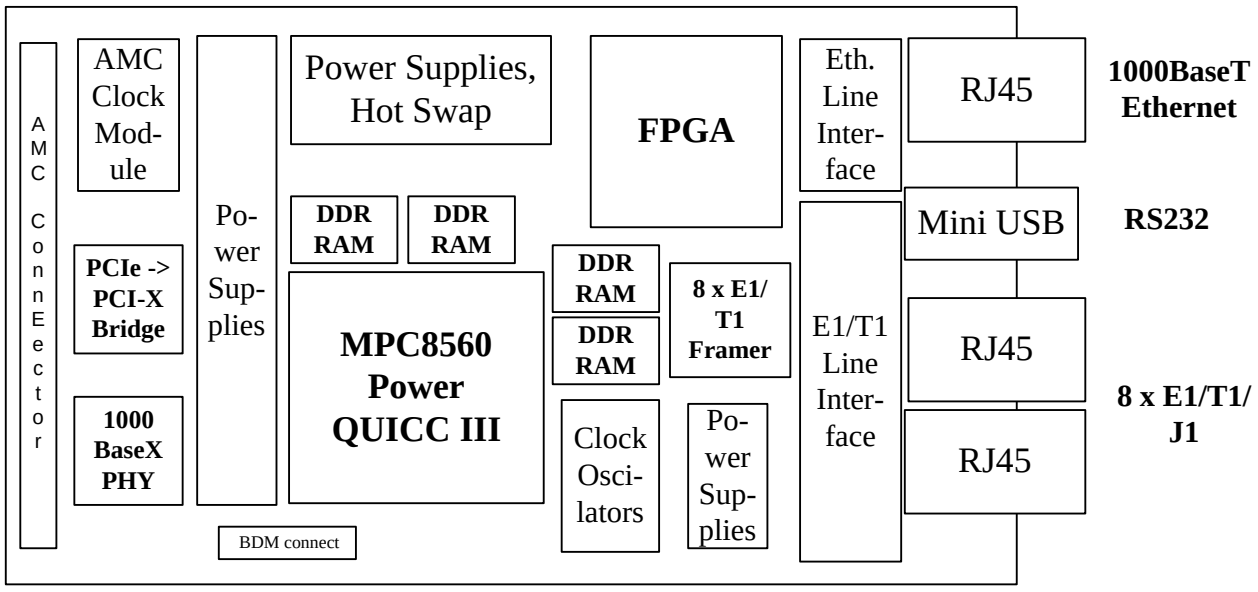
2.3.4 Product Safety

The board complies with EN60950 and UL1950.

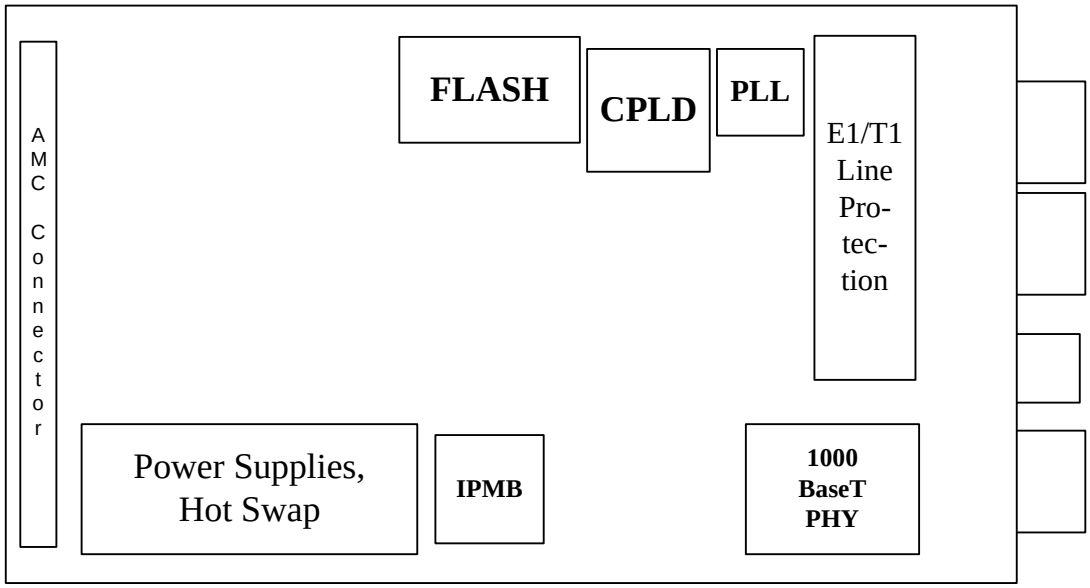
2.4 Location Overview

Figure 3 "Location diagram of the **NAMC-8560-8E1/T1/J1**" shows the position of important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: Location diagram of the NAMC-8560-8E1/T1/J1



Top View



Bottom View

3 Functional Blocks

The **NAMC-8560-8E1/T1/J1** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 Processor Core

The MPC8560 PowerQUICC III™ is a versatile communications processor that integrates on one chip a high-performance PowerPC™ RISC microprocessor, a very flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PowerPC e500™ core with 32 Kbytes of instruction cache and 32 Kbytes of data cache. To this primary cache adds 256 Kbytes of Level 2 cache. The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, and many other peripherals making this device a complete system on a chip.

3.2 Processor – Integrated I/O

The MPC8560 PowerQUICC III™ integrates a Rapid I/O Interface, a switch fabric, and 2 10/100/1000 MB MACs, which support various standard protocols.

The communications processor module (CPM) includes four serial communications controllers (SCCs), with the addition of three high-performance communication channels that support new emerging protocols (for example, 155 Mbps ATM and Fast Ethernet). The MPC8560 has dedicated hardware that can handle up to 256 full-duplex, time-division-multiplexed logical channels, as well as DMA functionality executing memory to memory and memory to I/O transfers.

The MPC8560 integrates a 64 bit PCI / PCI-X interface, and a 4-channel DMA controller.

3.3 Memory

3.3.1 DDR SDRAM

The onboard DDR SDRAM memory is 64 bit wide. Its size is 128 MB (default) or 256 MB (assembly option). The interface to the DDR SDRAM is implemented in the MPC8560. By programming several registers the DDR RAM controller can be adapted to different RAM architectures.

3.3.2 FLASH

FLASH memory is connected to the demultiplexed upper 16 data bits D0 – 15 and to the latched address lines. Demultiplexing of the local address/data bus of the CPU, as well as address latching, is performed by an FPGA. The FLASH on the **NAMC-8560-8E1/T1/J1** can be programmed either by the CPU (by appropriate software or through the BDM port) or by a PCI bus master.

3.3.3 I^2C Devices

There are two I^2C links on the **NAMC-8560-8E1/T1/J1**, which are connected to the MPC8560 I^2C buses; an EEPROM used for storage of board-specific information, which is connected to the dedicated I^2C bus of the MPC8560, and the Cyclone II FPGA device, which connects to the I^2C bus of the MPC8560's CPM. The EEPROM for storage of board-specific information defaults to a 24C08 device.

Two additional I^2C buses connect the IPMI controller, an ATMEL Atmega168 microcontroller, to the IPMB bus of the AMC connector, and to a couple of local devices. The local devices, all powered by IPMB power, are an EEPROM for storage of board-specific information, a 24C08 device, and a temperature sensor, a LM75, which is located near the MPC8560 CPU to sense the processor temperature.

3.3.4 Registers

There are a number of status/control registers implemented. Some of them reside within a CPLD, e.g. those which manage RESET options. Others are implemented in a FPGA, e.g. those which manage the iTDM controller. Refer to chapter 6.3 for details.

3.4 PCI Express Interface

The **NAMC-8560-8E1/T1/J1** includes a 1 lane PCI Express interface. This is implemented in a PEX8111 PCI-X to PCIe bridge (PLX). The PCIe bridge may receive its reference clock either from the Clock 3 port of the AMC backplane connector, or from a local 100 MHz oscillator circuitry (default). The clock source is programmable.

3.5 Front Panel Ethernet

The National Semiconductor DP83865 Ethernet LIU is connected to the MPC8560's TSEC1 through the GMII interface. It connects to the front panel connector S1. The line interface is 1000BaseT.

Configuration settings of the DP83865 are set up by pullup / pulldown resistors. Settings that may need to be altered depending on the application are set up by the FPGA. This applies to signals SPEEDx, DUPLEX, AN_EN, MDIX_EN, and PHY_AD0. Refer to chapter 6.2 for details. The DP83865 LIU, like all other I/O devices, is resettable by software by programming a CPLD register.

3.6 Backplane Ethernet

The Freescale MC92604 Ethernet LIU is connected to the MPC8560's TSEC2 through the GMII interface, which is fed through the FPGA. It connects to the serial Type P Control Path, the physical layer of which is 1000BaseX. Within FPGA logic the Type P Control Path data are multiplexed on the iTDM data and transferred through the same physical port. By default, the LIU is programmed to connect to Port 1 of the Common Options Region of the AMC backplane connector. It can also be programmed to connect to Port 0, in order to support a redundant µTCA system.

Configuration settings of the MC92604 are set up by pullup / pulldown resistors. Settings that may need to be altered depending on the application are set up by the FPGA. Refer to chapter 6.2 for details. The MC92604 LIU, like all other I/O devices, is resettable by software by programming a CPLD register.

3.7 iTDM

The Freescale MC92604 Ethernet LIU is connected to the FPGA through a GMII interface. It connects to the iTDM backplane interface, the physical layer of which is 1000BaseX. Within FPGA logic the Type P Control Path data are multiplexed on the iTDM data and transferred through the same physical port. By default, the LIU is programmed to connect to Port 1 of the Common Options Region of the AMC backplane connector. It can also be programmed to connect to Port 0, in order to support a redundant µTCA system. The iTDM interface is implemented in FPGA logic.

Configuration settings of the MC92604 are set up by pullup / pulldown resistors. Settings that may need to be altered depending on the application are set up by the FPGA. Refer to chapter 6.2 for details.

3.8 Backplane TDM

The **NAMC-8560-8E1/T1/J1** implements a 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32 MHz. Thus, every frame consists of 512 timeslots. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. It bridges to an module – internal TDM bus, which connects to the MCC ports of the MPC8560 CPM, and to the IDT 82P2288 framer. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Extended Options Region of the AMC connector.

3.9 E1/T1/J1 Line Interfaces

The eight E1/T1/J1 interfaces connect the IDT 82P2288 framer to the front panel RJ45 connector S2. Timing and interface characteristics can be set up by software within the 82P2288. The line interfaces conform to EN60950 and G.703 / G.823 (Jitter Attenuation). The front panel RJ45 connector S2 consists of 4 RJ45 jacks, stacked 2 x 2, with integrated LEDs. In order to support 8 E1/T1/J1 interfaces each RJ45 jack carries 2 E1/T1/J1 interfaces. The LEDs are bi-colored and programmable through registers which reside within the FPGA.

3.10 AMC Clock Interface

The **NAMC-8560-8E1/T1/J1** implements a very flexible clocking functionality concerning the AMC backplane clock ports Clock 1 – Clock 3.

AMC backplane clock port Clock 1 is connected to the FPGA, in order to be used as a Telecom standard clock. Clock 1 is only received.

AMC backplane clock port Clock 2 is connected to the FPGA, in order to be used as a Telecom standard reference. Clock 2 may be received from or transmitted to the MCH, in order to become the reference clock for the entire system.

AMC backplane clock port Clock 3 is connected to the PCIe → PCI-X bridge, in order to be used as a reference clock for PCI Express. Clock 3 is only received. Clock 3 is routed to a multiplexer, which allows programming the clock source of the PCIe line to be either Clock 3, or an internal differential 100 MHz reference clock.
In case clock 3 is to be used for a different functionality, it also feeds the FPGA and may be used there for any suitable purpose.

A description on how to program the clock sources can be found in chapter 6.2.

3.11 IPMB Interface

The **NAMC-8560-8E1/T1/J1** implements an IPMB interface consisting of an AVRmega168 microcontroller and a couple of I2C devices, such as a temperature sensor, and an EEPROM. The IPMB controller manages also the hot swap functionality and the geographical address as requested by the AMC specification.

(to be continued)

4 Hardware

4.1 Memory Map

All addresses are set up by programming the corresponding Chip-Select Decoders of the PowerQUICC III.

Table 3: Memory Map

Device	CS Line	Address	Function	Notes
Main FLASH	LCS0	programmable	Boot, user code	16 – 64 MByte FLASH PROM (16 bit wide)
IDT 82P2288	LCS1	programmable	8 x E1 framer	8 bit wide
Registers	LCS2	programmable	CPLD registers	8 bit wide
FPGA	LCS3	programmable	iTDM / local TDM / misc. registers	16 bit wide
FPGA	LCS4 - LCS7	programmable	for future use	TBD
SDRAM	MCS0	programmable	DDR SDRAM	64 bit wide
not used	MCS1 - MCS3	not used		

4.2 Definition of PowerQUICC III Port Pins

PowerQUICC II port pins are used to communicate with the framers and to set up some board configuration. In detail:

Table 4: PowerQUICC III Port Pin Usage (Port A)

Signal Function	PowerQUICC III Port A Pin	Description
not used	PA31	*pin is unconnected*
not used	PA30	*pin is unconnected*
not used	PA29	*pin is unconnected*
not used	PA28	*pin is unconnected*
not used	PA27	*pin is unconnected*
not used	PA26	*pin is unconnected*
not used	PA25	*pin is unconnected*
not used	PA24	*pin is unconnected*
not used	PA23	*pin is unconnected*
not used	PA22	*pin is unconnected*
not used	PA21	*pin is unconnected*
not used	PA20	*pin is unconnected*
not used	PA19	*pin is unconnected*
not used	PA18	*pin is unconnected*
not used	PA17	*pin is unconnected*
not used	PA16	*pin is unconnected*
not used	PA15	*pin is unconnected*
not used	PA14	*pin is unconnected*
not used	PA13	*pin is unconnected*
not used	PA12	*pin is unconnected*
not used	PA11	*pin is unconnected*
not used	PA10	*pin is unconnected*
TDM_A1_TX	PA9	MCC Channel A1
TDM_A1_RX	PA8	MCC Channel A1
TDM_SYNC0	PA7	MCC Sync
TDM_SYNC0	PA6	MCC Sync
not used	PA5	*pin is unconnected*
not used	PA4	*pin is unconnected*
TDM_CLK1	PA3	MCC Clock
TDM_CLK1	PA2	MCC Clock
not used	PA1	*pin is unconnected*
not used	PA0	*pin is unconnected*

Table 5: PowerQUICC II Port Pin Usage (Port B)

Signal Function	PowerQUICC II Port B Pin	Description
TDM_B2_TX	PB31	MCC Channel B2
TDM_B2_RX	PB30	MCC Channel B2
TDM_SYNC1	PB29	MCC Sync
TDM_SYNC1	PB28	MCC Sync
TDM_C2_TX	PB27	MCC Channel C2
TDM_C2_RX	PB26	MCC Channel C2
TDM_SYNC1	PB25	MCC Sync
TDM_SYNC1	PB24	MCC Sync
TDM_D2_TX	PB23	MCC Channel D2
TDM_D2_RX	PB22	MCC Channel D2
TDM_SYNC1	PB21	MCC Sync
TDM_SYNC1	PB20	MCC Sync
not used	PB19	*pin is unconnected*
not used	PB18	*pin is unconnected*
TDM_CLK1	PB17	MCC Clock
TDM_CLK1	PB16	MCC Clock
TDM_C1_TX	PB15	MCC Channel C1
TDM_C1_RX	PB14	MCC Channel C1
TDM_SYNC0	PB13	MCC Sync
TDM_SYNC0	PB12	MCC Sync
TDM_D1_TX	PB11	MCC Channel D1
TDM_D1_RX	PB10	MCC Channel D1
TDM_SYNC0	PB9	MCC Sync
TDM_SYNC0	PB8	MCC Sync
TDM_A2_TX	PB7	MCC Channel A2
TDM_A2_RX	PB6	MCC Channel A2
TDM_SYNC1	PB5	MCC Sync
TDM_SYNC1	PB4	MCC Sync

Table 6: PowerQUICC II Port Pin Usage (Port C)

Signal Function	PowerQUICC II Port C Pin	Description
TDM_CLK0	PC31	MCC Clock
TDM_CLK0	PC30	MCC Clock
TDM_CLK0	PC29	MCC Clock
TDM_CLK0	PC28	MCC Clock
TDM_CLK0	PC27	MCC Clock
TDM_CLK0	PC26	MCC Clock
TDM_CLK0	PC25	MCC Clock
TDM_CLK0	PC24	MCC Clock
not used	PC23	*pin is unconnected*
not used	PC22	*pin is unconnected*
not used	PC21	*pin is unconnected*
not used	PC20	*pin is unconnected*
TDM_CLK1	PC19	MCC Clock
TDM_CLK1	PC18	MCC Clock
TDM_CLK1	PC17	MCC Clock
TDM_CLK1	PC16	MCC Clock
CTS1	PC15	CTS SCC1
not used	PC14	*pin is unconnected*
not used	PC13	*pin is unconnected*
not used	PC12	*pin is unconnected*
not used	PC11	*pin is unconnected*
not used	PC10	*pin is unconnected*
not used	PC9	*pin is unconnected*
not used	PC8	*pin is unconnected*
CONF_DONE	PC7	FPGA Programming Interface
STATUS	PC6	FPGA Programming Interface
ASDI	PC5	FPGA Programming Interface
DATAO	PC4	FPGA Programming Interface
CSO	PC3	FPGA Programming Interface
CONFIG	PC2	FPGA Programming Interface
CECONF	PC1	FPGA Programming Interface
DCLK	PC0	FPGA Programming Interface

Table 7: PowerQUICC II Port Pin Usage (Port D)

Signal Function	PowerQUICC II Port D Pin	Description
RXD1	PD31	receive data, SCC1
TXD1	PD30	transmit data, SCC1
RTS1	PD29	RTS SCC1
Reserved	PD28	reserved for future use
Reserved	PD27	reserved for future use
not used	PD26	*pin is unconnected*
not used	PD25	*pin is unconnected*
not used	PD24	*pin is unconnected*
not used	PD23	*pin is unconnected*
Reserved	PD22	reserved for future use
Reserved	PD21	reserved for future use
not used	PD20	*pin is unconnected*
SPISEL	PD19	*pin is unconnected*
SPICLK	PD18	SPI Bus, Clock
SPIMOSI	PD17	SPI Bus, Data Out
SPIMISO	PD16	SPI Bus, Data In
SDA_CPM	PD15	I^2C Bus, data
SCL_CPM	PD14	I^2C Bus, clock
TDM_B1_TX	PD13	MCC Channel B1
TDM_B1_RX	PD12	MCC Channel B1
TDM_SYNC0	PD11	MCC Sync
TDM_SYNC0	PD10	MCC Sync
Reserved	PD9	reserved for future use
not used	PD8	*pin is unconnected*
not used	PD7	*pin is unconnected*
not used	PD6	*pin is unconnected*
not used	PD5	*pin is unconnected*
not used	PD4	*pin is unconnected*

4.3 Interrupt Structure

The **NAMC-8560-8E1/T1/J1** has the following interrupt structure:

Table 8: Interrupt Structure

Interrupt source	PowerQUICC III Interrupt level
NC	IRQ-Level 0 (highest level)
NC	IRQ-Level 1
IDT82P2288 Framer	IRQ-Level 2
TSI FPGA	IRQ-Level 3
MC92604 PHY	IRQ-Level 4
INTA from PCIe or FPGA	IRQ-Level 5
NC	IRQ-Level 6
NC	IRQ-Level 7
NC	IRQ-Level 8 (lowest level)

4.4 AMC Port Definition

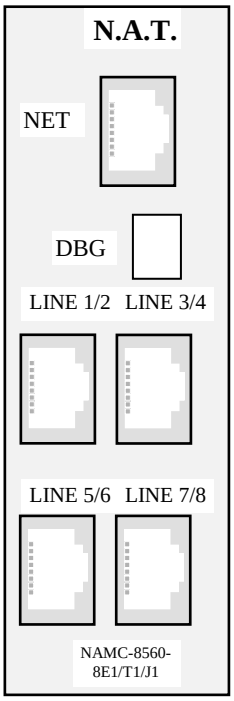
Table 9: AMC Port Definition

	Port No.	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1
	CLK2		Reference Clock 2
	CLK3		Reference Clock 3
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and Type P), default
	1		1000BaseX Ethernet Channel 2 (iTDM and Type P), redundant
	2		unassigned
	3		unassigned
	4	Fat Pipes	PCI Express Lane 0, default
	5		unassigned
	6		unassigned
	7		unassigned
Extended Connector	8	Region	PCI Express Lane 0, redundant
	9		unassigned
	10		unassigned
	11		unassigned
	12	Extended Options Region	TDM Bus D0-3 (H.110 extended)
	13		TDM Bus D4-7 (H.110 extended)
	14		optional clock lines (H.110 extended)/ unassigned
	15		Unassigned
	CLK4/5		Unassigned
	17		Unassigned
	18		optional clock lines (Rear I/O)/ unassigned
	19		Rear I/O (TDM P2P/E1 Framer)
	20		Rear I/O (SPI)

4.5 Front Panel and LEDs

The **NAMC-8560-8E1/T1/J1** module is equipped with 8 LEDs, which are completely software programmable. They are integrated in the 4 RJ45 E1/T1/J1 line interface jacks.

Figure 4: Front Panel



Connectors:

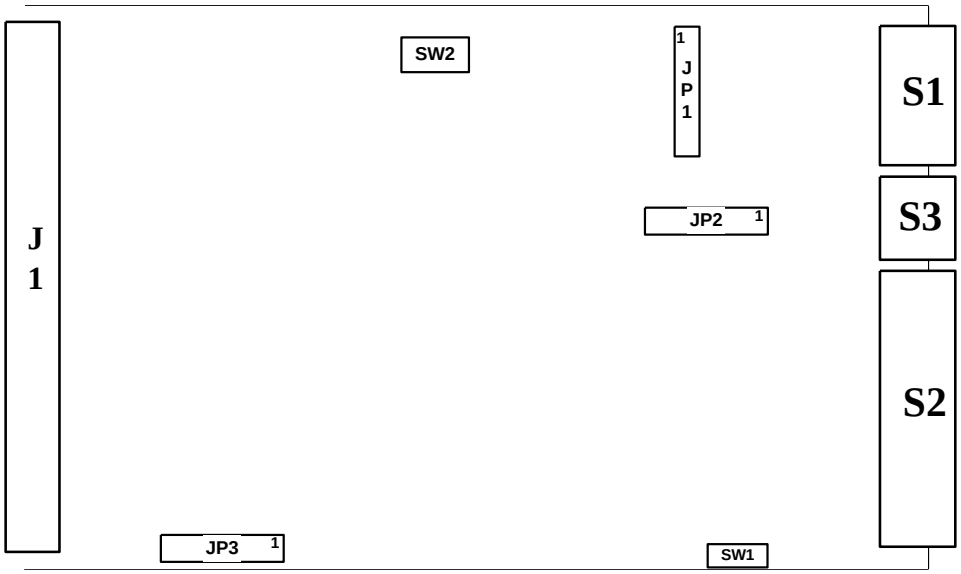
NET	The RJ45 connector S1 connects to an 100BaseT Ethernet network.
DBG	The Mini USB connector S3 connects to an RS232 debug interface.
LINE 1/2, LINE 3/4 LINE 5/6, LINE 7/8	The RJ45 connectors S2a – S2d carry the 8 E1/T1/J1 interfaces. Each 2 interfaces share one connector. There is one LED for every line interface.

Please refer to Chapter 5.8 for details on front panel connectors.

5 Connectors

5.1 Connector Overview

Figure 5: Connectors of the NAMC-8560-8E1/T1/J1



Please refer to the following tables to look up the connector pin assignment of the **NAMC-8560-8E1/T1/J1**.

5.2 AMC Connector J1

Table 10: AMC Connector J1

Pin No.	AMC-Signal	AMC-Signal	Pin No.
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	/SPISEL	163
9	PWR	SPICLK	162
10	GND	GND	161
11	XLINK1_P	SPIMOSI	160
12	XLINK1_N	SPIMISO	159
13	GND	GND	158
14	RLINK1_P	PORT19TX_P	157
15	RLINK1_N	PORT19TX_N	156
16	GND	GND	155
17	GA1	PORT19RX_P	154
18	PWR	PORT19RX_N	153
19	GND	GND	152
20	XLINK2_P	PORT18TX_P	151
21	XLINK2_N	PORT18TX_N	150
22	GND	GND	149
23	RLINK2_P	PORT18RX_P	148
24	RLINK2_N	PORT18RX_N	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134

Pin No.	AMC-Signal	AMC-Signal	Pin No.
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PET0_P_P4	RESVD	127
45	PET0_N_P4	TDM_REF	126
46	GND	GND	125
47	PER0_P_P4	TDM_FS	124
48	PER0_N_P4	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	PER1_P	TDM5	118
54	PER1_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	CLK_1_P	NC	97
75	CLK_1_N	NC	96
76	GND	GND	95
77	CLK_2_P	NC	94
78	CLK_2_N	NC	93

Pin No.	AMC-Signal	AMC-Signal	Pin No.
79	GND	GND	92
80	CLK_3_P	PET0_P_P8	91
81	CLK_3_N	PET0_N_P8	90
82	GND	GND	89
83	/PS0	PER0_P_P8	88
84	PWR	PER0_N_P8	87
85	GND	GND	86

5.3 Connector JP1: Altera FPGA Programming Port

Connector JP2 connects the JTAG- or programming-port of the Altera FPGA CPLD device.

Table 11: Altera FPGA Programming Port

Pin No.	Signal	Signal	Pin No.
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATAO	/CSO	8
9	ASDI	GND	10

5.4 Connector JP2: Lattice programming port

Connector JP2 connects the JTAG- or programming-port of the Lattice CPLD devices. The CPLD devices are connected to a TDI – TDO daisy-chain.

Table 12: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	nc	nc	10

5.5 Connector JP3: BDM and JTAG connector

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufactorers.

Table 13: Development Port / BDM Connector Pinout

Pin No.	Signal	Signal	Pin No.
1	TDO	nc	2
3	TDI	/TRST	4
5	nc	+3.3V	6
7	TCK	/CKSTP_IN	8
9	TMS	nc	10
11	/SRESET	nc	12
13	/HRESET	nc	14
15	/CKSTP_OUT	GND	16

5.6 Hot Swap Switch SW1

Switch SW1 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

5.7 DIL Switch SW2

5.7.1 Boot FLASH Select Switch (SW2 Switch 1)

By switching switch no. 1 of DIL switch SW2 to ON, the upper half of the Boot FLASH is selected for booting. If switch no. 1 of DIL switch SW2 is switched to OFF, the lower half of the Boot FLASH is selected for booting.

Default:

Switch no. 1 of DIL switch SW2 is switched to OFF, lower half of the Boot FLASH is selected for booting.

5.7.2 PCIe Bridge Direction Switch (SW2 Switch 2)

This switch is used to set the direction of system functions (Forward Bridge, Reverse Bridge). This functionality is preliminary and subject to change. Please refer to the PEX8111 Data Book for more information.

Default:

Switch no. 2 of DIL switch SW2 is switched to OFF, Forward Bridge operation selected

5.8 The Front Panel Connectors (S1 – S3)

5.8.1 The Ethernet Connector S1

Table 14: shows the pin assignment of RJ45-connector S1. This connector carries the 1000BaseT signals of the Ethernet interface. Term. is the 100BaseT termination used for pins 4, 5, 7, and 8.

Table 14: Pin Assignment of the Front-panel Connectors S3 (Ethernet)

Pin No.	Signal	Signal	Pin No.
1	MX0+	MX0-	2
3	MX1+	MX2+	4
5	MX2-	MX1-	6
7	MX3+	MX3-	8

5.8.2 The ISDN Connector S2

The ISDN front panel connectors are 8-pin RJ45 connectors. The 8 E1/T1/J1 line interfaces are available on the pins of the front panel connectors S2a – S2d. Table 15: - Table 18: show the pin assignments.

Table 15: Pin Assignment of the Front-panel Connectors S2a (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX0+	TX0-	2
3	TX1+	RX1+	4
5	RX1-	TX1-	6
7	RX0+	RX0-	8

Table 16: Pin Assignment of the Front-panel Connectors S2b (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX2+	TX2-	2
3	TX3+	RX3+	4
5	RX3-	TX3-	6
7	RX2+	RX2-	8

Table 17: Pin Assignment of the Front-panel Connectors S2c (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX4+	TX4-	2
3	TX5+	RX5+	4
5	RX5-	TX5-	6
7	RX4+	RX4-	8

Table 18: Pin Assignment of the Front-panel Connectors S2d (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX6+	TX6-	2
3	TX7+	RX7+	4
5	RX7-	TX7-	6
7	RX6+	RX6-	8

5.8.3 The RS232 Connector S3

Table 19: shows the pin assignment of the signals of the RS232 interface.

Table 19: Pin Assignment of the Front-panel Connector S3 (RS232)

Pin No.	Signal	Signal	Pin No.
1	RTS_SCC1	RxD_SCC1	2
3	TxD_SCC1	CTS_SCC1	4
5	GND		

Front Panel Connector S3 is connected to SCC1 of the MPC8560 CPM.

6 NAMC-8560-8E1/T1/J1 Programming Notes

6.1 Setup of the Serial Interfaces

6.1.1 RS232 Interface on the Front Panel Connector S3

The programming of the RS232 serial interface is performed through SCC1 (PC15, PD29 – PD31).

6.1.2 I^2C Interfaces

There are 2 I^2C interfaces connected to the MPC8560 CPU. The 1st one connects to an EEPROM of 8 kBit size. The address of this EEPROM used for storage of board-specific parameters is 0. The control code (1st 4 bits of the address) for the 24C08 EEPROM is 1010b, which results in address $50 for the parameter EEPROM.
The second I^2C interface is connected to port pins PD14 (Clk) and PD15 (Data). This I^2C interface is routed to the FPGA for future use.

6.1.3 SPI Interface

The SPI interface is connected to port pins PD16 (SPIMISO), PD17 (SPIMOSI), PD18 (SPICLK), and PD19 (/SPISEL). It is routed to the FPGA for future use.

Note:

This chapter will be completed in a later version of the User's Manual. For the time being, contact N.A.T. for further assistance on programming NAMC-8560-8E1 devices.

6.2 CPLD Registers

6.2.1 PCB Version Register

There is an 8 bit wide PCB Version Register implemented in the CPLD onboard the **NAMC-8560-8E1/T1/J1**, which contains the revision code of the PCB. This code reads decimally-coded in 2 nibbles, i.e. the PCB version V1.0 reads 0x10. The register is addressed by the Register Chip Select CS4 as described in Table 3: with address offset 0x0.

Table 20: PCB Version Register

PCB Version – Address Offset 0x0								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB Version Major				PCB Version Minor			

6.2.2 CPLD Version Register

There is an 8 bit wide Lattice CPLD Version Register implemented in the CPLD onboard the **NAMC-8560-8E1/T1/J1**, which contains the revision code of the Lattice CPLD. This code reads decimally-coded in 2 nibbles, i.e. the CPLD version V1.0 reads 0x10. The register is addressed by the Register Chip Select CS4 as described in Table 3: with address offset 0x8.

Table 21: CPLD Version Register

CPLD Version – Address Offset 0x8								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	CPLD Version Major				CPLD Version Minor			

6.2.3 CPLD Status/Control Register 1

This 8-Bit register holds the status of the Freescale MC92604 Ethernet PHY strapping pins. If reprogrammed, a PHY Reset has to be performed, in order for the strapping pin settings to take effect. This can be achieved by programming CPLD Status/Control Register 2.

Table 22: CPLD Status/Control Register 1

CPLD Status/Control Register 1 – Address Offset 0x10								
Default value 0x39								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Reset Value	0	0	1	1	1	0	0	1
Func	-	-	REC_CLK_ CENT	RCCE	EN_RED_LI	BROADCAST	MEDIA	EN_AN

REC_CLK_CENT – EN_AN — Backplane Ethernet PHY strapping pins, refer to Freescale MC92604 User's Manual for details

6.2.4 CPLD Status/Control Register 2

This 8-Bit register allows the user to reset the Ethernet and PCIe I/O devices. There is a separate Reset bit for each device. Furthermore, a reload of the FPGA code may be initiated.

Table 23: CPLD Status/Control Register 2

CPLD Status/Control Register 2 – Address Offset 0x18								
Default value 0x0								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Power-On Reset Value	0	0	0	0	0	0	0	0
Func	-	-	-	RES_ALL	FPGA_RECONF	RES_BPPHY	RES_NPHY	PERST

RES_BPPHY — Backplane Ethernet PHY Reset; writing a '1' to this bit will reset the Freescale MC92604 Ethernet PHY. The Reset is automatically removed after some microseconds.

RES_NPHY — Front Panel Ethernet PHY Reset; writing a '1' to this bit will reset the National DP83865 Ethernet PHY. The Reset is automatically removed after some microseconds.

PERST — PCIe Reset; writing a '1' to this bit will assert the /PERST signal to the PLX PEX8111 PCIe to PCI Bridge. The Reset is automatically removed after some microseconds.

FPGA_RECONF — Reconfiguration of the FPGA, writing a '1' to this bit will assert the /CONFIG signal to the EP2C70 FPGA. The signal is automatically removed after some microseconds.

RES_ALL — Reset of the board, writing a '1' to this bit will assert all resets on the board, except the IPMI-µC. The signal is automatically removed after some microseconds.

6.3 Programming the FPGA Interface

The FPGA on the **NAMC-8560-8E1/T1/J1** contains a legacy timeslot interchanger (TSI) beside an iTDM-to-TDM conversion engine. The table below shows the memory map for the logical sub-blocks of the design. Refer to the following sub-chapters for detailed information.

Table 24: FPGA Memory Map

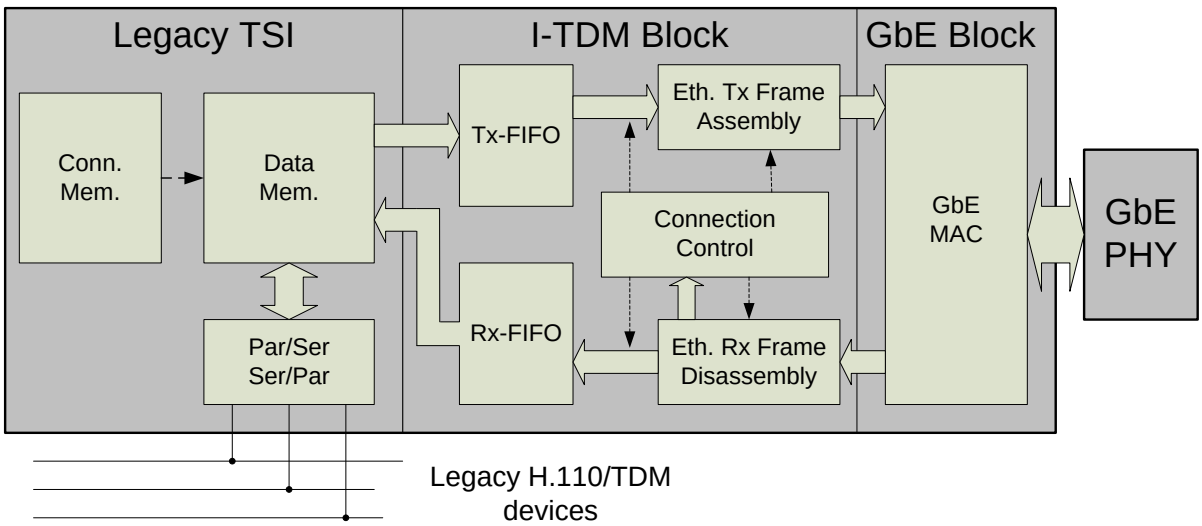
Address Offset	Logical Block
0x00000	General Purpose Status
0x00100	General Purpose Registers
0x01000	Interface to FPGA PROM
0x10000	GbE-Interface Block
0x20000	Local-TDM Block
0x80000	iTDM Block

The FPGA-Design consists of four main blocks:

- Misc. board control- and status registers, and a register-interface to access the FPGA's PROM
- GbE-MAC and frame preprocessing block
- Legacy Timeslot Interchanger (TSI)
- iTDM block

TDM-connections between the local TDM-devices (8E1-Framer, CPU MCC) and the legacy H.110-like TDM bus implemented on AMC-Ports 12-14 can be established by only using the legacy TSI. To route one of the legacy TDM timeslots over iTDM, this timeslot first has to be connected to a free iTDM timeslot within the legacy TSI, and then to be converted by the iTDM engine.

Figure 6: Organisation of the (i)TDM FPGA



6.3.1 TSI Data Line Usage

The following picture shows the TDM interconnect on the **NAMC-8560-8E1/T1/J1** with the FPGA-TSI being the central switching matrix. The board-specific information given below must be combined with the general FPGA-TSI functionality as described in the FPGA-TSI Manual (Appendix A, [11]).

Figure 7: TSI TDM Interconnect

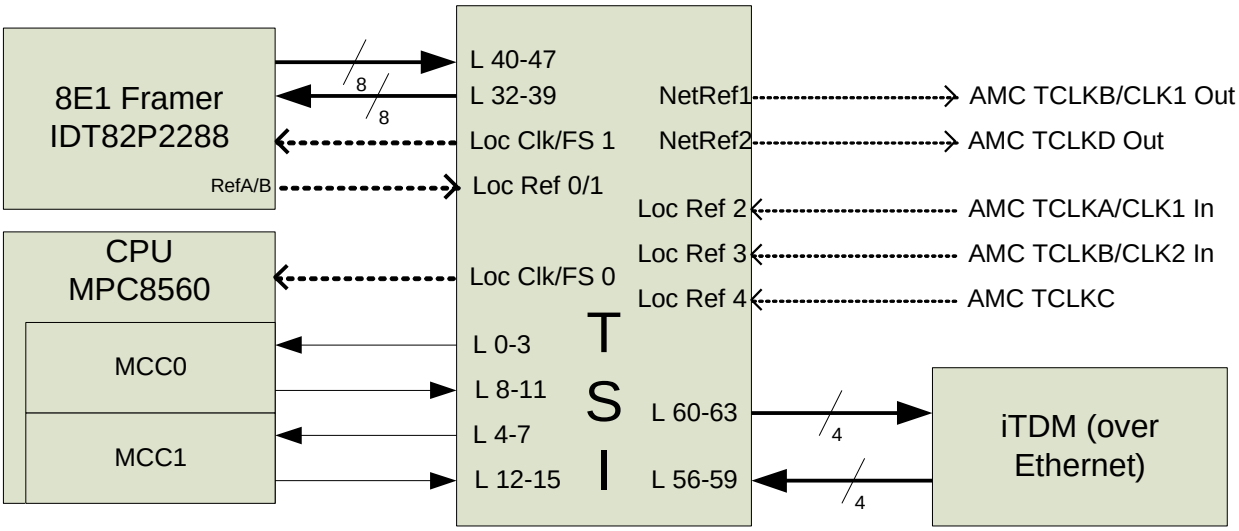


Table 25: Local TDM Structure

TSI data line	Connected TDM Device	TDM Channel	Direction from FPGA-TSI	Sync for TDM Channel	Clock for TDM Channel
Line 0-3	MPC8560	TDM_A1_Rx	Output	L_FS1	L_CLK1
Line 4-7	MPC8560	TDM_A2_Rx	Output	L_FS1	L_CLK1
Line 8-11	MPC8560	TDM_A1_Tx	Input	L_FS1	L_CLK1
Line 12-15	MPC8560	TDM_A2_Tx	Input	L_FS1	L_CLK1
Line 32-39	8E1 Framer	LIF 0-7 Tx	Output	L_FS0	L_CLK0
Line 40-47	8E1 Framer	LIF 0-7 Rx	Input	L_FS0	L_CLK0
Line 56-59	iTDM	TimeSlot 0-511 Rx	Input	internal	internal
Line 60-63	iTDM	TimeSlot 0-511 Tx	Output	internal	internal

6.3.2 FPGA GP Registers/Status

This chapter describes the basic board control registers implemented within the FPGA. Further register description will follow up in future versions of this manual.

6.3.2.1 FPGA Version Register

The Version Register holds the FPGA Revision, encoded in two nibbles.

Table 26: FPGA Version Register

FPGA Version - Address 0x00			
Default value 0x0015			
Bit	15..8	7..4	3..0
Access	R	R	R
Func	**reserved**	**Version Major**	**Version Minor**

6.3.2.2 FPGA ID_1 Register

This read only register can be used by the device driver to probe register access.

Table 27: FPGA ID_1 Register

FPGA ID_1 - Address 0x02	
Default value 0xAA55	
Bit	15..0
Access	R
Func	**ID_1**

6.3.2.3 FPGA ID_2 Register

This read only register can be used by the device driver to probe register access.

Table 28: FPGA ID_2 Register

FPGA ID_2 - Address 0x04	
Default value 0xDEAD	
Bit	15..0
Access	R
Func	**ID_2**

6.3.2.4 FPGA BOARD_ID Register

This read only register can be used by the device driver to probe register access. it hold the N.A.T. internal board-id of the **NAMC-8560-8E1/T1/J1.**

Table 29: FPGA BOARD_ID Register

FPGA BOARD_ID - Address 0x06	
Default value 0x0B01	
Bit	15..0
Access	R
Func	**BOARD_ID**

6.3.2.5 FPGA Reset Register

The Reset Register is used to trigger a reset to the whole FPGA logic, FPGA blocks, or external devices. Writing a '1' to a bit triggers the reset. After reset, the bit is self-cleared to '0'.

Table 30: FPGA Reset Register

Reset – Address Offset 0x100								
Default value 0x0000								
Bit	15..7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**reserved**	**IPMI-µC**	**8E1-Framer**	**ZPLL**	**TSI**	**GbE**	**iTDM**	**FPGA global**

6.3.2.6 AMC LEDs Register

This register is used to control the AMC LEDs 3 (most upper; yellow) and 2 (second from top; green) on the AMC module front panel.
Note: the other two AMC LEDs (LED 1 and LED blue) are controlled by the IPMI-µC.

Table 31: AMC LEDs Register

AMC LEDs - Address 0x108			
Default value 0x0000			
Bit	15..8	7..4	3..0
Access	R/W	R/W	R/W
Func	**reserved**	**LED AMC 3**	**LED AMC 2**

The AMC LEDs can be configured to the functionality listed below:

Table 32: AMC LED Values

Value	AMC-LED2 Function	AMC-LED3 Function
0x0	TDM-PLL Lock Status	PCIe Link Status
0x1	on	on
0x2	off	off
others	reserved	reserved

6.3.2.7 E1 LEDs Register

This register is used to control the LEDs integrated in the RJ45 connectors that hold the 8E1 interfaces. Writing a '1' to a bit switches the respective LED on.

Table 33: E1 LEDs Register

E1 LEDs - Address 0x10a									
Default value 0x0000									
Bit	15..8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**reserved**	**LED E1 8**	**LED E17**	**LED E1 6**	**LED E1 5**	**LED E1 4**	**LED E1 3**	**LED E1 2**	**LED E1 1**

6.3.2.8 Ethernet LEDs Register

This register is used to control the LEDs integrated in the RJ45 connector that hold the front panel Ethernet interface. These LEDs are bicolor devices and the table below shows the possible color modes.

Table 34: Ethernet LEDs Register

Ethernet LEDs - Address 0x10c			
Default value 0x0000			
Bit	15..8	7..4	3..0
Access	R	R/W	R/W
Func	**reserved**	**left Eth LED**	**right Eth LED**

Table 35: Ethernet LEDs Values

Value	LED Function
0x0	PHY Link Status
0x1	orange
0x2	green
0x3	off
others	reserved

6.3.3 FPGA GbE/iTDM Configuration

For configuration and programming of the GbE/iTDM block please refer to the N.A.T. iTDM-FPGA Manual (Appendix A, [12], NDA required).

6.3.4 FPGA Legacy TSI Configuration

For configuration and programming of the Legacy-TSI block please refer to the N.A.T. FPGA-TSI Manual (Appendix A, [11]).

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] Freescale, MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual, 7/2004, Rev. 1
[2] Altera, Cyclone II Device Handbook, 11/2005, Rev. 2.1
[3] Samsung, DDR SDRAM 512 MB C-die, Rev. 1.1, 6/2005
[4] National Semiconductor, DP83865 Gig Phyter V, 10/2004
[5] Freescale, MC92604 Dual Gigabit Ethernet Transceiver Reference Manual, Rev. 1, 6/2005
[6] Atmel, Atmega48/88/168/V Product Data, Rev. 2545G, 06/06
[7] PLX Technology, PEX8111BB, PCI Express to PCI/PCI-X Bridge, Data Book, 6/2006, Rev. 1.2
[8] Zarlink, ZL30100 T1/E1 System Synchronizer, Data Sheet, 11/2005
[9] Traco Power DC/DC Converters, TOS Series, POL Converter, Rev. 10/05
[10] IDT, Octal T1/E1/J1 Long Haul / Short Haul Transceiver IDT82P2288, Ver. 3, 3/2004
[11] Spansion, S29GL-N MirrorBit Flash Family Data Sheet, Rev. B, Am. 3, 10/2006
[12] N.A.T., FPGA-TSI Technical Reference Manual, March 2005, Ver. 1.0
[13] N.A.T., iTDM-FPGA Technical Reference Manual, October 2006, Ver. 1.0

Appendix B: Document's History

Revision	Date	Description	Author
1.0	02.05.2006	initial revision	ga
1.1	16.08.2006	adapted to HW Rev. 1.1	ga
1.2	25.10.2006	description of CPLD and FPGA interfaces added	ga/te
1.3	13.03.2007	adapted to HW Rev. 1.2, chapter 2.3 added	ga
1.4	20.06.2007	added functionality to CPLD and FPGA, fixed error in E1 port description	te
1.5	20.11.2007	modified register interface of FPGA	te
1.6	09.01.08	added information for thermal requirements; added compliance statements	te
1.7	29.04.09	Corrected E1 jack description; changed local tdm line assignments	te
1.8	17.08.09	Corrected AMC Clock to TSI Clock assignment description	te