NPMC-8E1/T1/J1

P(T)MC Module for Telecom Applications
Technical Reference Manual V1.5
Hardware Revision V1.1

The NPMC-8E1/T1/J1 has been designed by:

N.A.T. GmbH
Kamillenweg 22
D-53757 Sankt Augustin

Phone: ++49/2241/3989-0
Fax: ++49/2241/3989-10

E-Mail: support@nateurope.com
Internet: http://www.nateurope.com

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

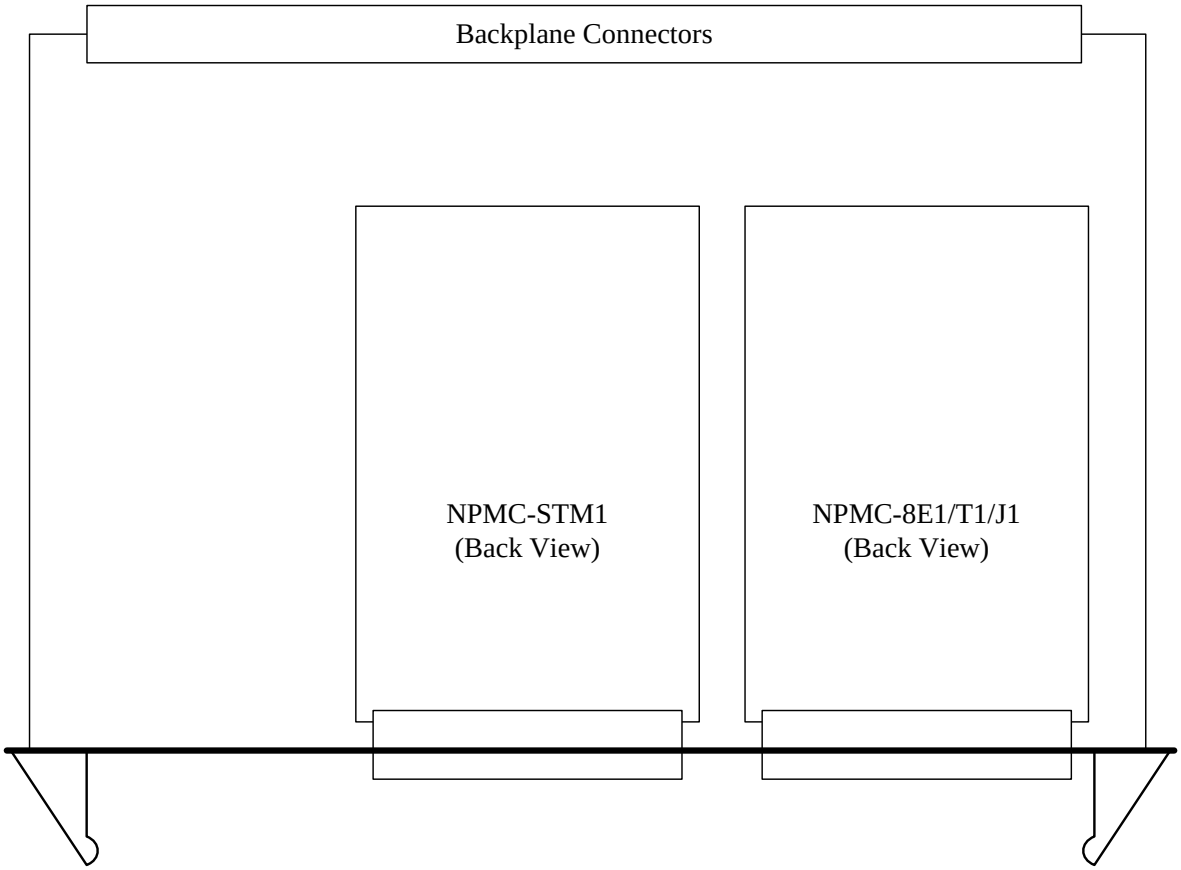
Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
E1	2.048 Mbit G.703 Interface
H.110	Time-Slot Interchange Bus
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCSA	Signal Computing System Architecture
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner

1 Introduction

The **NPMC-8E1/T1/J1** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

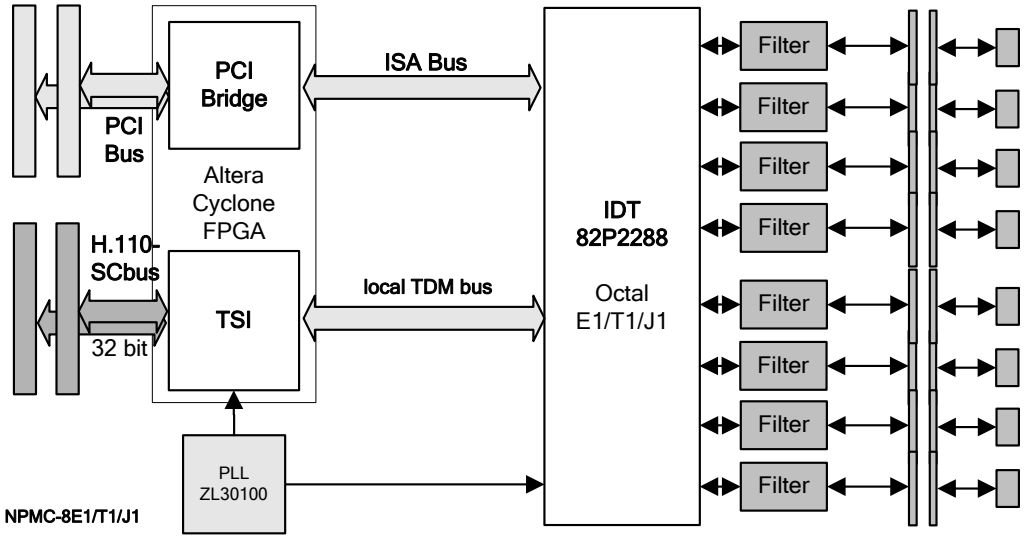
Figure 1: NPMC-8E1/T1/J1 on a carrier board (VMEbus, cPCI)



The **NPMC-8E1/T1/J1** has the following major features on-board:

- 8 x E1 / T1 / J1 primary rate line interface
- Front-panel I/O
- 32 bit / 33 MHz PCI Bus interface Rev. 2.2
- H.110 / SCSA TSI bus

Figure 2: NPMC-8E1/T1/J1 Block Diagram



1.1 Board Features

- **Interfaces**

  PCI: The **NPMC-8E1/T1/J1** includes a 32 bit 33 MHz PCI bus interface. This is implemented by an FPGA solution based on an Altera Cyclone FPGA device.

  H.110/SCSA: The **NPMC-8E1/T1/J1** implements a 32 bit H.110 interface, which includes a SCbus interface on I/O-connector P14 according to PMC specifications. This is implemented in the Altera Cyclone FPGA device. The H.110 interface is also available on PMC connector P13 according to PTMC configurations 3 and 5. PTID coding is configuration 5.

  SPI: The **NPMC-8E1/T1/J1** implements a SPI bus interface on the PMC I/O connector P14, which connects to the Altera Cyclone FPGA.

- **I/O**

  E1/T1/J1: The module carries a IDT 82P2288 framer, which implements eight E1/T1/J1 interfaces.

1.2 Board Specification

Table 2: NPMC-8E1/T1/J1 Features

PMC-Module	Standard PCI Mezzanine Card Type 1	
Front-I/O	4 RJ45 connectors	
Rear-I/O	H.110 and SCbus (32 bit) on P14, support of PTMC interface configurations 3 and 5 on P13. PTID coding is configuration 5.	
PCI to PMC bus bridge	Altera Cyclone 1C12 FPGA	
H.110 TSI	Altera Cyclone 1C12 FPGA	
Firmware	OK1, VxWorks driver (on request)	
Power consumption	3.3V 1.0A typ. 5.0V 0.1A typ.	
Environmental conditions	Temperature (operating):	0°C to +60°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PCI Rev. 2.2 IEEE P1386.1 / Draft 2.4a, PICMG 2.15 R1.0	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NPMC-8E1/T1/J1** during its usual life-time take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NPMC-8E1/T1/J1** read this installation section
- Before installing or uninstalling the **NPMC-8E1/T1/J1**, read the Installation Guide and the User's Manual of the carrier board used
- Before installing or uninstalling the **NPMC-8E1/T1/J1** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-8E1/T1/J1** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-8E1/T1/J1**
- power supply

2.2.2 Power supply

The power supply for the **NPMC-8E1/T1/J1** must meet the following specifications:

- required for the module:
  - +3,3V / 1.0A typical
  - +5,0V / 0.1A typical

2.2.3 Automatic Power Up

In the following situations the **NPMC-8E1/T1/J1** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V *
- when +5V voltage level rises above 5,6V *
- when +3.3V voltage level drops below 2,65V *
- when +3.3V voltage level rises above 3,9V *
- or when the carrier board signals a PCI Reset

Watchdog (if enabled)

* defined by: “PCI Specification Revision 2.2, Section 4.2.1.1 and Section 4.3.2”

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that whereever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly intergrated into larger and more complex envionments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

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2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

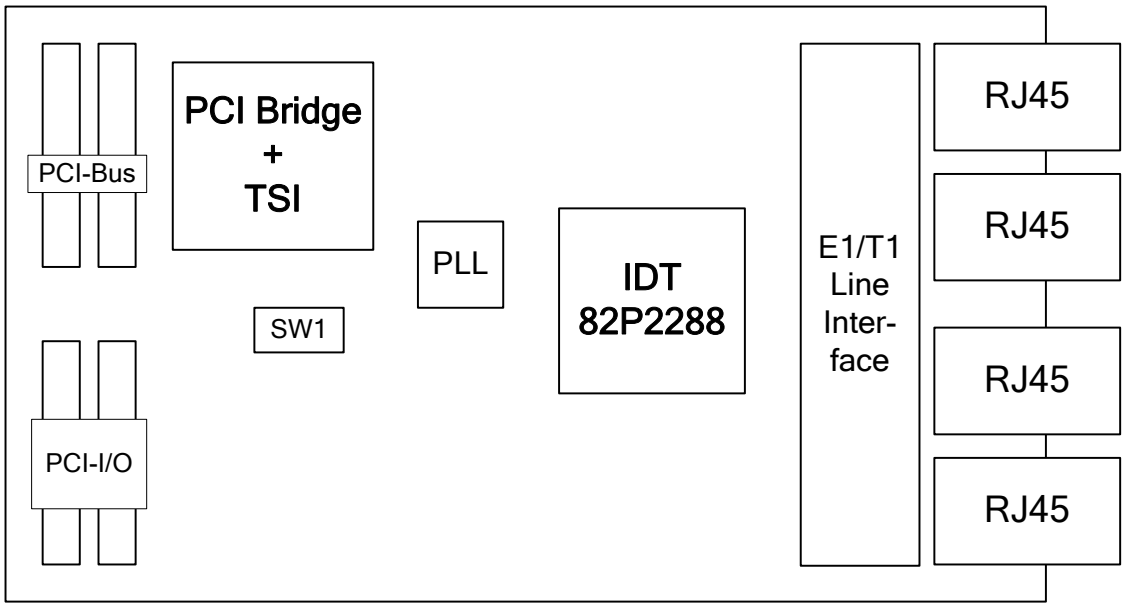
2.3.4 Product Safety

The board complies to EN60950 and UL1950.

2.4 Location Overview

The figure 3 "Location diagram of the **NPMC-8E1/T1/J1**" highlights the position of the important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: Location diagram of the NPMC-8E1/T1/J1



3 Functional Blocks

The **NPMC-8E1/T1/J1** can be divided into a number of functional blocks, which are described in the following paragraphs.

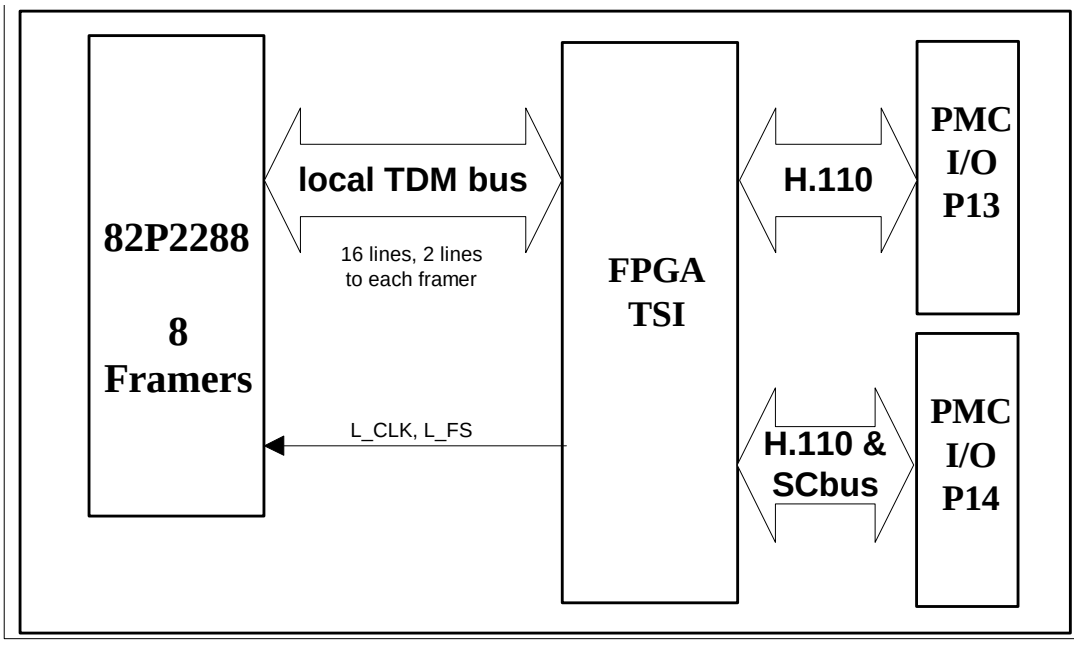
3.1 PCI Interface

The **NPMC-8E1/T1/J1** includes a 32 bit, 33 MHz PCI interface to connect to the carrier board. This is implemented by an Altera Cyclone FPGA and transfers to an ISA – like bus, which connects to the framer and to the TSI, which implements the TDM TSI and some control/status registers.

3.2 H.110 Bus Controller and Line Interfaces

3.2.1 Block Diagramm of the TDM Structure

Figure 4: Local TDM Bus Organisation and Synchronisation



3.2.2 Description of the TDM Structure

The TDM data are routed through the Altera Cyclone FPGA device, which implements a TSI device. Hence, any timeslot switching between H.110/SC bus and framer is possible. Local TDM data lines TDM[0 – 15] are routed between the framer and the TSI. The TSI device derives its time base either from the H.110/SC bus or from the framer. From this input it generates local clock and frame sync for the framer to synchronize to. Hence, the TSI implemented in the FPGA may be clock slave or clock master to the H.110 or SCbus on the carrier module. The sync and clock signals L_FS and L_CLK can be programmed within the FPGA control register settings.

The connection between the TDM data lines LD[0 – 15] and the corresponding serial channels Rx/Tx of the framer is shown in the following Table 3:

Table 3: TDM Channel ←→ Framer Serial Data Line Connection

TSI local TDM Channel	Framer serial channel	TSI local TDM Channel	Framer serial channel
LD8	RxSER1	LD0	TxSER1
LD9	RxSER2	LD1	TxSER2
LD10	RxSER3	LD2	TxSER3
LD11	RxSER4	LD3	TxSER4
LD12	RxSER5	LD4	TxSER5
LD13	RxSER6	LD5	TxSER6
LD14	RxSER7	LD6	TxSER7
LD15	RxSER8	LD7	TxSER8

3.2.3 SCbus Compatibility

The SCbus implemented on the **NPMC-8E1/T1/J1** is a subset of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D[0 – 15]. On the **NPMC-8E1/T1/J1**, the bus width has been extended to 32 bit, in order to make use of all the 32 data lines switching capabilities of the TSI device. See chapter 5.8 (PMC P14 Connector) for reference.

3.2.4 E1/T1/J1 Line Interfaces

The eight E1/T1/J1 interfaces connect the IDT 82P2288 framer to the front panel RJ45 connectors. Timing and interface characteristics can be set up by software within the 82P2288. The line interface is conform to EN60950 and G.703.

4 Hardware

4.1 Memory Map

Addresses are defined by programming the base and translation address registers which reside in the PCI configuration space of the Cyclone FPGA PCI bridge. This setting may be done by the user application-specific. If required the **NPMC-8E1/T1/J1** can be configured to implement a 4-byte-interleave mode via SW1_2 (see chapter 5.4). The memory window used to decode the devices given below requires 16kB in size for standard mode or 32kB if switched to 4-byte-interleave mode.
For the Framer's memory map please refer to Appendix A [1] (if 4-byte-interleave mode is enabled, all addresses in the framer's manual must be multiplied by **four**). For the FPGA-TSI memory map please refer to Appendix A [4] and to chapter 4.3.6 for the special implementation of the control-bits for the status LEDs located at the front panel (if 4-byte-interleave mode is enabled, all addresses in the FPGA-TSI's manual must be multiplied by **two**).

Table 4: Memory Map

Device	Address Offset normal mode	Address Offset 4-byte-interleave	Access in normal mode	Function
PCI FPGA	0x0000.0000	0x0000.0000	16 bit r/w	I/O register access
Framer	0x0000.1000	0x0000.2000	8 bit r/w	Framer Register access
TSI FPGA	0x0000.2000	0x0000.4000	16 bit r/w	TSI FPGA register access, routing memory

4.2 Interrupts

The **NPMC-8E1/T1/J1** wire-or's the framer interrupt and the TSI interrupt to the PMC /INTA signal. Each of these interrupts is software maskable not only in the framer and TSI devices themselves, but also in the PCI-FPGA, through which these interrupts are routed. By default, the interrupts are masked (disabled). Refer to chapter 4.3 for details on the PCI FPGA control/status registers.

4.3 Registers

4.3.1 I/O Register Overview

The following table gives an overview of all registers contained in the PCI-FPGA:

Table 5: I/O Register

Address (normal)	Address (4-byte-interl.)	Name	Access	Description
0x00	0x00	VER	r	Version Register
0x02	0x04	IRQ_Mask	r/w	Interrupt Mask Register (set '1' to enable Int.)
0x04	0x08	IRQ_Status	r	Interrupt Status Register (shows actual state of IRQ; '1' showing Interrupt is asserted)
0x06 – 0x0e	0x0c – 0x1c	reserved	r	reserved
0x10 – 0x1e	0x20 – 0x3c	GP_TIMER 0 - 7	r/w	IRQ is triggered after time written to register

4.3.2 Version Register

The Version Register shows the actual PCB and PCI-FPGA releases.

Table 6: Version Register

VER - Address 0x00																
Default value 0x1010																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Func	PCB Version								FPGA Version							

There is a 16 bit wide I/O-register that holds the PCB revision and the PCI-FPGA version implemented in the PCI-FPGA onboard the **NPMC-8E1/T1/J1**, which contains the revision code of the PCB in the bits [15-8] and the revision code of the PCI-FPGA in bits [7-0]. This code reads decimally-coded in 2 nibbles, i.e. the PCB version V1.0 reads 0x10. The register is addressed by address offset 0x0.

4.3.3 IRQ_Mask – Interrupt Mask Register

The Interrupt Mask Register allows the individual masking of the interrupt sources. Interrupt sources which are enabled are wired or'ed to the PCI /INTA pin, thus leading to a PCI interrupt. The source for the interrupt can be read from the IRQ-Status register.
The meaning of the individual bits is explained in the following table.

Table 7: IRQ_Mask Register

IRQ_Mask - Address 0x02 / 0x04																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W
Func	**IRQ Timer7**	**IRQ Timer6**	**IRQ Timer5**	**IRQ Timer4**	**IRQ Timer3**	**IRQ Timer2**	**IRQ Timer1**	**IRQ Timer0**	-	-	-	-	-	-	**IRQ TSI**	**IRQ Framer**

0 = Interrupt is disabled
1 = Interrupt is enabled

4.3.4 IRQ_Stat – Interrupt Status Register

By means of the IRQ_Stat register the status of the interrupt lines of the individual onboard interrupt sources can be determined. The value of a bit does not depend on the setting of the corresponding bit in the IRQ_Mask register. If a bit in the IRQ_Stat register is set (meaning Interrupt is asserted) and the corresponding bit in the IRQ_Mask register is enabled, the PCI interrupt line /INTA will be activated.
The following table shows the assignment of the register bits.

Table 8: IRQ_Stat Register

IRQ_Stat - Address 0x04 / 0x08																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Func	**IRQ Timer7**	**IRQ Timer6**	**IRQ Timer5**	**IRQ Timer4**	**IRQ Timer3**	**IRQ Timer2**	**IRQ Timer1**	**IRQ Timer0**	-	-	-	-	-	-	**IRQ TSI**	**IRQ Framer**

0 = no Interrupt asserted
1 = Interrupt is asserted

4.3.5 GP_TIMER Registers

Writing a value different from zero to one of this registers results in an interrupt being triggered after the value written in microseconds. The timer can be re-triggered once running by writing again to the register. The generated interrupt (after counting down to zero) is cleared by writing zero to the register; writing zero while the timer is running results in clearing and disabling the timer without generating an interrupt.

Table 9: GP_TIMER_N Registers

GP_TIMER_N - Address 0x10-0x1e / 0x20-0x3c																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**GP_TIMER_N**															

4.3.6 LED_Control – LED Mode Select Register

The LED_Cotrol register is implemented in one of the TSI's general purpose register at offset 0x1206 (0x240c in 4-byte-interleave mode) from the TSI's base address.
The following table shows the assignment of the register bits.

Table 10: LED_Control Register

LED_Control - Address (0x2000 + 0x1206) / (0x4000 + 0x240c)																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	**LED4 Mode [3..0]**				**LED3 Mode [3..0]**				**LED2 Mode [3..0]**				**LED1 Mode [3..0]**			

For each of the LEDs one of the following modes can be selected:

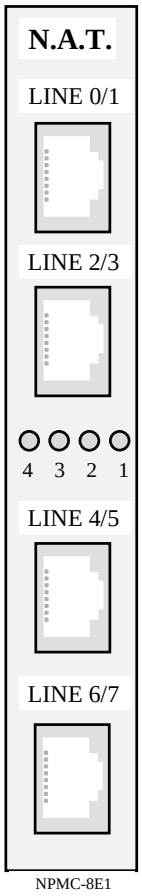
Table 11: LED available Modes

LED Mode [3..0]	pattern during ~2 seconds grey: on
0x0	
0x1	
0x2	
0x3	
0x4	
0x5	
0x6	
0x7	
0x8	
0x9	
0xa	
0xb	
0xc	
0xd	
0xe	
0xf	

4.4 Front Panel and LEDs

The **NPMC-8E1/T1/J1** module is equipped with 4 LEDs, which are completely software programmable. Thus their functionality depends very much of the application running on the module.

Figure 5: Front Panel and LEDs



LEDs:

LED 1 - 4 the green LEDs 1 – 4 are fully software programmable and their meaning depends on user application.

Connectors:

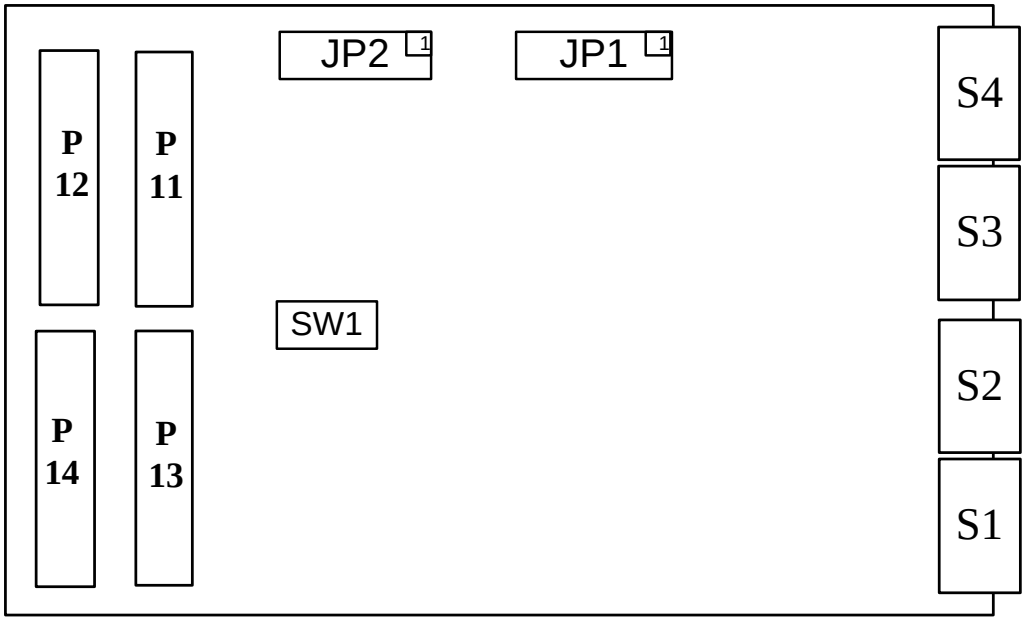
LINE 0/1, LINE 2/3, LINE 4/5, LINE 6/7 These RJ45 connectors S1 – S4 carry the 8 E1/T1/J1 interfaces. Each 2 interfaces share one connector.

Please refer to Chapter 5.9 for details on front panel connectors.

5 Connectors

5.1 Connector Overview

Figure 6: Connectors of the NPMC-8E1/T1/J1



Please refer to the following tables to look up the pin assignment of the **NPMC-8E1/T1/J1**.

5.2 Connector JP1: FPGA JTAG Port

Connector JP1 connects the JTAG-port of the FPGA device.

Table 12: TSI_FPGA JTAG port

Pin No.	Signal	Signal	Pin No.
1	TCK_A	GND	2
3	TDO_A	+3.3V	4
5	TMS_A	nc	6
7	nc	nc	8
9	TDI_A	GND	10

5.3 Connector JP2: FPGA Programming Port

Connector JP1 connects the programming-port of the FPGA device. It is used to program the serial EEPROM that stores the configuration-data of the FPGA.

Table 13: TSI_FPGA programming port

Pin No.	Signal	Signal	Pin No.
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATAO	/CSO	8
9	ASDI	GND	10

5.4 DIL Switch SW1: Enable PTMC-Mode / Enable Interleave

This dual DIL Switch is used in for selecting the TDM I/O configuration the **NPMC-8E1/T1/J1** uses and to enable the optional 4-byte-interleave**.**

Table 14: DIL Switch SW1

SW No.	ON	OFF (default)
1	PTMC enabled (P13 I/O selected)	PTMC disabled (P14 I/O selected)
2	enable 4-byte-interleave mode	no interleave

5.5 PMC Connector P11

Table 15: PMC Connector P11

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A	4
5	/INT B	/INT C	6
7	/BUSMODE1	+5V	8
9	/INT D	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK	GND	14
15	GND	/GNT	16
17	/REQ	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pins for –12V, Vaux, and V(I/O) are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but is 5V tolerant.

5.6 PMC Connector P12

Table 16: PMC Connector P12

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.

5.7 PMC Connector P13 (PTMC Option H.110)

Table 17: PMC Connector P13

ext. Signal	Pin No.	Pin No.	ext. Signal
CT_D26	1	2	GND
GND	3	4	-
CT_D24	5	6	-
CT_D22	7	8	GND
V(I/O)	9	10	CT_D31
GNDZ11	11	12	CT_D29
CT_D20	13	14	GND
GND	15	16	CT_D27
CT_FRAME_A	17	18	CT_D25
CT_FRAME_B	19	20	GND
V(I/O)	21	22	CT_D23
GNDZ23	23	24	CT_D21
CT_C8_A	25	26	GND
GND	27	28	CT_D19
CT_D18	29	30	CT_D17
CT_D16	31	32	GND
GND	33	34	CT_NETR2
CT_D14	35	36	CT_D30
CT_D12	37	38	GND
/PTEN	39	40	CT_D28
GNDZ41	41	42	CT_NETR1
CT_C8_B	43	44	GND
GND	45	46	CT_D15
CT_D10	47	48	CT_D13
CT_D8	49	50	CT_D11
GND	51	52	CT_D9
CT_D7	53	54	CT_D6
CT_D4	55	56	GND
-	57	58	CT_D5
CT_D2	59	60	CT_D3
CT_D1	61	62	GND
GND	63	64	CT_D1

5.8 PMC Connector P14 (PMC I/O)

Table 18: PMC Connector P14

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
MC	1	I/O	I/O	2	CT_D15
CT_D14	3	I/O	I/O	4	CT_D13
CT_D12	5	I/O	I/O	6	GND
CT_D11	7	I/O	I/O	8	CT_D10
CT_D09	9	I/O	I/O	10	CT_D8
CT_D07	11	I/O	I/O	12	GND
CT_D06	13	I/O	I/O	14	CT_D5
CT_D04	15	I/O	I/O	16	CT_D3
CT_D02	17	I/O	I/O	18	CT_D1
GND	19	I/O	I/O	20	CT_D0
CLKFAIL	21	I/O	I/O	22	/FSYNC
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	/SCLKx2
SL_4	27	I/O	I/O	28	/C16+
SL_2	29	I/O	I/O	30	SL_3
SL_0	31	I/O	I/O	32	SL_1
SPICLK	33	I/O	I/O	34	/SPISEL
SPIMISO	35	I/O	I/O	36	SPIMOSI
/C16-	37	I/O	I/O	38	CT_FRAME_B
CT_FRAME_A	39	I/O	I/O	40	CT_NETREF2
CT_NETREF1	41	I/O	I/O	42	/C4
C2	43	I/O	I/O	44	GND
CT_C8_B	45	I/O	I/O	46	CT_C8_A
CT_D16	47	I/O	I/O	48	CT_D17
CT_D18	49	I/O	I/O	50	CT_D19
GND	51	I/O	I/O	52	CT_D20
CT_D21	53	I/O	I/O	54	CT_D22
CT_D23	55	I/O	I/O	56	CT_D24
GND	57	I/O	I/O	58	CT_D25
CT_D26	59	I/O	I/O	60	CT_D27
CT_D28	61	I/O	I/O	62	CT_D29
CT_D30	63	I/O	I/O	64	CT_D31

The SCbus implemented on the **NPMC-8E1/T1/J1** is a subset of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15.

5.9 The Front Panel Connectors (S1 – S4)

Figure 7: The E1/T1/J1 Connector

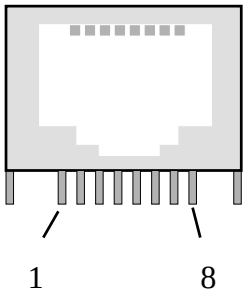


Table 19: Pin Assignment of the E1/T1/J1 connectors

Pin	Signal	
1	TXa+	Output
2	TXa-	Output
3	TXb+	Output
4	RXb+	Input
5	RXb-	Input
6	TXb-	Output
7	RXa+	Input
8	RXa-	Input

TXa/RXa refer to the first line interface on the respective connector.

6 Known Bugs / Restrictions

The PTMC option does not work together with N.A.T.s **NPMC-EXT64** Extender Board, cause up to Revision 1.2 of the **NPMC-EXT64** all P13 and P14 pins, which connect to power in a 64-bit PCI environment are connected directly to the respective power planes.
Hence, do NOT use the **NPMC-8E1/T1/J1** on a **NPMC-EXT64** Extender Board, unless it is configured to PTMC-mode disabled!

Appendix A: Reference Documentation

[1] IDT, Octal T1/E1/J1 Long Haul / Short Haul Transceiver IDT82P2288, 3/2004, Rev. 3
[2] Altera, ACEX 1K Programmable Logic Device Family, May 2003, Ver. 2.4 data sheet
[3] Altera, Cyclone FPGA Family Data Sheet, Oct. 2003, Ver. 1.2
[4] N.A.T., FPGA-TSI Technical Reference Manual, March 2005, Ver. 1.0

Appendix B: Document's History

Revision	Date	Description	Author
1.0	21.11.2005	initial revision	ga
1.1	10.02.2006	'Statement on Environmental Protection' added	ga
1.2	30.06.2006	chapters 6 and 7 added	ga
1.3	11.09.2006	adapted to hardware revision 1.1	te
1.4	16.05.2007	added functionality to enable 4-byte-interleave via SW1	te
1.5	24.05.2007	added timer to trigger irq after time written to register; altered address layout to reduce memory usage	te