NPMC-860-CPU
CPU PMC Module
Technical Reference Manual V1.2

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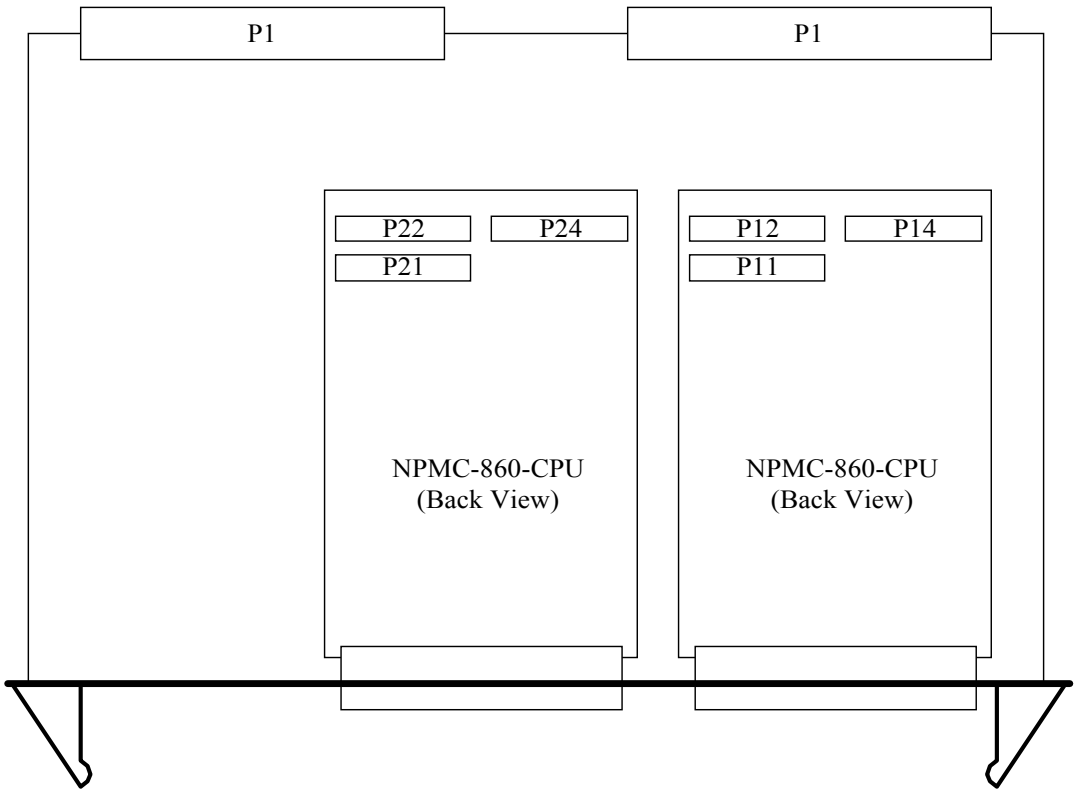
1 Introduction

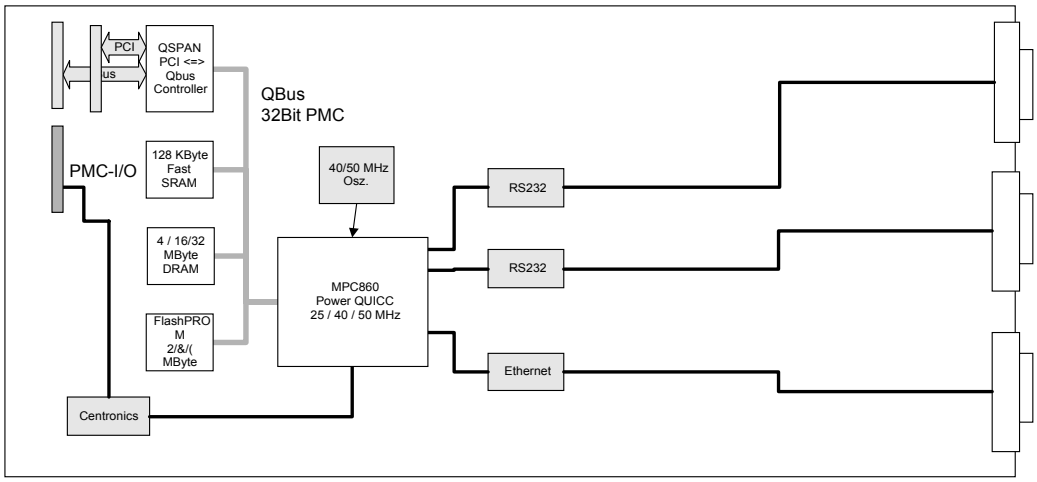
The **NPMC-860-CPU** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

Figure 1: NPMC-860-CPU on a VMEbus carrier



- PowerQUICC MPC860 based Embedded PowerPC Architecture
- Ethernet Port
- RS232 Ports
- Centronics Port
- Single Slot VME solution together with the PMC carrier board

Figure 2: Block Diagram NPMC-860-CPU



Memory

- DRAM: The **NPMC-860-CPU** provides 4, 16 or 32 MByte EDO DRAM on board. The DRAM is 32 Bit wide.

- Flash PROM: The 8Bit boot FlashPROM provides a maximum capacity of 2 Mbyte.

- SRAM: The high speed 32 bit SRAM capacity is 256 Kbyte (max.).

Interfaces

- PCI: The **NPMC-860-CPU** includes a 32 bit 33MHz PCI bus interface.

Ports

- RS232

- Centronics

- Ethernet: AUI

CPU

Depending on the used CPU the PowerQUICC runs with a minimum frequency of 25 Mhz. (40 MHz or 50 Mhz are optional available)

1.1 Overview

Table 1: Technical Overview

Processor	PowerQUICC MPC860 based Emdedded PowerPC Architecture
Main Memory	4, 16 or 32 Mbyte EDO DRAM
PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to QBUS bridge	QSPAN
Centronics	P1284 compatible Parallel Port
serial I/O	RS-232 compatible
Flash PROM	2 Mbyte Flash PROM. On board programmable.
Fast SRAM	(opt.) 128kbyte / 256kbyte fast SRAM
Firmware	pSOS+ BSP, VxWorks BSP (on request)
Power consumption	3.3V 0,5A 5.0V 0,6A
Environm. conditions Temperature (operating) Temperature (storage) Humidity	 0° C to +50 °C -40 °C to +85°C 5 % to 95 % noncondensing
Standards compliance	PCI Rev. 2.1 P1386.1 / Draft 2.0

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NPMC-860-CPU** during its usual lifetime take the following precautions before handling the board.

CAUTION

Malfunction or damage to the board or connected components

Electrostatic discharge and incorrect board swappings can damage circuits or shorten their lifetime.

- Before installing or uninstalling the board read this installation section
- Before installing or uninstalling the **NPMC-860-CPU**, read the Installation Guide and the User´s Manual of the **NPMC-860-CPU** carrier board
- Before installing or uninstalling the **NPMC-860-CPU** on a carrier board or both in a VME rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-860-CPU** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetc radiation ensure that the module
  - is bolted the front panel or VME rack
  - and shielded by closed housing.

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-860-CPU**
- power supply

Power supply

The power supply for the **NPMC-860-CPU** must meet the following specifications:

- required for the module:
  - +3,3V / 0,5 A typical
  - +5,0V / 0,6 A typical

2.2.2 Location Overview

(subject to change)

The figure 1 „Location diagram of the **NPMC-860-CPU**“ highlights the position of the important components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 3: Location diagram of the **NPMC-860-CPU** front panel (schematic)

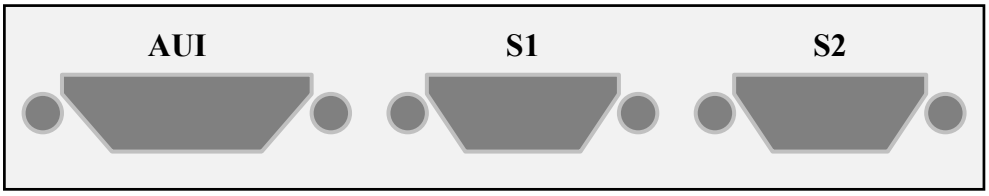
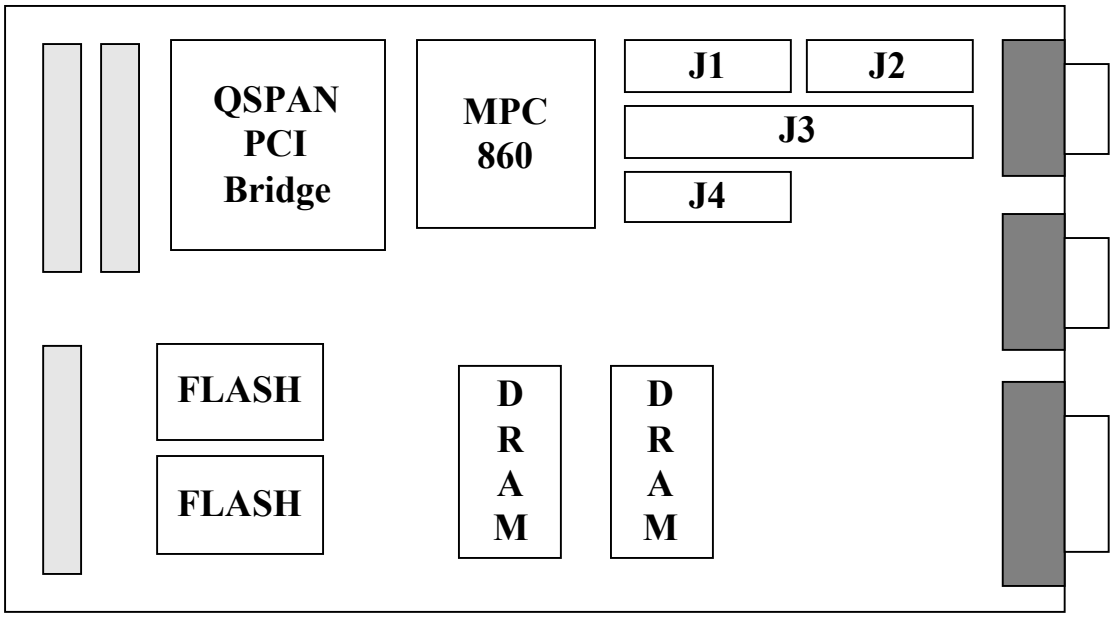
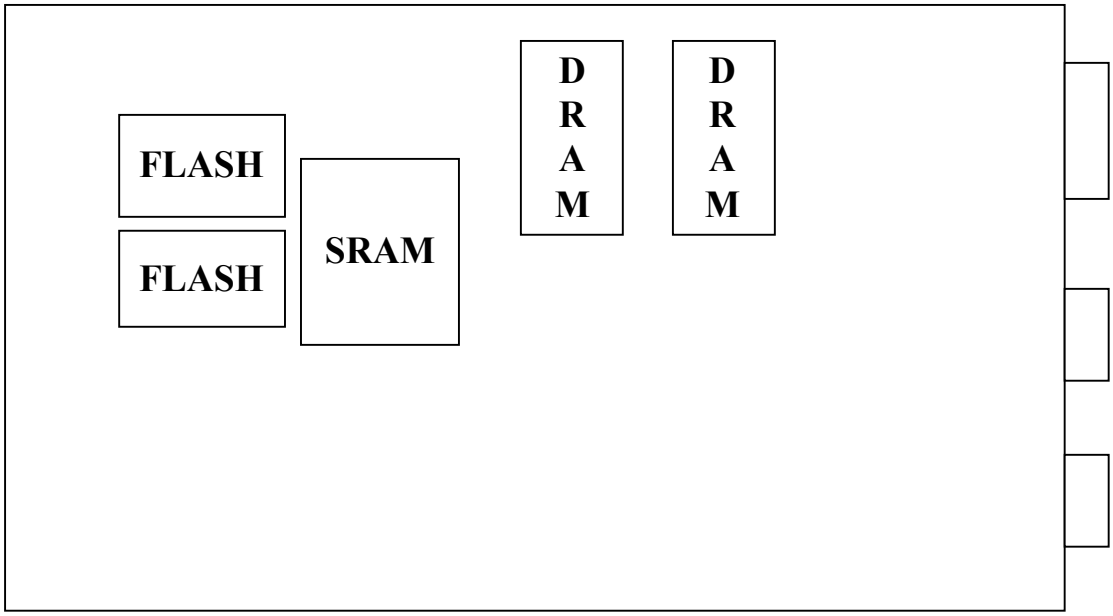


Figure 4: Location diagram of the **NPMC-860-CPU** (schematic)



Top View



Bottom View

2.3 Automatic Power Up

In the following situations the **NPMC-860-CPU** will automatically be reset and proceed with a normal power up. Is the **NPMC-860-CPU** in the reset state, both green LEDs on the frontpanel are turned on and off in a period way.

Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V *
- when +5V voltage level rises above 5,6V *
- when +3.3V voltage level drops below 2,65V *
- when +3.3V voltage level rises above 3,9V *
- or when the carrier board signals a PCI Reset

Watchdog timer

Per factory default the watchdog timer of the PowerQUICC is disabled. If the watchdog timer is enabled, it generates an non-maskable interrupt (NMI) followed by a reset when it is not retriggered by software (see the PowerQUICC users manual).

* PCI Specifications Revision 2.1, Section 4.2.1.1 and Section 4.3.2

2.4 Switch Settings

Currently there is no switch or jumper on the **NPMC-860-CPU**.
All operation options are pre-installed in the factory.

3 Hardware

3.1 Memory Map

3.1.1 NPMC-860-CPU memory map seen from the host CPU (carrier borad)

The following address table carries the default values as they are foreseen from the design.
These addresses may be changed at any time by programming the CS decoder within the SIU of the PowerQuicc processor .
All given addresses are offsets to the PCI bus memory base address of the module.

Table 2: NPMC-860-CPU memory map seen from the host CPU (carrier borad)

Device	Address	Notice
Flash-PROM*	$xx00 0000	2 MByte Flash-Prom (8 Bit wide)
DRAM**	$xx40 0000	4 MByte EDODRAM (32 Bit wide)
Fast SRAM**	$xx20 0000	128/256k Fast SRAM (32 Bit wide)

xx depents on the base address of the module
* only if the PowerQUICC is in the RESET state
** only if the Power QUICC is in the RUN state

3.1.2 NPMC-860-CPU Memory Map Seen from the Power QUICC CPU

All addresses are setup by programming the corresponding Chip-Select Decoder of the PowerQUICC. The given addresses represent only one possible configuration:

Table 3: NPMC-860-CPU Memory Map Seen from the Power QUICC CPU

Device	CS Line	Default Address	Function	Notes
Flash-PPROM*	CS0	$0000 0000		2 Mbyte Flash-Prom (8 Bit wide)
Fast SRAM**	CS2	$0020 0000		128/256k Fast SRAM (32 Bit wide)
DRAM**	CS1	$0040 0000		4 Mbyte EDO DRAM (32 Bit wide)
RESETIO	CS5	$0130 0600	Reset IO-Chip´s write only	not available
CSPMC	CS3	>$1000 0000	CS for PCI / PMCbus access	there are two PCI images available selectet by the IMS-Signal. This Signal is generated by the Port D Bit PD15
CSQSPAN	CS4	$0200 0000	Qbus access to the QSPAN Registers	

3.2 PowerQUICC CPU

3.2.1 Introduction

The MPC860 PowerPC™ Quad Integrated Communications Controller (PowerQUICC) is a versatile one-chip integrated microporocessor and peripheral controller combination that can be used in a variety of applications. It particularly excels in both communications and networking systems.

The MPC860 is a PowerPC-based derivative of Motorola´s MC68360 (Quad Integrated Communications Controller(QUICC™). The CPU on the MPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) of the MC68360 QUICC has been enhanced with the addition of the interprocessor-integrated-controller (I^2C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs). Overall systems functionality is completed with the addition of a PCMCIA socket controller supporting up to two sockets and a real time clock.

3.3 QSpan™ Bus Bridge

3.3.1 Introduction

The QSpan™ chip is a member of Tundra Semiconductor Corporation´s family of PCI bus-bridging devices enabling board designers to bring PCI-based embedded products to market faster and for less cost.
The QSpan™ is designed to gluelessly bridge the QUICC™ (MC68360), the PowerQUICC™ as well as the MPC801 embedded controllers to PCI.

3.3.2 Features

The QSpan™ has the following features:

- A direct connect interface to the PCI bus for Motorola´s QUICC (MC68360), PowerQUICC(MPC860), M68040, the PMC821 and the MPC861 embedded controllers;
- 32-bit PCI interface compliant wih PCI Revision 2.1;
- Decoupled transfer technology: three 16-entry deep FIFOs buffer multiple transaction in both directions, allowing zero wait state bursting on the PCI and Motorola buses;
- IDMA peripheral support for QUICC and PowerQUICC;
- Flexible address space mapping and translation between the PCI and Motorola buses;
- Programmable endian byte ordering;
- Two user-programmable slave images available for PCI access to the Motorola buses;
- QSpan™ control and status registers accessible from both PCI and Motorola buses;
- PCI bus and Motorola buses can be operated at different clock frequencies;

3.3.3 Host Setup of the QSpan PCI Bridge

In order to configure the **NPMC-860-CPU** to work on the PCI-bus, the following steps must be taken:

1. Look up the address of the PCI-bus controller of the **NPMC-860-CPU** in the ***Configuration Space*** of the PCI-bus of the carrier board (please refer to the manual for the carrier board).
The PCI-bus controller of the **NPMC-860-CPU** occupies 256 Bytes in the ***Configuration Space*** and you should see the following address map (first 64 bytes according to PCI specification 2.1):

Table 4: NPMC-860-CPU memory map in the configuration space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address configuration space
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
...	...	...
0x003c	PCI_MISC1	miscellaneous 1

For more details regarding the QSpan registers of the **NPMC-860-CPU**, please refer to the QSpan manual's register map (table A.1, Appp. A-2).

2. Now write - to the offset address 0x0010 (QSpan register PCI_BSM, 32 bit) - the start address of the **NPMC-860-CPU** where it should appear in the ***memory space*** of the carrier board's PCI-bus. Please note, that all PCI register accesses have to be done in little endian format.
The register image of the QSpan should now be visible in the PCI memory space.

Table 5: NPMC-860-CPU memory map in the PCI memory space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address QSpan register
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	Class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
0x0014	-	QSpan unimplemented
...	...	...
0x003c	PCI_MISC1	miscellaneous 1
...	...	...
0x800	MISC_CTL	miscellaneous control
0x804	EEPROM_CS	EEPROM control
...	...	...
0x0ffc	-	QSpan reserved

3. Initialize the register PBTI0_CTL for target image 0 and set the necessary parameters:
The longword read/write access must be enabled by writing the PBTI0_CTL at offset 0x0100 (image enable, block size BS[3:0] = 0110 = 4 MB, or BS[3:0] = 1000 = 16 MB, Q-bus destination port size DSIZE[1:0] = 00 = 32 bit).

4. Set address translation decoding on register PBTI0_ADD at offset 0x0104 (host system dependent):
Write the start address where the memory of the NPMC-860-CPU module should appear in the ***Memory Space*** of the PCI bus.

5. Make certain that there are no address conflicts in your systems (set/check the amount of the memory occupied by the **NPMC-860-CPU** in the PCI memory space).

3.3.4 Q-Bus Configuration

Through the MISC_CTL register parameters for configurating the local bus (Q-Bus) are set. The settings to be performed are system dependant. But, the following aspect has to be taken into account in any case:

Setting of bit 0 (SW-RST) will cause a RESET on the Q-Bus, if the Q-BUS HRESET signal is connected to the RESETO pin of the QSPAN (like for this module). The RESETO signal follows the programming of the SW-RST bit directly, i.e. without any delay in time. Therefore, if the MPC860 is to be reset by this means, the minimum time period necessary to perform an orderly hardware reset of the MPC860 has to be strictly obeyed. Otherwise the MPC860 may enter an undefined state. A time period of 100ms is recommended between the setting and resetting of this bit. In time-critical applications this period may be reduced. Any value longer than 1ms should be suuficient. 100ms is a period of time which is suitable and safe for resetting the Q-Bus in all cases and for all CPU operating frequencies.

3.3.5 EEPROM Configuration

By means of register EEPROM_CS the Configuration-EEPROM may be read and reprogrammed, which the QSPAN uses for Power-Up – initialialisation. Please be aware of the fact that programming the EEPROM with unsuitable values may cause the PCI-Bus to hang completely.

NOTE: For more information, please refer to the QSpan manual. Please make certain that you use the correct endian format when writing into the QSpan registers.

3.4 DRAM

The **NPMC-860-CPU** provides an on-board DRAM (EDO-DRAM). This memory is accessible from the PowerQUICC or the QSPAN PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the DRAM. This fexible memory controller allows the implementation of memory systems with very specific timing requirements.

The user is allowed to define different timing patters for the control signals that govern a memory device. This patterns define how the external control signals behave in a read-access request, write-access request, burst read-access request, or burst write-access request. The user defines how the external control signals toggle when the periodic timers reach the maximum programmed value for refresh operation.

The memory capacity is 4 MByte (optinally 16 or 32MByte), the memory is 32 bit wide. The access time of the EDO DRAM is 60 nsec for new accesses, the access time within a row is 30 nsec (bursting)

For different operating frequence of the MPC860 the user need to define different timing patters.

The User Programmable Machine A (UPM A) controls the PowerQUICC and the PCI accesses to the DRAM memory.

In the PowerQUICC Reset-state accesses to the DRAM will be inhibited.
Parity generation and check will not supported by the module.

3.5 SRAM

The **NPMC-860-CPU** provides optionally an on board high speed SRAM. This memory is accessible from the PowerQUICC or the QSPAN PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the SRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements

The memory capacity is 128 kbyte (optionally 256kbyte), the memory is 32 bit wide. The access time of the SRAM is 10 nsec for every access type.

There is no restriction on accessing the SRAM.

3.6 Boot Flash

The flash memory area is located on the PowerQUICC bus so that the reset vector table in the boot flash is visible to the CPU after power on reset. The boot flash memory has a maximum size of 2 MByte and can directly be accessed by the CPU. The flash memory area is 8-bit wide organized.

The flash memory is a 5V only device. For programming the Flash is no extra programming voltage necessary.
Programming the flash memory is possibile in two ways:

- Programming the entire flash memory from the PCI-bus. The module must be in the RESET-State.
- Programming the flash memory in the run state of the PowerQUICC.

3.7 Interrupt Structure

The NPMC-Module has the following Interrupt structure:

Table 6: Interrupt Structure

Interrupt source	**PowerQUICC Interrupt level**
Abort	IRQ-Level 0 (highest level)
NC	IRQ-Level 1
NC	IRQ-Level 2
QSPAN	IRQ-Level 3
NC	IRQ-Level 4
NC	IRQ-Level 5
NC	IRQ-Level 6
NC	IRQ-Level 7 (lower level)

4 Conncetors

4.1 Serial I/O, BDM

The two RS232 serial I/O ports are available via a 20 pin SMD micro connector together with the JTAG / development Port / BDM Port.

The two RS232 ports are realised with the PowerQUICC serial communication controller SCC1 and SCC2. If the SCC1 or SCC2 are used for other application. The serial Line can optionally driven by the SMCs.

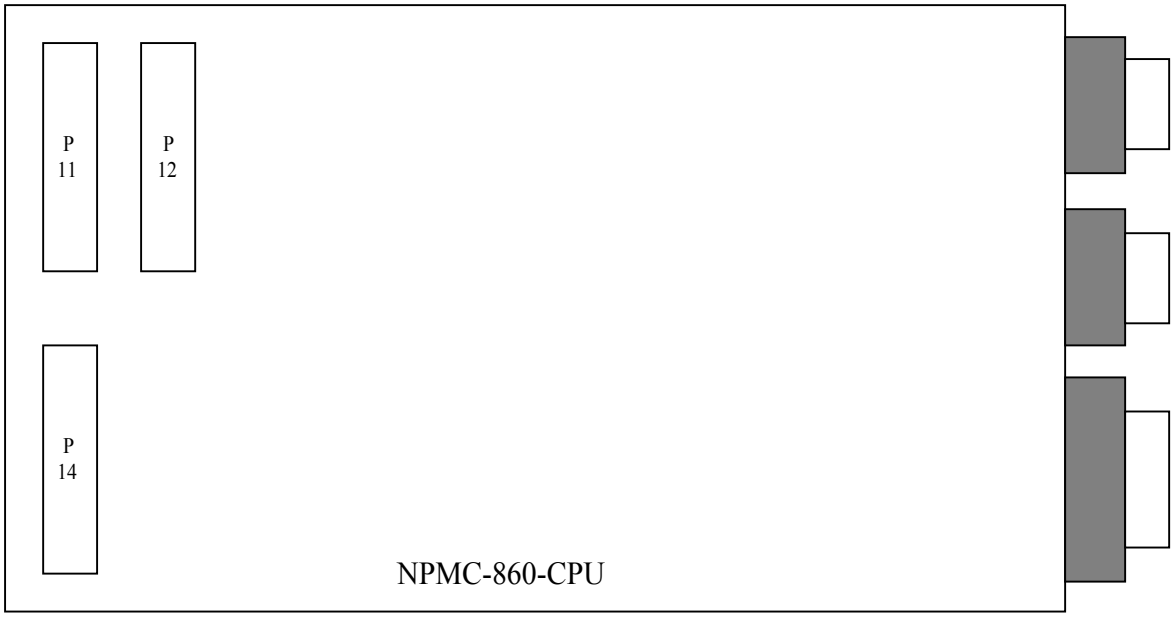
To select the JTAG mode of the PowerQUICC pin 15 of the connector must held low during power up, otherwise development port or background debug mode port is enable.

Table 7: Development Port / BDM and IEEE 1149.1 Connector Pin-out Options (J4)

JTAG	Development Port	BDM Port	PIN					
VFLS0	VFLS0	VFLS0	1		2	/SRESET	/SRESET	/SRESET
GND	GND	GND	3		4	DSCK	DSCK	TCK
GND	GND	GND	5		6	VFLS1	VFLS1	VFLS1
/HRESET	/HRESET	/HRESET	7		8	DSDI	DSDI	TDI
+5V	+5V	+5V	9		10	DSDO	DSDO	TDO
/ABORT	/ABORT	/ABORT	11		12	--------	--------	TMS
--------	--------	FRZ	13		14	+3.3V	+3.3V	+3.3V
/JT/DBG	/JT/DBG	/JT/DBG	15		16	GND	GND	GND
TXD1	TXD1	TXD1	17		18	TXD2	TXD2	TXD2
RXD1	RXD1	RXD1	19		20	RXD2	RXD2	RXD2

4.2 PMC Connector

Figure 5: PMC Conncetor



4.2.1 PMC Connector P11

Table 8: P11 Pin Assignment

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	TCK	-12V	2	n.c.
GND	3	GND	/INT A	4	/IRQ-QSPAN
n.c.	5	/INT B	/INT C	6	n.c.
n.c.	7	bus mode 1	+5V	8	+5V
n.c.	9	/INT D	PCI_RSV1	10	n.c.
GND	11	GND	PCI_RSV2	12	n.c.
CLK	13	CLK	GND	14	n.c.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
n.c.	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
n.c.	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	n.c.
n.c.	41	/SDONE	/SB0	42	n.c.
PAR	43	PAR	GND	44	GND
n.c.	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
n.c.	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	n.c.

4.2.2 PMC Connector P12

Table 9: PMC Connector P12 Pin Assignment

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
n.c.	1	+12V	/TRST	2	n.c.
n.c.	3	TMS	TDO	4	n.c.
n.c.	5	TDI	GND	6	GND
GND	7	GND	PCI_RSV3	8	n.c.
n.c.	9	PCI_RSV	PCI_RSV4	10	n.c.
n.c.	11	BUS-MODE 2	+3.3V	12	+3.3V
/RST	13	/RTS	BUS-MODE 3	14	n.c.
+3.3V	15	+3.3V	BUS-MODE 4	16	n.c.
n.c.	17	PCI_RSV	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESVD	34	n.c.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	n.c.
+3.3V	53	+3.3V	PCI_RESV	54	n.c.
n.c.	55	PCI_RESV	GND	56	GND
n.c.	57	PCI_RESV	PCI_RESV	58	n.c.
GND	59	GND	PCI_RESV	60	n.c.
n.c.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	n.c.

4.2.3 Pin Assignment of the PMC Connector P14 (PMC I/O)

Table 10: Pin Assignment of the PMC Connector - P14, Version I

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
NC	1	I/O	I/O	2	NC
NC	3	I/O	I/O	4	NC
NC	5	I/O	I/O	6	NC
NC	7	I/O	I/O	8	NC
NC	9	I/O	I/O	10	NC
NC	11	I/O	I/O	12	NC
NC	13	I/O	I/O	14	NC
NC	15	I/O	I/O	16	NC
NC	17	I/O	I/O	18	NC
NC	19	I/O	I/O	20	NC
NC	21	I/O	I/O	22	NC
NC	23	I/O	I/O	24	NC
NC	25	I/O	I/O	26	NC
NC	27	I/O	I/O	28	NC
NC	29	I/O	I/O	30	NC
NC	31	I/O	I/O	32	NC
CENT_STROBE	33	I/O	I/O	34	NC
CENT D0	35	I/O	I/O	36	CENT_ERROR
CENT D1	37	I/O	I/O	38	NC
CENT D2	39	I/O	I/O	40	NC
CENT D3	41	I/O	I/O	42	GND
CENT D4	43	I/O	I/O	44	GND
CENT D5	45	I/O	I/O	46	GND
CENT D6	47	I/O	I/O	48	GND
CENT D7	49	I/O	I/O	50	GND
CENT_ACK	51	I/O	I/O	52	GND
CENT_BUSY	53	I/O	I/O	54	GND
CENT_PE	55	I/O	I/O	56	GND
CENT_SEL	57	I/O	I/O	58	I2CSDA
I2CSLC	59	I/O	I/O	60	GND
SMC_TX1	61	I/O	I/O	62	SMC_RX1
SMC_TX2	63	I/O	I/O	64	SMC_RX2

In this version an SMC port is available on the PMC I/O (pins 61 - 64).
The SMC (pin 61 - 64) is not available when Centronics is used.

Table 11: Pin Assignment of the PMC Connector - P14, Version II

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
NC	1	I/O	I/O	2	NC
NC	3	I/O	I/O	4	NC
NC	5	I/O	I/O	6	NC
NC	7	I/O	I/O	8	NC
NC	9	I/O	I/O	10	NC
NC	11	I/O	I/O	12	NC
NC	13	I/O	I/O	14	NC
NC	15	I/O	I/O	16	NC
NC	17	I/O	I/O	18	NC
NC	19	I/O	I/O	20	NC
NC	21	I/O	I/O	22	NC
NC	23	I/O	I/O	24	NC
NC	25	I/O	I/O	26	NC
NC	27	I/O	I/O	28	NC
NC	29	I/O	I/O	30	NC
NC	31	I/O	I/O	32	NC
CENT_STROBE	33	I/O	I/O	34	NC
CENT D0	35	I/O	I/O	36	CENT_ERROR
CENT D1	37	I/O	I/O	38	NC
CENT D2	39	I/O	I/O	40	NC
CENT D3	41	I/O	I/O	42	GND
CENT D4	43	I/O	I/O	44	GND
CENT D5	45	I/O	I/O	46	GND
CENT D6	47	I/O	I/O	48	GND
CENT D7	49	I/O	I/O	50	GND
CENT_ACK	51	I/O	I/O	52	GND
CENT_BUSY	53	I/O	I/O	54	GND
CENT_PE	55	I/O	I/O	56	GND
CENT_SEL	57	I/O	I/O	58	I2CSDA
I2CSLC	59	I/O	I/O	60	GND
PMC IRQ 1	61	I/O	I/O	62	PMC IRQ 3
PMC IRQ 2	63	I/O	I/O	64	NC

Instead of the SMC port in version I, three interrupt lines to interrupt the MPC860 on the NPMC-860-CPU are available.

Table 12: Description P14 Signals

Signal	DescriptionGeneral
CENT_STROBE	Centronics Strobe Signal
CENT D0	Centronics D0 Line
CENT D1	Centronics D1 Line
CENT D2	Centronics D2 Line
CENT D3	Centronics D3 Line
CENT D4	Centronics D4 Line
CENT D5	Centronics D5 Line
CENT D6	Centronics D6 Line
CENT D7	Centronics D7 Line
CENT_ACK	Centronics Acknowledge
CENT_BUSY	Centronics Busy Signal
CENT_PE	Centronics Paper Error
CENT_SEL	Centronics Select Signal
CENT_ERROR	Centronics Error Signal
GND	Ground
NC	Not Connected
I2CSCL	I2C Clock
I2CSDA	I2C Data Line
SMC_TX1	SMC 1 Transmit Line
SMC_TX2	SMC 2 Transmit Line*
SMC_RX1	SMC 1 Receive Line
SMC_RX2	SMC 2 Receive Line*
PMC IRQ	Hardware Interrupt Line for MPC860

The SMC is not available when Centronics is used.

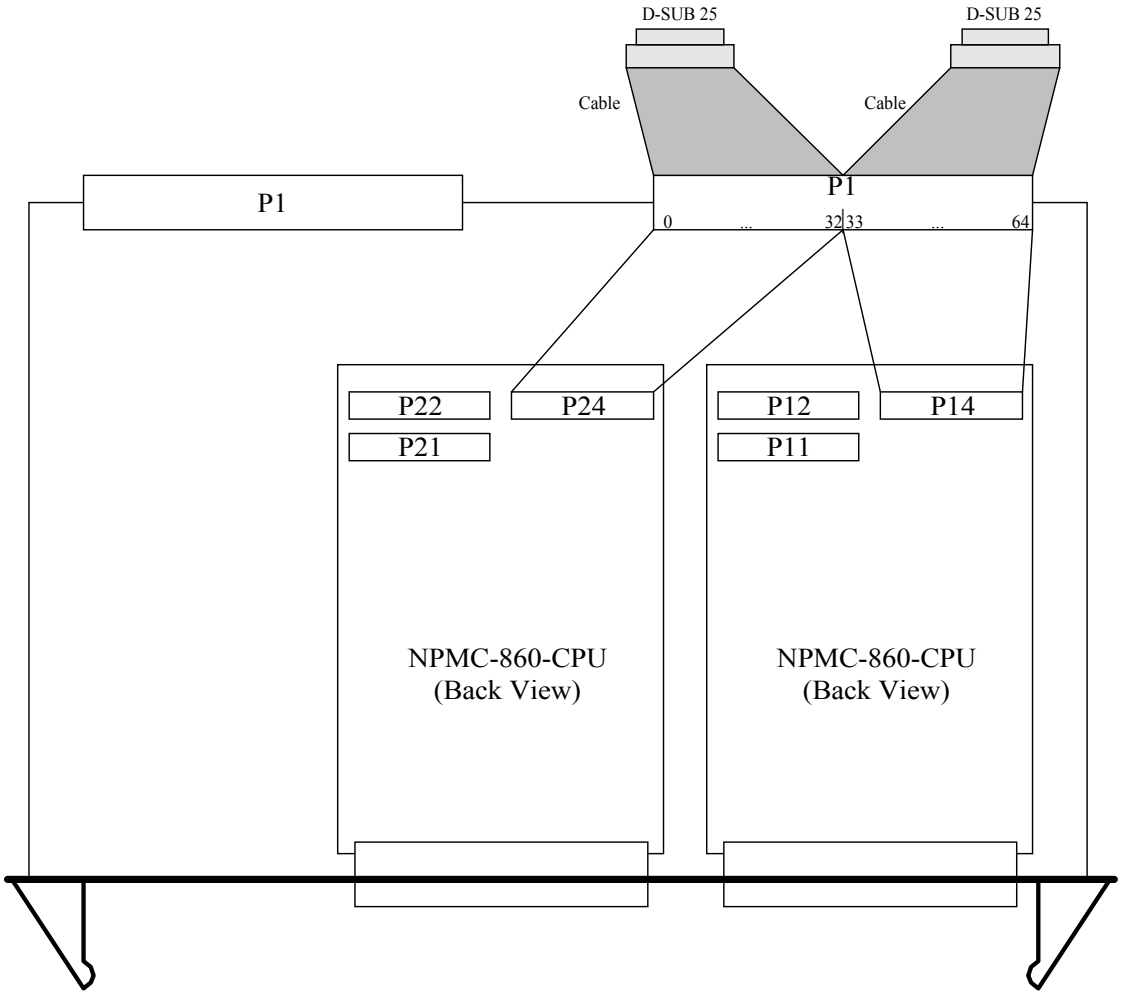
4.2.4 NPMC-860-CPU P14 Specials

Following Ports are available on the P14, respectively on the P2 connector of the carrier board:

- Centronics
- I2C
- SMC channel of MPC860
- SMC channel of MPC860

The Centronics signals are placed to the signal comes out of the P2 connector of the carrier board as a standard D-Sub 25:

Figure 6: NPMC-860-CPU Connectors and PMC I/O



4.3 Front Panel Connectors

4.3.1 RS232

The two 9 pin micro Sub-D (S1 and S2) connector carry the AUI Ethernet signals.

Table 13: Pin Assignment RS232 Connectors

Pin	Signal	Meaning
1	N.C.	Not Connected
2	RxD	Read Data
3	TxD	Write Data
4	N.C.	Not Connected
5	GND	Ground
6	N.C.	Not Connected
7	/RTS	Request to Send
8	/CTS	Clear to Send
9	N.C.	Not Connected

4.3.2 Ethernet/AUI

The 15 pin micro Sub-D connector carries the AUI Ethernet signals.

Table 14: Pin Assignment AUI Connector

Pin	Signal	Meaning
1	GND/Shield	Ground or Shield connection
2	CLSN+	Collision (+)
3	TR+	Send (+)
4	GND/Shield*	Ground or Shield connection
5	Rec+	Receive (+)
6	GND	Ground
7	N.C.	Not Connected
8	GND/Shield*	Ground or Shield connection
9	CLSN-	Collision (-)
10	TR+	Transmit (-)
11	GND/Shield*	Ground or Shield connection
12	Rec-	Receive (-)
13	12V	12 Volt for AUI
14	GND/Shield*	Ground or Shield connection
15	N.C.	Not Connected

In case R31 (resistor) is installed on the NPMC-860-CPU then the * pins (1, 4, 8, 11 and 14) are connected to Ground.

In case R32 (resistor) is installed on the NPMC-860-CPU then the * pins (1, 4, 8, 11 and 14) are connected to the shield.

4.4 On-board Connectors

The on-board connectors J1, J2 and J3 have the followig meaning:

- J1 additional serial I/O port
- J2 additional serial I/O port
- J3 UTOPIA (when MPC860-SAR is used)

Please contact N.A.T. for details in case you want to use these connectors.

4.4.1 RS232

The two 9 pin micro Sub-D (S1 and S2) connector carry the AUI Ethernet signals.

5 Boot Software

See VxWorks manual.

6 Documentation reference

6.1 PCI Interface chip

Company: TUNDRA
Title: QSPAN (CA91CC860)
PCI to Motorola Processor Bridge Manual

6.2 MPC860 PowerQUICC

Company: Motorola Inc.
Title: MPC860 PowerQUICC
User´s Manual

7 Document's History

Version	Date	Description	Author
1.0	1997	Initial version	ghb
1.1	26.07.1999	Layout improvements	as
	03.01.2001	Correction of 3.1.1 (QSpan)	as
1.2	22.06.2001	QSPAN programming description extended	ga