cPCI-PCI Adapter

Reference Manual

Version 1.0

The cPCI-PCI Adapter has been designed by:

N.A.T. GmbH
Kamillenweg 22
D-53757 Sankt Augustin
Phone: ++49/2241/3989-0
Fax: ++49/2241/3989-10

E-Mail: sales@nateurope.com
Internet: http://www.nateurope.com

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1 Introduction

The cPCI-PCI Adapter is a passive PCI to cPCI adapter board intended for use with cPCI boards for testing and debug purposes. It eases debugging of cPCI boards by enabling the user to access the module under test from both sides, while being able to do software development and debug in a standard PC environment.

2 Technical Specifications

2.1 Bus Interface

- PCI bus 64 bit, 33/66 MHz supported
- H.110 implementation on J4, routed to standard SCSA connector for flat cable access

2.2 Power Supply

The cPCI-PCI Adapter draws very little power from the carrier supplies. Current drawn from +3.3V, +5V, +12V, -12V, V(I/O) is less than 10mA each.
+3.3V, +5V, V(I/O), and GND are connected to separate power planes.

V(I/O) may be taken from the PC's V(I/O), +3.3V, or +5V depending on the PCI bus signalling requirements. This setting is made by closing a solder bridge connection to the desired I/O voltage. For use in older motherboards, which do not supply +3.3V to the PCI connectors, a +5V --> +3.3V voltage regulator circuitry is implemented, which may be fed to the cPCI board by closing a solder bridge.

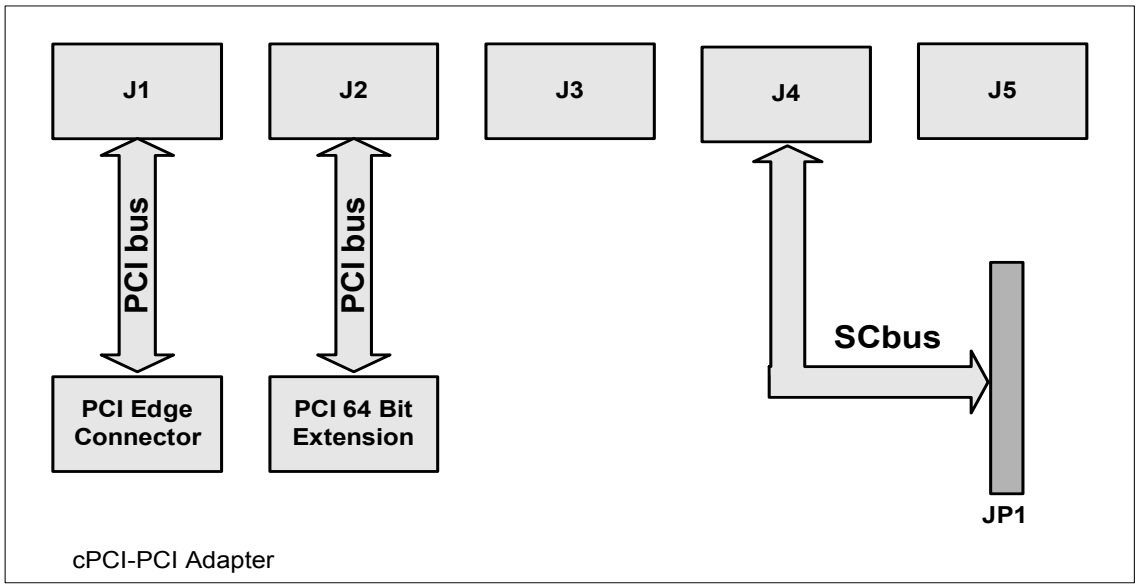
2.3 Environment

Temperature:	-40 – +85°C	operating and storage
Humidity:	5 – 90% rh	not condensing

3 Hardware Description

This chapter contains a brief description of the cPCI-PCI Adapter extender board.

Figure 1: Wiring Diagram

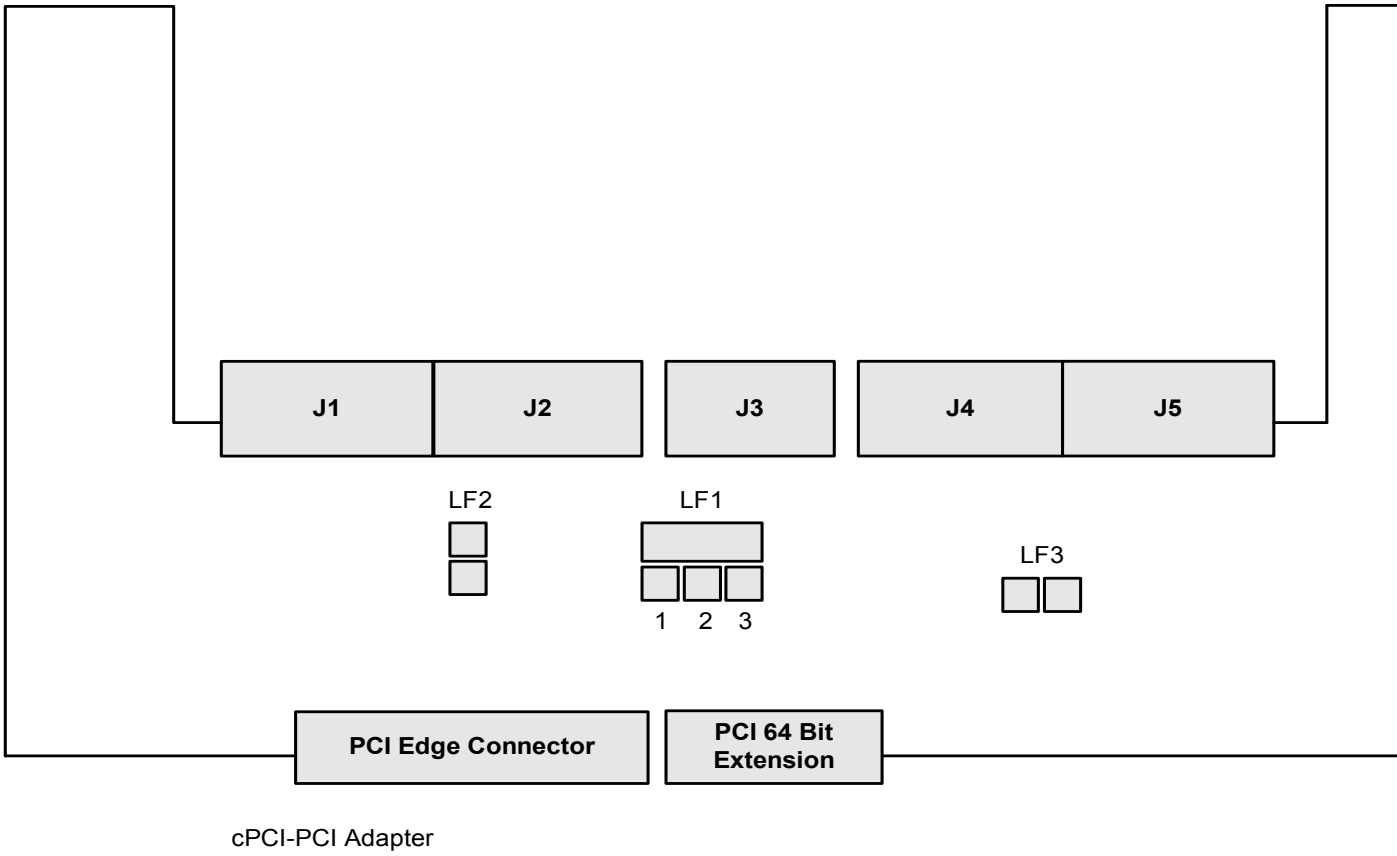


3.1 Hardware Overview

The cPCI-PCI Adapter is a passive extender board, i.e. it does not contain any circuitry apart from 2 PCI connector sets (PCI edge connectors plugging into the motherboard, J1 – J5 for acceptance of the cPCI board under test).

The SCbus subgroup of H.110 signals on connector J4 is routed to a 26-pin male header with the standard SCbus pin assignment for flat cable attachment in PCs. ies the signals, the other is grounded. The male headers assembled fit directly into the probes of e.g. a Tectronix TLA logic analyzer series.

Figure 2: Position of Connectors and Solderfields

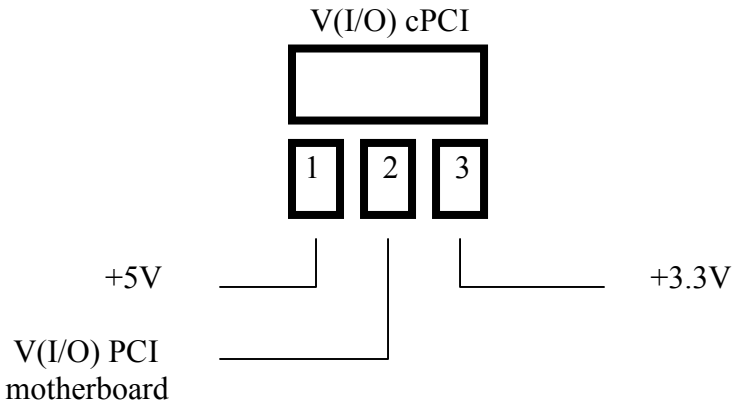


3.2 Solder Fields

There are 3 solder fields on the cPCI-PCI Adapter; one for the selection of the I/O voltage V(I/O), the other two for the selection of the source of the +3.3V cPCI supply voltage. They are described below:

3.2.1 Solder Field LF1

This solder field lets the user select between different voltage sources for V(I/O). The solder field looks like this:



By means of this solder field the signalling voltage can be selected for motherboards that don't supply V(I/O), or for cPCI boards that need a different I/O voltage from what the motherboard supplies.

Care with this feauture is highly recommended, as not all PCI devices are 5V-tolerant!
By default, V(I/O) PCI motherboard is connected to V(I/O) cPCI.

3.2.2 Solder Fields LF2 and LF3

Solder fields LF2 and LF3 must never be closed at the same time, as they supply the +3.3V to the cPCI board. They were introduced, as many older PC motherboards do not supply +3.3V to the PCI slots. For this case LF3 has to be closed, while LF2 is open. Then, the +3.3V will be supplied to the cPCI board by a regulator generating it from the +5V supply, which is always present.

By default, LF2 will be closed, leaving LF3 open, thus connecting the motherboard PCI +3.3V supply to the cPCI +3.3V.

4 Connectors

4.1 PCI Motherboard Edge Connector

Table 1: PCI Motherboard Edge Connector

Pin No.	PCI-Signal Side B	PCI-Signal Side A	Pin No.	PCI-Signal Side B	PCI-Signal Side A
1	-12V	TRST#*	32	AD17	AD16
2	TCK**	+12V	33	C/BE2#	+3.3V
3	GND	TMS*	34	GND	FRAME#
4	TDO	TDI	35	IRDY#	GND
5	+5V	+5V	36	+3.3V	TRDY#
6	+5V	INTA#	37	DEVSEL#	GND
7	INTB#	INTC#	38	GND	STOP#
8	INTD#	+5V	39	LOCK#*	+3.3V
9	PRSNT1#**	nc	40	PERR#	SDONE**
10	nc	V(I/O)*	41	+3.3V	SBO#**
11	PRSNT2#***	nc	42	SERR#	GND
12	Keyway	Keyway	43	+3.3V	PAR
13	Keyway	Keyway	44	C/BE1#	AD15
14	nc	nc	45	AD14	+3.3V
15	GND	RST#	46	GND	AD13
16	CLK	V(I/O)*	47	AD12	AD11
17	GND	GNT#	48	AD10	GND
18	REQ#	GND	49	M66EN	AD9
19	V(I/O)*	nc	50	Keyway	Keyway
20	AD31	AD30	51	Keyway	Keyway
21	AD29	+3.3V	52	AD8	C/BE0#
22	GND	AD28	53	AD7	+3.3V
23	AD27	AD26	54	+3.3V	AD6
24	AD25	GND	55	AD5	AD4
25	+3,3V	AD24	56	AD3	GND
26	C/BE3#	IDSEL	57	GND	AD2
27	AD23	+3.3V	58	AD1	AD0
28	GND	AD22	59	V(I/O)*	V(I/O)*
29	AD21	AD20	60	ACK64#	REQ64#
30	AD19	GND	61	+5V	+5V
31	+3.3V	AD18	62	+5V	+5V

Table 2: PCI Motherboard Edge Connector, 64 Bit Extension

Pin No.	PCI-Signal Side B	PCI-Signal Side A	Pin No.	PCI-Signal Side B	PCI-Signal Side A
63	nc	GND	79	V(I/O)*	AD48
64	GND	C/BE7#	80	AD47	AD46
65	C/BE6#	C/BE5#	81	AD45	GND
66	C/BE4#	V(I/O)*	82	GND	AD44
67	GND	PAR64	83	AD43	Ad42
68	AD63	AD62	84	AD41	V(I/O)*
69	AD61	GND	85	GND	AD40
70	+5V	AD60	86	AD39	AD38
71	AD59	AD58	87	AD37	GND
72	AD57	GND	88	V(I/O)*	AD36
73	GND	AD56	89	AD35	AD34
74	AD55	AD54	90	AD33	GND
75	AD53	V(I/O)*	91	GND	AD32
76	GND	AD52	92	nc	nc
77	AD51	AD50	93	nc	GND
78	AD49	GND	94	GND	nc

* V(I/O) of the PC motherboard PCI edge connectors is not wired directly to V(I/O) of the cPCI connectors Jx. cPCI V(I/O) can be connected via a solder bridge either to V(I/O) PCI (default setting), or to +5V, or to +3.3V.

** signal is not connected

*** PRSNT2# is connected to GND to signal board insertion

4.2 Compact PCI Backplane Connector J1

Table 3: Compact PCI Backplane Connector J1 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	+5V	-12V	/TRST*
2	TCK*	+5V	TMS*
3	/INTA	/INTB	/INTC
4	nc	/HEALTHY*	V(I/O)
5	nc	nc	/RST
6	/REQ	GND	+3.3V
7	AD30	AD29	AD28
8	AD26	GND	V(I/O)
9	/C/BE3	IDSEL	AD23
10	AD21	GND	+3.3V
11	AD18	AD17	AD16
12	Key Area		
13			
14			
15	+3.3V	/FRAME	/IRDY
16	/DEVSEL	PCIXCAP**	V(I/O)
17	+3.3V	nc	nc
18	/SERR	GND	3.3V
19	+3.3V	AD15	AD14
20	AD12	GND	V(I/O)
21	+3.3V	AD9	AD8
22	AD7	GND	3.3V
23	+3.3V	AD4	AD3
24	AD1	+5V	V(I/O)
25	+5V	/REQ64	/ENUM*

Table 4: Compact PCI Backplane Connector J1 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	+12V	+5V	GND
2	nc	TDI*	GND
3	+5V	/INTD	GND
4	INTP**	INTS**	GND
5	GND	/GNT	GND
6	CLK	AD31	GND
7	GND	AD27	GND
8	AD25	AD24	GND
9	GND	AD22	GND
10	AD20	AD19	GND
11	GND	/C/BE2	GND
12	Key Area		
13			
14			
15	/BD_SEL**	/TRDY	GND
16	/STOP	/LOCK	GND
17	GND	/PERR	GND
18	PAR	/C/BE1	GND
19	GND	AD13	GND
20	AD11	AD10	GND
21	M66EN	/C/BE0	GND
22	AD6	AD5	GND
23	+5V	AD2	GND
24	AD0	/ACK64	GND
25	+3.3V	+5V	GND

* signal is not connected
** signal pulled low

4.3 Compact PCI Backplane Connector J2

Table 5: Compact PCI Backplane Connector J2 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	nc	GND	nc
2	nc	nc	/SYSEN**
3	nc	GND	nc
4	V(I/O)	nc	/C/BE7
5	/C/BE5	GND	V(I/O)
6	AD63	AD62	AD61
7	AD59	GND	V(I/O)
8	AD56	AD55	AD54
9	AD52	GND	V(I/O)
10	AD49	AD48	AD47
11	AD45	GND	V(I/O)
12	AD42	AD41	AD40
13	AD38	GND	V(I/O)
14	AD35	AD34	AD33
15	nc	GND	/FAL**
16	nc	nc	/DEG**
17	nc	GND	/PRST**
18	nc	GND	nc
19	GND	GND	nc
20	nc	GND	nc
21	nc	GND	nc
22	GA4*	GA3*	GA2*

* signal is not connected
** signal pulled low

Table 6: Compact PCI Backplane Connector J2 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	nc	nc	GND
2	nc	nc	GND
3	nc	nc	GND
4	GND	/C/BE6	GND
5	/C/BE4	PAR64	GND
6	GND	AD60	GND
7	AD58	AD57	GND
8	GND	AD53	GND
9	AD51	AD50	GND
10	GND	AD46	GND
11	AD44	AD43	GND
12	GND	AD39	GND
13	AD37	AD36	GND
14	GND	AD32	GND
15	nc	nc	GND
16	GND	nc	GND
17	nc	nc	GND
18	GND	nc	GND
19	nc	nc	GND
20	GND	nc	GND
21	nc	nc	GND
22	GA1*	GA0*	GND

* signal is not connected

4.4 Compact PCI Backplane Connector J4

Compact PCI backplane connector J4 carries the H.110 bus signals.

Table 7: Compact PCI Backplane Connector J4 Rows A – C

Pin No.	Row A Signal	Row B Signal	Row C Signal
1	CT_D0	nc	CT_D1
2	CT_D4	CT_D5	CT_D6
3	CT_D8	CT_D9	CT_D10
4	CT_D11	nc	CT_D12
5	nc	CT_D14	CT_D15
6	nc	nc	nc
7	nc	nc	nc
8	nc	nc	nc
9	nc	nc	nc
10	nc	nc	nc
11	nc	nc	nc
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	nc
22	nc	nc	nc
23	nc	nc	/CT_EN*
24	nc	nc	nc
25	nc	nc	nc

* signal is connected to GND

Table 8: Compact PCI Backplane Connector J4 D – F

Pin No.	Row D Signal	Row E Signal	Row F Signal
1	CT_D2	CT_D3	nc
2	CT_D7	nc	nc
3	nc	SCLKX2	nc
4	nc	SCLK	nc
5	nc	nc	nc
6	nc	nc	nc
7	nc	nc	nc
8	nc	nc	nc
9	nc	/FSYNC	nc
10	nc	nc	nc
11	nc	nc	nc
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	nc
22	nc	nc	nc
23	nc	nc	nc
24	nc	nc	nc
25	nc	nc	nc

4.5 Compact PCI Backplane Connector J3, J5

cPCI connectors J3 and J5 are assembled for stability reasons, but do not carry any signal routing.

4.6 SCbus Connector JP1

Connector J4 carries the H.110 specific signals. The SCbus known in a PC environment consists of signals, which form a subgroup of the signals defined for H.110 bus. This subgroup of SCbus signlas is routed to a 26-pin male header according to standard SCbus definition for PCs. A flat cable can be connected to JP1 for connection with other add-in cards that support SCbus.

Table 9: SCbus Connector JP1

Pin	Signal	Signal	Pin
1	SCLKx2#	GND	2
3	SCLK	nc	4
5	FSYNC#	nc	6
7	CT_D0	GND	8
9	CT_D1	CT_D2	10
11	CT_D3	CT_D4	12
13	CT_D5	CT_D6	14
15	GND	CT_D7	16
17	CT_D8	CT_D9	18
19	CT_D10	CT_D11	20
21	GND	CT_D12	22
23	CT_D13	CT_D14	24
25	CT_D15	nc	26

5 Document's History

Version	Date	Description	Author
1.0	12.2.2003	Initial Version	ga